AMD Xilinx - XC2V8000-5FFG1517C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	11648
Number of Logic Elements/Cells	-
Total RAM Bits	3096576
Number of I/O	1108
Number of Gates	8000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v8000-5ffg1517c

Table 1: **Virtex-II Field-Programmable Gate Array Family Members**

Device	System Gates	CLB (1 CLB = 4 slices = Max 128 bits)			Multiplier Blocks	SelectRAM Blocks		DCMs	Max I/O Pads(1)
		Array Row x Col.	Slices	Maximum Distributed RAM Kbits		18 Kbit Blocks	Max RAM (Kbits)		
XC2V40	40K	8 x 8	256	8	4	4	72	4	88
XC2V80	80K	16 x 8	512	16	8	8	144	4	120
XC2V250	250K	24 x 16	1,536	48	24	24	432	8	200
XC2V500	500K	32 x 24	3,072	96	32	32	576	8	264
XC2V1000	1M	40 x 32	5,120	160	40	40	720	8	432
XC2V1500	1.5M	48 x 40	7,680	240	48	48	864	8	528
XC2V2000	2M	56 x 48	10,752	336	56	56	1,008	8	624
XC2V3000	3M	64 x 56	14,336	448	96	96	1,728	12	720
XC2V4000	4M	80 x 72	23,040	720	120	120	2,160	12	912
XC2V6000	6M	96 x 88	33,792	1,056	144	144	2,592	12	1,104
XC2V8000	8M	112 x 104	46,592	1,456	168	168	3,024	12	1,108

Notes:
1. See details in Table 2, "Maximum Number of User I/O Pads".

General Description

The Virtex-II family is a platform FPGA developed for high performance from low-density to high-density designs that are based on IP cores and customized modules. The family delivers complete solutions for telecommunication, wireless, networking, video, and DSP applications, including PCI, LVDS, and DDR interfaces.

The leading-edge 0.15 µm / 0.12 µm CMOS 8-layer metal process and the Virtex-II architecture are optimized for high speed with low power consumption. Combining a wide variety of flexible features and a large range of densities up to 10 million system gates, the Virtex-II family enhances programmable logic design capabilities and is a powerful alternative to mask-programmed gates arrays. As shown in Table 1, the Virtex-II family comprises 11 members, ranging from 40K to 8M system gates.

Packaging

Offerings include ball grid array (BGA) packages with 0.80 mm, 1.00 mm, and 1.27 mm pitches. In addition to traditional wire-bond interconnects, flip-chip interconnect is used in some of the BGA offerings. The use of flip-chip interconnect offers more I/Os than is possible in wire-bond versions of the similar packages. Flip-chip construction offers the combination of high pin count with high thermal capacity.

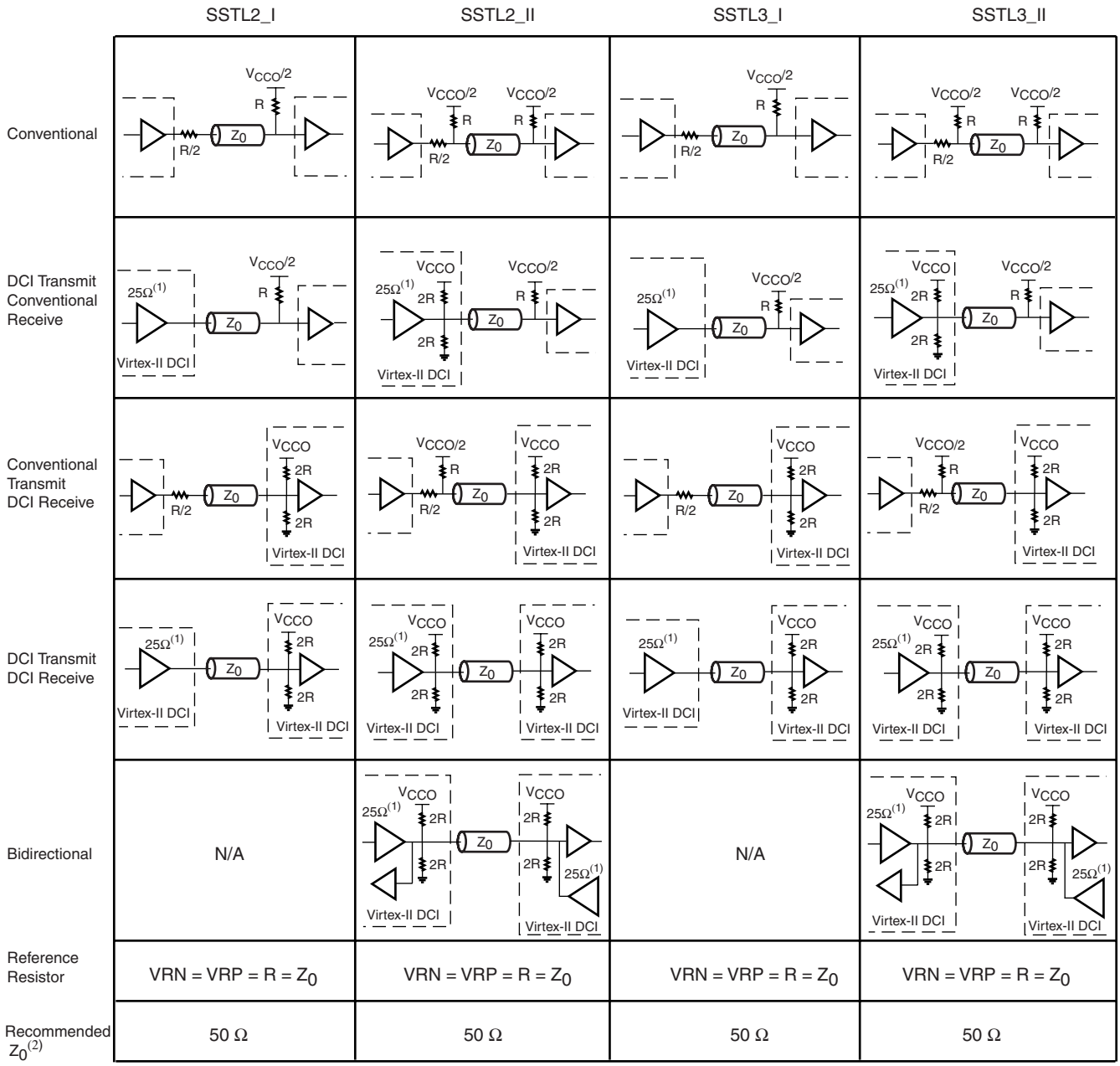
Wire-bond packages CS, FG, and BG are optionally availabe in Pb-free versions CSG, FGG, and BGG. See Virtex-II Ordering Examples, page 6.

Table 2 shows the maximum number of user I/Os available. The Virtex-II device/package combination table (Table 6 at the end of this section) details the maximum number of I/Os for each device and package using wire-bond or flip-chip technology.

Table 2: **Maximum Number of User I/O Pads**

Device	Wire-Bond	Flip-Chip
XC2V40	88	-
XC2V80	120	-
XC2V250	200	-
XC2V500	264	-
XC2V1000	328	432
XC2V1500	392	528
XC2V2000	-	624
XC2V3000	516	720
XC2V4000	-	912
XC2V6000	-	1,104
XC2V8000	-	1,108

Figure 12 provides examples illustrating the use of the SSTL2_I_DCI, SSTL2_II_DCI, SSTL3_I_DCI, and SSTL3_II_DCI I/O standards. For a complete list, see the **Virtex-II Platform FPGA User Guide**.



Notes:
1. The SSTL-compatible 25Ω series resistor is accounted for in the DCI buffer, and it is not DCI controlled.
2. Z_0 is the recommended PCB trace impedance.

DS031_65b_112502

Figure 12: **SSTL DCI Usage Examples**

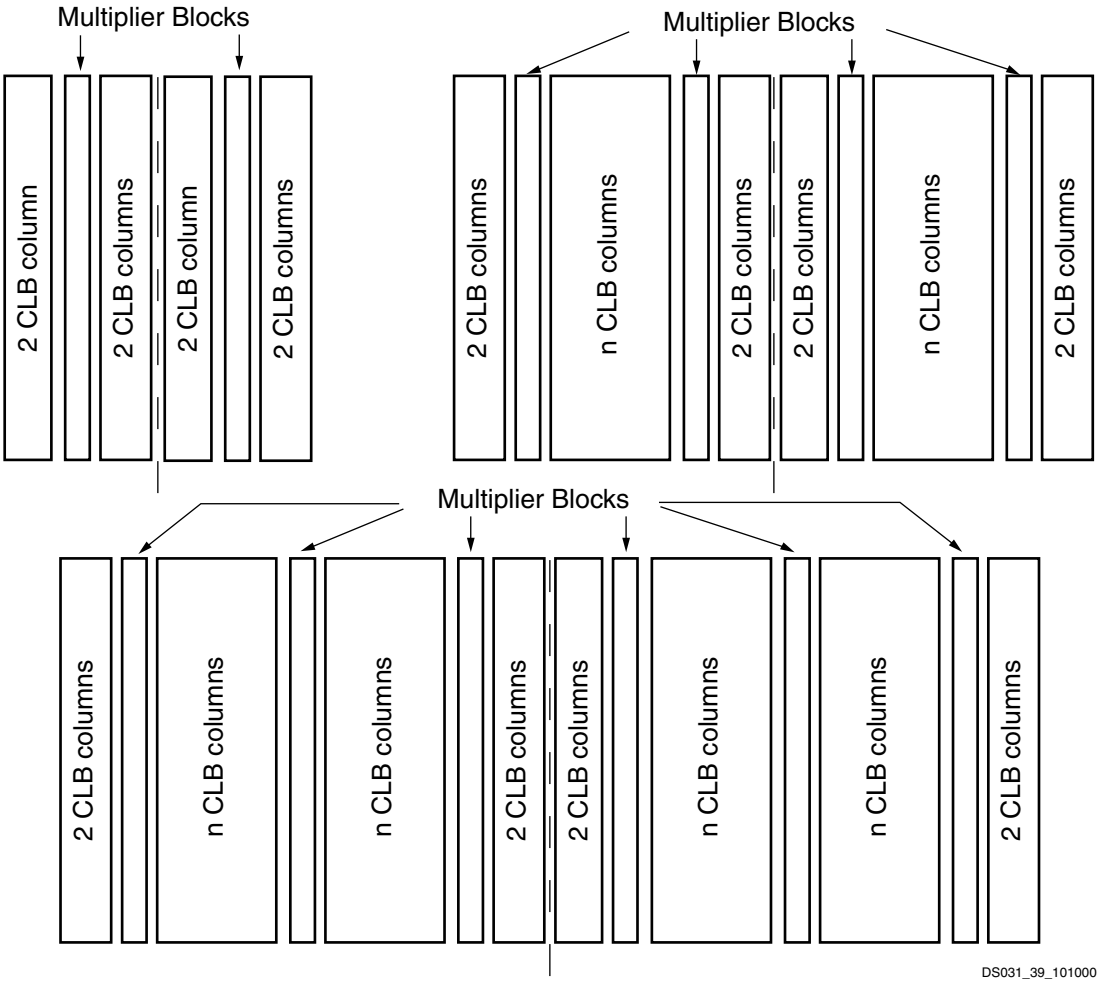


Figure 37: **Multipliers (2-column, 4-column, and 6-column)**

Global Clock Multiplexer Buffers

Virtex-II devices have 16 clock input pins that can also be used as regular user I/Os. Eight clock pads are on the top edge of the device, in the middle of the array, and eight are on the bottom edge, as illustrated in Figure 38.

The global clock multiplexer buffer represents the input to dedicated low-skew clock tree distribution in Virtex-II devices. Like the clock pads, eight global clock multiplexer buffers are on the top edge of the device and eight are on the bottom edge.

Each global clock buffer can either be driven by the clock pad to distribute a clock directly to the device, or driven by the Digital Clock Manager (DCM), discussed in Digital Clock Manager (DCM), page 29. Each global clock buffer can also be driven by local interconnects. The DCM has clock output(s) that can be connected to global clock buffer inputs, as shown in Figure 39.

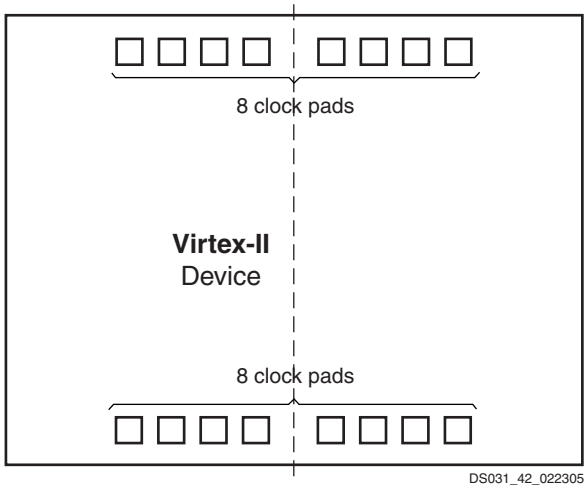


Figure 38: **Virtex-II Clock Pads**

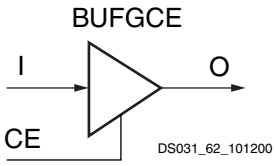


Figure 42: **Virtex-II BUFGCE Function**

If the CE input is inactive (Low) prior to the incoming rising clock edge, the following clock pulse does not pass through the clock buffer, and the output stays Low. Any level change of CE during the incoming clock High time has no effect. CE must not change during a short setup window just prior to the rising clock edge on the BUFGCE input I. Violating this setup time requirement can result in an undefined runt pulse output.

BUFGMUX

BUFGMUX can switch between two unrelated, even asynchronous clocks. Basically, a Low on S selects the I0 input, a High on S selects the I1 input. Switching from one clock to the other is done in such a way that the output High and Low time is never shorter than the shortest High or Low time of either input clock. As long as the presently selected clock is High, any level change of S has no effect .

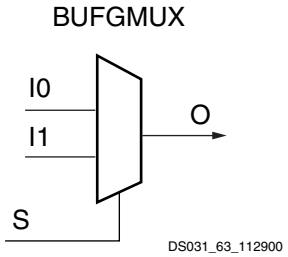


Figure 43: **Virtex-II BUFGMUX Function**

If the presently selected clock is Low while S changes, or if it goes Low after S has changed, the output is kept Low until the other ("to-be-selected") clock has made a transition from High to Low. At that instant, the new clock starts driving the output.

The two clock inputs can be asynchronous with regard to each other, and the S input can change at any time, except for a short setup time prior to the rising edge of the presently selected clock (I0 or I1). Violating this setup time requirement can result in an undefined runt pulse output.

All Virtex-II devices have 16 global clock multiplexer buffers.

Figure 44 shows a switchover from I0 to I1.

- The current clock is CLK0.
- S is activated High.
- If CLK0 is currently High, the multiplexer waits for CLK0 to go Low.
- Once CLK0 is Low, the multiplexer output stays Low until CLK1 transitions High to Low.
- When CLK1 transitions from High to Low, the output switches to CLK1.
- No glitches or short pulses can appear on the output.

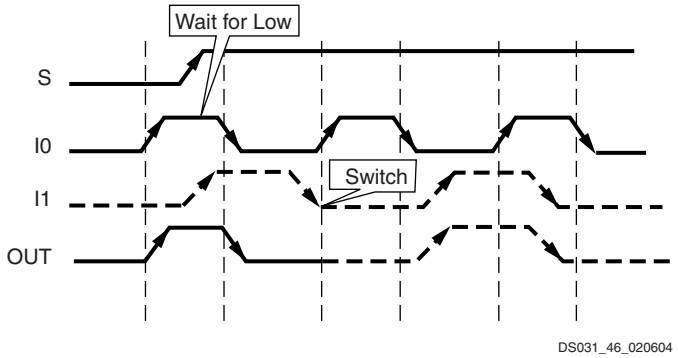


Figure 44: **Clock Multiplexer Waveform Diagram**

Local Clocking

In addition to global clocks, there are local clock resources in the Virtex-II devices. There are more than 72 local clocks in the Virtex-II family. These resources can be used for many different applications, including but not limited to memory interfaces. For example, even using only the left and right I/O banks, Virtex-II FPGAs can support up to 50 local clocks for DDR SDRAM. These interfaces can operate beyond 200 MHz on Virtex-II devices.

Digital Clock Manager (DCM)

The Virtex-II DCM offers a wide range of powerful clock management features.

- **Clock De-skew**: The DCM generates new system clocks (either internally or externally to the FPGA), which are phase-aligned to the input clock, thus eliminating clock distribution delays.
- **Frequency Synthesis**: The DCM generates a wide range of output clock frequencies, performing very flexible clock multiplication and division.
- **Phase Shifting**: The DCM provides both coarse phase shifting and fine-grained phase shifting with dynamic phase shift control.

The DCM utilizes fully digital delay lines allowing robust high-precision control of clock phase and frequency. It also utilizes fully digital feedback systems, operating dynamically to compensate for temperature and voltage variations during operation.

Up to four of the nine DCM clock outputs can drive inputs to global clock buffers or global clock multiplexer buffers simultaneously (see Figure 45). All DCM clock outputs can simultaneously drive general routing resources, including routes to output buffers.

Enhanced Multiplier Switching Characteristics

Table 26 and Table 27 provide timing information for enhanced Virtex-II multiplier blocks, available in stepping revisions of Virtex-II devices. For more information on stepping revisions, availability, and ordering instructions, see your local sales representative.

Table 26: **Enhanced Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Propagation Delay to Output Pin					
Input to Pin 35	T_{MULT1_P35}	4.66	5.14	5.91	ns, Max
Input to Pin 34	T_{MULT1_P34}	4.57	5.03	5.79	ns, Max
Input to Pin 33	T_{MULT1_P33}	4.47	4.93	5.66	ns, Max
Input to Pin 32	T_{MULT1_P32}	4.37	4.82	5.54	ns, Max
Input to Pin 31	T_{MULT1_P31}	4.28	4.71	5.42	ns, Max
Input to Pin 30	T_{MULT1_P30}	4.18	4.61	5.29	ns, Max
Input to Pin 29	T_{MULT1_P29}	4.08	4.50	5.17	ns, Max
Input to Pin 28	T_{MULT1_P28}	3.99	4.39	5.05	ns, Max
Input to Pin 27	T_{MULT1_P27}	3.89	4.28	4.92	ns, Max
Input to Pin 26	T_{MULT1_P26}	3.79	4.18	4.80	ns, Max
Input to Pin 25	T_{MULT1_P25}	3.69	4.07	4.68	ns, Max
Input to Pin 24	T_{MULT1_P24}	3.60	3.96	4.56	ns, Max
Input to Pin 23	T_{MULT1_P23}	3.50	3.86	4.43	ns, Max
Input to Pin 22	T_{MULT1_P22}	3.40	3.75	4.31	ns, Max
Input to Pin 21	T_{MULT1_P21}	3.31	3.64	4.19	ns, Max
Input to Pin 20	T_{MULT1_P20}	3.21	3.54	4.06	ns, Max
Input to Pin 19	T_{MULT1_P19}	3.11	3.43	3.94	ns, Max
Input to Pin 18	T_{MULT1_P18}	3.02	3.32	3.82	ns, Max
Input to Pin 17	T_{MULT1_P17}	2.92	3.21	3.69	ns, Max
Input to Pin 16	T_{MULT1_P16}	2.82	3.11	3.57	ns, Max
Input to Pin 15	T_{MULT1_P15}	2.72	3.00	3.45	ns, Max
Input to Pin 14	T_{MULT1_P14}	2.63	2.89	3.33	ns, Max
Input to Pin 13	T_{MULT1_P13}	2.53	2.79	3.20	ns, Max
Input to Pin 12	T_{MULT1_P12}	2.43	2.68	3.08	ns, Max
Input to Pin 11	T_{MULT1_P11}	2.34	2.57	2.96	ns, Max
Input to Pin 10	T_{MULT1_P10}	2.24	2.47	2.83	ns, Max
Input to Pin 9	T_{MULT1_P9}	2.14	2.36	2.71	ns, Max
Input to Pin 8	T_{MULT1_P8}	2.05	2.25	2.59	ns, Max
Input to Pin 7	T_{MULT1_P7}	1.95	2.14	2.46	ns, Max
Input to Pin 6	T_{MULT1_P6}	1.85	2.04	2.34	ns, Max
Input to Pin 5	T_{MULT1_P5}	1.75	1.93	2.22	ns, Max
Input to Pin 4	T_{MULT1_P4}	1.66	1.82	2.10	ns, Max
Input to Pin 3	T_{MULT1_P3}	1.56	1.72	1.97	ns, Max
Input to Pin 2	T_{MULT1_P2}	1.46	1.61	1.85	ns, Max
Input to Pin 1	T_{MULT1_P1}	1.37	1.50	1.73	ns, Max
Input to Pin 0	T_{MULT1_P0}	1.27	1.40	1.60	ns, Max

Table 3: **Virtex-II Device/Package Combinations and Maximum Number of Available I/Os**

Package	Available I/Os										
	XC2V 40	XC2V 80	XC2V 250	XC2V 500	XC2V 1000	XC2V 1500	XC2V 2000	XC2V 3000	XC2V 4000	XC2V 6000	XC2V 8000
CS144	88	92	92	-	-	-	-	-	-	-	-
FG256	88	120	172	172	172	-	-	-	-	-	-
FG456	-	-	200	264	324	-	-	-	-	-	-
FG676	-	-	-	-	-	392	456	484	-	-	-
FF896	-	-	-	-	432	528	624	-	-	-	-
FF1152	-	-	-	-	-	-	-	720	824	824	824
FF1517	-	-	-	-	-	-	-	-	912	1,104	1,108
BG575	-	-	-	-	328	392	408	-	-	-	-
BG728	-	-	-	-	-	-	-	516	-	-	-
BF957	-	-	-	-	-	-	624	684	684	684	-

Virtex-II Pin Definitions

This section describes the pinouts for Virtex-II devices in the following packages:

- CS144: wire-bond chip-scale ball grid array (BGA) of 0.80 mm pitch
- FG256, FG456, and FG676: wire-bond fine-pitch BGA of 1.00 mm pitch
- FF896, FF1152, FF1517: flip-chip fine-pitch BGA of 1.00 mm pitch
- BG575 and BG728: wire-bond BGA of 1.27 mm pitch
- BF957: flip-chip BGA of 1.27 mm pitch

All of the devices supported in a particular package are pinout compatible and are listed in the same table (one table per package). In addition, the FG456 and FG676 packages are compatible, as are the FF896 and FF1152 packages. Pins that are not available for the smallest devices are listed in right-hand columns.

Each device is split into eight I/O banks to allow for flexibility in the choice of I/O standards (see the Virtex-II *Data Sheet*). Global pins, including JTAG, configuration, and power/ground pins, are listed at the end of each table. Table 4 provides definitions for all pin types.

The FG256 pinouts (Table 6) is included as an example. All Virtex-II pinout tables are available on the distribution CD-ROM, or on the web (at **http://www.xilinx.com**).

FG256/FGG256 Fine-Pitch BGA Package

As shown in Table 6, XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000 Virtex-II devices are available in the FG256/FGG256 fine-pitch BGA package. The pins in the XC2V250, XC2V500, and XC2V1000 devices are same. The No Connect columns show pin differences for the XC2V40 and XC2V80 devices. Following this table are the FG256/FGG256 Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
0	IO_L01N_0	C4		
0	IO_L01P_0	B4		
0	IO_L02N_0	D5		
0	IO_L02P_0	C5		
0	IO_L03N_0/VRP_0	B5		
0	IO_L03P_0/VRN_0	A5		
0	IO_L04N_0/VREF_0	D6	NC	NC
0	IO_L04P_0	C6	NC	NC
0	IO_L05N_0	B6	NC	NC
0	IO_L05P_0	A6	NC	NC
0	IO_L92N_0	E6	NC	NC
0	IO_L92P_0	E7	NC	NC
0	IO_L93N_0	D7	NC	NC
0	IO_L93P_0	C7	NC	NC
0	IO_L94N_0/VREF_0	B7		
0	IO_L94P_0	A7		
0	IO_L95N_0/GCLK7P	D8		
0	IO_L95P_0/GCLK6S	C8		
0	IO_L96N_0/GCLK5P	B8		
0	IO_L96P_0/GCLK4S	A8		
1	IO_L96N_1/GCLK3P	A9		
1	IO_L96P_1/GCLK2S	B9		
1	IO_L95N_1/GCLK1P	C9		
1	IO_L95P_1/GCLK0S	D9		
1	IO_L94N_1	A10		
1	IO_L94P_1/VREF_1	B10		
1	IO_L93N_1	C10	NC	NC
1	IO_L93P_1	D10	NC	NC
1	IO_L92N_1	E10	NC	NC

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
3	IO_L52P_3	P18	NC	
3	IO_L51N_3/VREF_3	P22	NC	
3	IO_L51P_3	P21	NC	
3	IO_L49N_3	P20	NC	
3	IO_L49P_3	P19	NC	
3	IO_L48N_3	R22		
3	IO_L48P_3	R21		
3	IO_L46N_3	R20		
3	IO_L46P_3	R19		
3	IO_L45N_3/VREF_3	R18		
3	IO_L45P_3	P17		
3	IO_L43N_3	T22		
3	IO_L43P_3	T21		
3	IO_L24N_3	T20	NC	NC
3	IO_L24P_3	T19	NC	NC
3	IO_L22N_3	U22	NC	NC
3	IO_L22P_3	U21	NC	NC
3	IO_L21N_3/VREF_3	U20	NC	NC
3	IO_L21P_3	U19	NC	NC
3	IO_L19N_3	T18	NC	NC
3	IO_L19P_3	U18	NC	NC
3	IO_L06N_3	V22		
3	IO_L06P_3	V21		
3	IO_L04N_3	V20		
3	IO_L04P_3	V19		
3	IO_L03N_3/VREF_3	W22		
3	IO_L03P_3	W21		
3	IO_L02N_3/VRP_3	Y22		
3	IO_L02P_3/VRN_3	Y21		
3	IO_L01N_3	W20		
3	IO_L01P_3	AA20		
4	IO_L01N_4/BUSY/DOUT(1)	AB19		
4	IO_L01P_4/INIT_B	AA19		

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
5	IO_L06P_5	W6		
5	IO_L05N_5/VRP_5	V7		
5	IO_L05P_5/VRN_5	V6		
5	IO_L04N_5	AB5		
5	IO_L04P_5/VREF_5	AA5		
5	IO_L03N_5/D4/ALT_VRP_5	Y5		
5	IO_L03P_5/D5/ALT_VRN_5	W5		
5	IO_L02N_5/D6	AB4		
5	IO_L02P_5/D7	AA4		
5	IO_L01N_5/RDWR_B	Y4		
5	IO_L01P_5/CS_B	AA3		
6	IO_L01P_6	V5		
6	IO_L01N_6	U5		
6	IO_L02P_6/VRN_6	Y2		
6	IO_L02N_6/VRP_6	Y1		
6	IO_L03P_6	V4		
6	IO_L03N_6/VREF_6	V3		
6	IO_L04P_6	W2		
6	IO_L04N_6	W1		
6	IO_L06P_6	U4		
6	IO_L06N_6	U3		
6	IO_L19P_6	V2	NC	NC
6	IO_L19N_6	V1	NC	NC
6	IO_L21P_6	U2	NC	NC
6	IO_L21N_6/VREF_6	U1	NC	NC
6	IO_L22P_6	T5	NC	NC
6	IO_L22N_6	R5	NC	NC
6	IO_L24P_6	T4	NC	NC
6	IO_L24N_6	T3	NC	NC
6	IO_L43P_6	T2		
6	IO_L43N_6	T1		
6	IO_L45P_6	R4		
6	IO_L45N_6/VREF_6	R3		

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
7	VCCO_7	H6		
7	VCCO_7	G6		
NA	CCLK	Y19		
NA	PROG_B	A2		
NA	DONE	AB20		
NA	M0	AB2		
NA	M1	W3		
NA	M2	AB3		
NA	HSWAP_EN	B3		
NA	TCK	C19		
NA	TDI	D3		
NA	TDO	D20		
NA	TMS	B20		
NA	PWRDWN_B	AB21		
NA	DXN	D5		
NA	DXP	A3		
NA	VBATT	A21		
NA	RSVD	A20		
NA	VCCAUX	AB11		
NA	VCCAUX	AA22		
NA	VCCAUX	AA1		
NA	VCCAUX	M22		
NA	VCCAUX	L1		
NA	VCCAUX	B22		
NA	VCCAUX	B1		
NA	VCCAUX	A12		
NA	VCCINT	U17		
NA	VCCINT	U6		
NA	VCCINT	T16		
NA	VCCINT	T15		
NA	VCCINT	T8		
NA	VCCINT	T7		

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
NA	GND	M10		
NA	GND	M9		
NA	GND	L14		
NA	GND	L13		
NA	GND	L12		
NA	GND	L11		
NA	GND	L10		
NA	GND	L9		
NA	GND	K14		
NA	GND	K13		
NA	GND	K12		
NA	GND	K11		
NA	GND	K10		
NA	GND	K9		
NA	GND	J14		
NA	GND	J13		
NA	GND	J12		
NA	GND	J11		
NA	GND	J10		
NA	GND	J9		
NA	GND	D19		
NA	GND	D4		
NA	GND	C20		
NA	GND	C3		
NA	GND	B21		
NA	GND	B2		
NA	GND	A22		
NA	GND	A1		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
7	IO_L78P_7	N6
7	IO_L78N_7	N7
7	IO_L76P_7	N9
7	IO_L76N_7	N8
7	IO_L75P_7/VREF_7	N5
7	IO_L75N_7	M6
7	IO_L73P_7	M1
7	IO_L73N_7	M2
7	IO_L72P_7	M4
7	IO_L72N_7	M5
7	IO_L70P_7	M8
7	IO_L70N_7	M9
7	IO_L69P_7/VREF_7	L1
7	IO_L69N_7	L2
7	IO_L67P_7	L3
7	IO_L67N_7	L4
7	IO_L54P_7	K1
7	IO_L54N_7	K2
7	IO_L52P_7	K4
7	IO_L52N_7	K5
7	IO_L51P_7/VREF_7	L6
7	IO_L51N_7	L7
7	IO_L49P_7	K6
7	IO_L49N_7	K7
7	IO_L48P_7	L8
7	IO_L48N_7	K8
7	IO_L46P_7	J1
7	IO_L46N_7	H1
7	IO_L45P_7/VREF_7	J2
7	IO_L45N_7	J3
7	IO_L43P_7	K3
7	IO_L43N_7	J4
7	IO_L30P_7	H3
7	IO_L30N_7	H4
7	IO_L28P_7	J5
7	IO_L28N_7	J6

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
5	IO_L23N_5	AD20		
5	IO_L23P_5	AD21		
5	IO_L22N_5	AK25		
5	IO_L22P_5	AK24		
5	IO_L21N_5/VREF_5	AH24		
5	IO_L21P_5	AH25		
5	IO_L20N_5	AE21		
5	IO_L20P_5	AD22		
5	IO_L19N_5	AJ25		
5	IO_L19P_5	AJ24		
5	IO_L06N_5	AG25		
5	IO_L06P_5	AG24		
5	IO_L05N_5/VRP_5	AC20		
5	IO_L05P_5/VRN_5	AC21		
5	IO_L04N_5	AK26		
5	IO_L04P_5/VREF_5	AK27		
5	IO_L03N_5/D4/ALT_VRP_5	AH26		
5	IO_L03P_5/D5/ALT_VRN_5	AJ27		
5	IO_L02N_5/D6	AE22		
5	IO_L02P_5/D7	AE23		
5	IO_L01N_5/RDWR_B	AJ28		
5	IO_L01P_5/CS_B	AK29		
6	IO_L01P_6	AC22		
6	IO_L01N_6	AB23		
6	IO_L02P_6/VRN_6	AG28		
6	IO_L02N_6/VRP_6	AF28		
6	IO_L03P_6	AJ30		
6	IO_L03N_6/VREF_6	AH30		
6	IO_L04P_6	AD23		
6	IO_L04N_6	AC23		
6	IO_L05P_6	AF27		
6	IO_L05N_6	AE27		
6	IO_L06P_6	AG29		
6	IO_L06N_6	AH29		
6	IO_L19P_6	AE24		
6	IO_L19N_6	AD24		

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
5	IO_L79P_5	AP21	NC
5	IO_L78N_5	AK22	
5	IO_L78P_5	AK21	
5	IO_L77N_5	AD18	
5	IO_L77P_5	AD19	
5	IO_L76N_5	AN22	
5	IO_L76P_5	AN21	
5	IO_L75N_5/VREF_5	AJ20	
5	IO_L75P_5	AH20	
5	IO_L74N_5	AG19	
5	IO_L74P_5	AG20	
5	IO_L73N_5	AP24	
5	IO_L73P_5	AP23	
5	IO_L72N_5	AL23	
5	IO_L72P_5	AL22	
5	IO_L71N_5	AF20	
5	IO_L71P_5	AF21	
5	IO_L70N_5	AM24	
5	IO_L70P_5	AM23	
5	IO_L69N_5/VREF_5	AJ21	
5	IO_L69P_5	AJ22	
5	IO_L68N_5	AJ24	
5	IO_L68P_5	AJ23	
5	IO_L67N_5	AN24	
5	IO_L67P_5	AN23	
5	IO_L60N_5	AN26	NC
5	IO_L60P_5	AN25	NC
5	IO_L54N_5	AL25	
5	IO_L54P_5	AL24	
5	IO_L53N_5	AE20	
5	IO_L53P_5	AE21	
5	IO_L52N_5	AN27	
5	IO_L52P_5	AP26	
5	IO_L51N_5/VREF_5	AP29	
5	IO_L51P_5	AP28	
5	IO_L50N_5	AG21	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
2	IO_L81P_2/VREF_2	U5		
2	IO_L82N_2	V2		
2	IO_L82P_2	U2		
2	IO_L83N_2	V8		
2	IO_L83P_2	W8		
2	IO_L84N_2	W7		
2	IO_L84P_2	V7		
2	IO_L91N_2	W1		
2	IO_L91P_2	V1		
2	IO_L92N_2	Y11		
2	IO_L92P_2	Y12		
2	IO_L93N_2	W4		
2	IO_L93P_2/VREF_2	V4		
2	IO_L94N_2	W2		
2	IO_L94P_2	W3		
2	IO_L95N_2	Y8		
2	IO_L95P_2	Y9		
2	IO_L96N_2	W5		
2	IO_L96P_2	W6		
3	IO_L96N_3	AB8		
3	IO_L96P_3	AA8		
3	IO_L95N_3	Y3		
3	IO_L95P_3	AA3		
3	IO_L94N_3	Y6		
3	IO_L94P_3	AA6		
3	IO_L93N_3/VREF_3	AB9		
3	IO_L93P_3	AA9		
3	IO_L92N_3	AA1		
3	IO_L92P_3	AB1		
3	IO_L91N_3	Y5		
3	IO_L91P_3	AA5		
3	IO_L84N_3	AB10		
3	IO_L84P_3	AA10		
3	IO_L83N_3	AA2		
3	IO_L83P_3	AB2		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
3	IO_L82N_3	AA4		
3	IO_L82P_3	AB4		
3	IO_L81N_3/VREF_3	AB11		
3	IO_L81P_3	AA11		
3	IO_L80N_3	AC1		
3	IO_L80P_3	AD1		
3	IO_L79N_3	AA7		
3	IO_L79P_3	AB7		
3	IO_L78N_3	AB12		
3	IO_L78P_3	AA12		
3	IO_L77N_3	AC2		
3	IO_L77P_3	AC3		
3	IO_L76N_3	AB5		
3	IO_L76P_3	AC5		
3	IO_L75N_3/VREF_3	AD9		
3	IO_L75P_3	AC9		
3	IO_L74N_3	AD2		
3	IO_L74P_3	AE2		
3	IO_L73N_3	AB6		
3	IO_L73P_3	AC6		
3	IO_L72N_3	AD10		
3	IO_L72P_3	AC10		
3	IO_L71N_3	AD3		
3	IO_L71P_3	AE3		
3	IO_L70N_3	AC7		
3	IO_L70P_3	AD7		
3	IO_L69N_3/VREF_3	AE8		
3	IO_L69P_3	AD8		
3	IO_L68N_3	AE1		
3	IO_L68P_3	AF1		
3	IO_L67N_3	AD4		
3	IO_L67P_3	AE4		
3	IO_L60N_3	AD12		
3	IO_L60P_3	AC12		
3	IO_L59N_3	AF3		
3	IO_L59P_3	AG3		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
3	IO_L10N_3	AK7	NC	
3	IO_L10P_3	AL7	NC	
3	IO_L09N_3/VREF_3	AK11	NC	
3	IO_L09P_3	AJ10	NC	
3	IO_L08N_3	AR1	NC	
3	IO_L08P_3	AT1	NC	
3	IO_L07N_3	AM5	NC	
3	IO_L07P_3	AN5	NC	
3	IO_L06N_3	AM7		
3	IO_L06P_3	AL8		
3	IO_L05N_3	AP3		
3	IO_L05P_3	AP4		
3	IO_L04N_3	AM6		
3	IO_L04P_3	AN6		
3	IO_L03N_3/VREF_3	AJ13		
3	IO_L03P_3	AH13		
3	IO_L02N_3/VRP_3	AR3		
3	IO_L02P_3/VRN_3	AT2		
3	IO_L01N_3	AP5		
3	IO_L01P_3	AR4		
4	IO_L01N_4/BUSY/DOUT(1)	AV4		
4	IO_L01P_4/INIT_B	AU4		
4	IO_L02N_4/D0/DIN(1)	AM9		
4	IO_L02P_4/D1	AM10		
4	IO_L03N_4/D2/ALT_VRP_4	AT6		
4	IO_L03P_4/D3/ALT_VRN_4	AR6		
4	IO_L04N_4/VREF_4	AU6		
4	IO_L04P_4	AU5		
4	IO_L05N_4/VRP_4	AL10		
4	IO_L05P_4/VRN_4	AL11		
4	IO_L06N_4	AR8		
4	IO_L06P_4	AR7		
4	IO_L07N_4	AW5	NC	
4	IO_L07P_4	AW4	NC	
4	IO_L08N_4	AK12	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
6	IO_L23N_6	AM38		
6	IO_L24P_6	AM36		
6	IO_L24N_6	AN36		
6	IO_L25P_6	AH30		
6	IO_L25N_6	AG30		
6	IO_L26P_6	AM37		
6	IO_L26N_6	AL37		
6	IO_L27P_6	AK34		
6	IO_L27N_6/VREF_6	AL34		
6	IO_L28P_6	AG29		
6	IO_L28N_6	AF29		
6	IO_L29P_6	AL35		
6	IO_L29N_6	AK35		
6	IO_L30P_6	AH33		
6	IO_L30N_6	AJ33		
6	IO_L31P_6	AJ32	NC	
6	IO_L31N_6	AH32	NC	
6	IO_L32P_6	AM39	NC	
6	IO_L32N_6	AL39	NC	
6	IO_L33P_6	AK36	NC	
6	IO_L33N_6/VREF_6	AL36	NC	
6	IO_L34P_6	AF28	NC	
6	IO_L34N_6	AE28	NC	
6	IO_L35P_6	AL38	NC	
6	IO_L35N_6	AK38	NC	
6	IO_L36P_6	AH34	NC	
6	IO_L36N_6	AJ34	NC	
6	IO_L43P_6	AG31		
6	IO_L43N_6	AF31		
6	IO_L44P_6	AK37		
6	IO_L44N_6	AJ37		
6	IO_L45P_6	AH36		
6	IO_L45N_6/VREF_6	AJ36		
6	IO_L46P_6	AF30		
6	IO_L46N_6	AE30		
6	IO_L47P_6	AK39		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
7	IO_L74P_7	U31		
7	IO_L74N_7	T31		
7	IO_L73P_7	R38		
7	IO_L73N_7	T38		
7	IO_L72P_7	T33		
7	IO_L72N_7	U33		
7	IO_L71P_7	U30		
7	IO_L71N_7	T30		
7	IO_L70P_7	R37		
7	IO_L70N_7	T37		
7	IO_L69P_7/VREF_7	R36		
7	IO_L69N_7	T36		
7	IO_L68P_7	T32		
7	IO_L68N_7	R32		
7	IO_L67P_7	P39		
7	IO_L67N_7	R39		
7	IO_L60P_7	R35		
7	IO_L60N_7	T35		
7	IO_L59P_7	U28		
7	IO_L59N_7	T28		
7	IO_L58P_7	N37		
7	IO_L58N_7	P37		
7	IO_L57P_7/VREF_7	R34		
7	IO_L57N_7	T34		
7	IO_L56P_7	T29		
7	IO_L56N_7	R29		
7	IO_L55P_7	M39		
7	IO_L55N_7	N39		
7	IO_L54P_7	N36		
7	IO_L54N_7	P36		
7	IO_L53P_7	R30		
7	IO_L53N_7	P30		
7	IO_L52P_7	M38		
7	IO_L52N_7	N38		
7	IO_L51P_7/VREF_7	P33		
7	IO_L51N_7	R33		

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
2	IO_L23N_2	E2	
2	IO_L23P_2	F2	
2	IO_L24N_2	H4	
2	IO_L24P_2	J4	
2	IO_L25N_2	K8	NC
2	IO_L25P_2	L8	NC
2	IO_L27N_2	J7	NC
2	IO_L27P_2/VREF_2	K7	NC
2	IO_L43N_2	F1	
2	IO_L43P_2	G1	
2	IO_L44N_2	L9	
2	IO_L44P_2	M9	
2	IO_L45N_2	G2	
2	IO_L45P_2/VREF_2	J2	
2	IO_L46N_2	H3	
2	IO_L46P_2	J3	
2	IO_L47N_2	J6	
2	IO_L47P_2	L6	
2	IO_L48N_2	J5	
2	IO_L48P_2	K5	
2	IO_L49N_2	H1	
2	IO_L49P_2	J1	
2	IO_L50N_2	N10	
2	IO_L50P_2	P10	
2	IO_L51N_2	L7	
2	IO_L51P_2/VREF_2	M7	
2	IO_L52N_2	K3	
2	IO_L52P_2	L3	
2	IO_L53N_2	M8	
2	IO_L53P_2	N8	
2	IO_L54N_2	L5	
2	IO_L54P_2	M5	
2	IO_L67N_2	K2	
2	IO_L67P_2	L2	
2	IO_L68N_2	M6	
2	IO_L68P_2	N6	
2	IO_L69N_2	L4	
2	IO_L69P_2/VREF_2	M4	