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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	166MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	1/10/100Mbps (1)
SATA	-
USB	USB 2.0 (2)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Hardware ID
Package / Case	208-LQFP
Supplier Device Package	208-LQFP
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep9301-cq

Table of Contents

List of Tables

PLL and Clocking

The Processor and the Peripheral Clocks operate from a single 14.7456 MHz crystal.

The Real Time Clock operates from a 32.768 KHz external oscillator.

Table J. PLL and Clocking Pin Assignments

Pin Mnemonic	Pin Name - Description
XTALI	Main Oscillator Input
XTALO	Main Oscillator Output
VDD_PLL	Main Oscillator Power
GND_PLL	Main Oscillator Ground

Timers

The Watchdog Timer ensures proper operation by requiring periodic attention to prevent a reset-on-time-out.

Two 16-bit timers operate as free-running down counters or as periodic timers for fixed-interval interrupts and have a range of 0.03 ms to 4.27 seconds.

One 32-bit timer, plus a 6-bit prescale counter, has a range of 0.03 µs to 73.3 hours.

One 40-bit debug timer, plus a 6-bit prescale counter, has a range of 1.0 µs to 12.7 days.

Interrupt Controller

The interrupt controller allows up to 54 interrupts to generate an Interrupt Request (IRQ) or Fast Interrupt Request (FIQ) signal to the processor core. Thirty-two hardware priority assignments are provided for assisting IRQ vectoring, and two levels are provided for FIQ vectoring. This allows time-critical interrupts to be processed in the shortest time possible. Internal interrupts may be programmed as active high or active low level sensitive inputs. GPIO pins programmed as interrupts may be programmed as active high level sensitive, active low level sensitive, rising edge triggered, falling edge triggered, or combined rising/falling edge triggered.

- Supports 54 interrupts from a variety of sources (such as UARTs, GPIO and ADC)
- Routes interrupt sources to either the ARM920T's IRQ or FIQ (Fast IRQ) inputs
- Three dedicated off-chip interrupt lines INT[2:0] operate as active-high level-sensitive interrupts
- Any of the 19 GPIO lines maybe configured to generate interrupts
- Software supported priority mask for all FIQs and IRQs

Table K. External Interrupt Controller Pin Assignment

Pin Mnemonic	Pin Name - Description
INT[3] and INT[1:0]	External Interrupts 2, 1, 0

Note: INT[2] is not bonded out.

Dual LED Drivers

Two pins are assigned specifically to drive external LEDs.

Table L. Dual LED Pin Assignments

Pin Mnemonic	Pin Name - Description	Alternative Usage
GRLED	Green LED	General Purpose I/O
REDLED	Red LED	General Purpose I/O

General Purpose Input/Output (GPIO)

The 16 EGPIO and the 3 FGPIO pins may each be configured individually as an output, an input or an interrupt input.

There are 10 pins that may alternatively be used as input, output, or open-drain pins, but do not support interrupts. These pins are:

- Ethernet MDIO
- Both LED Outputs
- EEPROM Clock and Data
- HGPIO[5:2]
- CGPIO[0]

6 pins may alternatively be used as inputs only:

- CTSn, DSRn / DCDn
- 3 Interrupt Lines

2 pins may alternatively be used as outputs only:

- RTSn
- ARSTn

Table M. General Purpose Input/Output Pin Assignment

Pin Mnemonic	Pin Name - Description
EGPIO[15:0]	Expanded General Purpose Input / Output Pins with Interrupts
FGPIO[3:1]	Expanded General Purpose Input / Output Pins with Interrupts

Electrical Specifications

Absolute Maximum Ratings

(All grounds = 0 V, all voltages with respect to 0 V)

Parameter		Symbol	Min	Max	Unit
Power Supplies		RVDD CVDD VDD_PLL VDD_ADC	- - - -	3.96 2.16 2.16 3.96	V V V V
Total Power Dissipation	(Note 1)		-	2	W
Input Current per Pin, DC (Except supply pins)			-	±10	mA
Output current per pin, DC			-	±50	mA
Digital Input voltage	(Note 2)		-0.3	RVDD+0.3	V
Storage temperature			-40	+125	°C

Note: 1. Includes all power generated by AC and/or DC output loading.
2. The power supply pins are at recommended maximum values.
3. At ambient temperatures above 70° C, total power dissipation must be limited to less than 2.5 Watts.

WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Recommended Operating Conditions

(All grounds = 0 V, all voltages with respect to 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supplies	RVDD CVDD VDD_PLL VDD_ADC	3.0 1.65 1.65 3.0	3.3 1.80 1.80 3.3	3.6 1.94 1.94 3.6	V V V V
Operating Ambient Temperature - Commercial	T_A	0	+25	+70	°C
Operating Ambient Temperature - Industrial	T_A	-40	+25	+85	°C
Processor Clock Speed - Commercial	FCLK	-	-	166	MHz
Processor Clock Speed - Industrial	FCLK	-	-	166	MHz
System Clock Speed - Commercial	HCLK	-	-	66	MHz
System Clock Speed - Industrial	HCLK	-	-	66	MHz

DC Characteristics

(T_A = 0 to 70° C; CVDD = VDD_PLL = 1.8; RVDD = 3.3 V;
All grounds = 0 V; all voltages with respect to 0 V unless otherwise noted)

Parameter			Symbol	Min	Max	Unit
High level output voltage	Iout = -4 mA	(Note 4)	V_{oh}	0.85 × RVDD	-	V
Low level output voltage	Iout = 4 mA		V_{ol}	-	0.15 × RVDD	V
High level input voltage		(Note 5)	V_{ih}	0.65 × RVDD	VDD + 0.3	V
Low level input voltage		(Note 5)	V_{il}	–0.3	0.35 × RVDD	V
High level leakage current	Vin = 3.3 V	(Note 5)	I_{ih}	-	10	µA
Low level leakage current	Vin = 0	(Note 5)	I_{il}	-	-10	µA

Parameter		Min	Typ	Max	Unit
Power Supply Pins (Outputs Unloaded), 25° C					
Power Supply Current:	CVDD / VDD_PLL Total RVDD	- -	180 45	230 80	mA mA
Low-Power Mode Supply Current	CVDD / VDD_PLL Total RVDD	- -	2 1.0	3.5 2	mA mA

Note: 4. For open drain pins, high level output voltage is dependent on the external load.
5. All inputs that do not include internal pull-ups or pull-downs, must be externally driven for proper operation (See Table Q on page 38). If an input is not driven, it should be tied to power or ground, depending on the particular function. If an I/O pin is not driven and programmed as an input, it should be tied to power or ground through its own resistor.

Timings

Timing Diagram Conventions

This data sheet contains one or more timing diagrams. The following key explains the components used in these diagrams. Any variations are clearly labelled when they occur. Therefore, no additional meaning should be attached unless specifically stated.

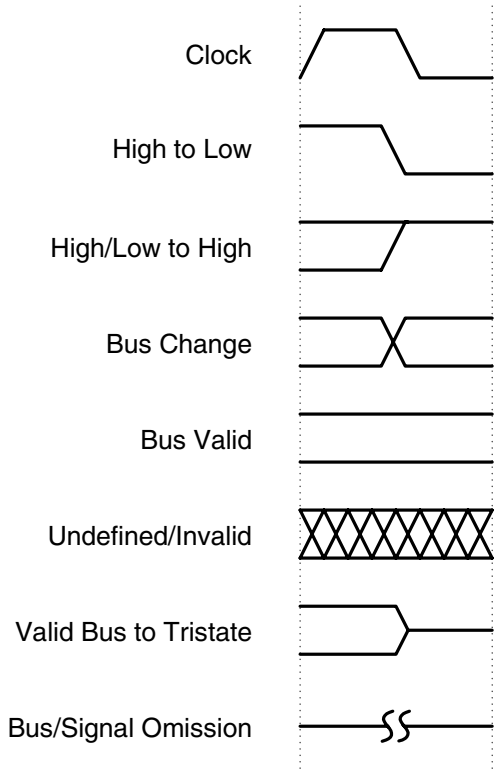

Figure 1. Timing Diagram Drawing Key

Timing Conditions

Unless specified otherwise, the following conditions are true for all timing measurements.

- T_A = 0 to 70° C
- CVDD = VDD_PLL = 1.8V
- RVDD = 3.3 V
- All grounds = 0 V
- Logic 0 = 0 V, Logic 1 = 3.3 V
- Output loading = 50 pF
- Timing reference levels = 1.5 V
- The Processor Bus Clock (HCLK) is programmable and is set by the user. The frequency is typically between 33 MHz and 100 MHz (92 MHz for industrial conditions).

SDRAM Burst Read Cycle

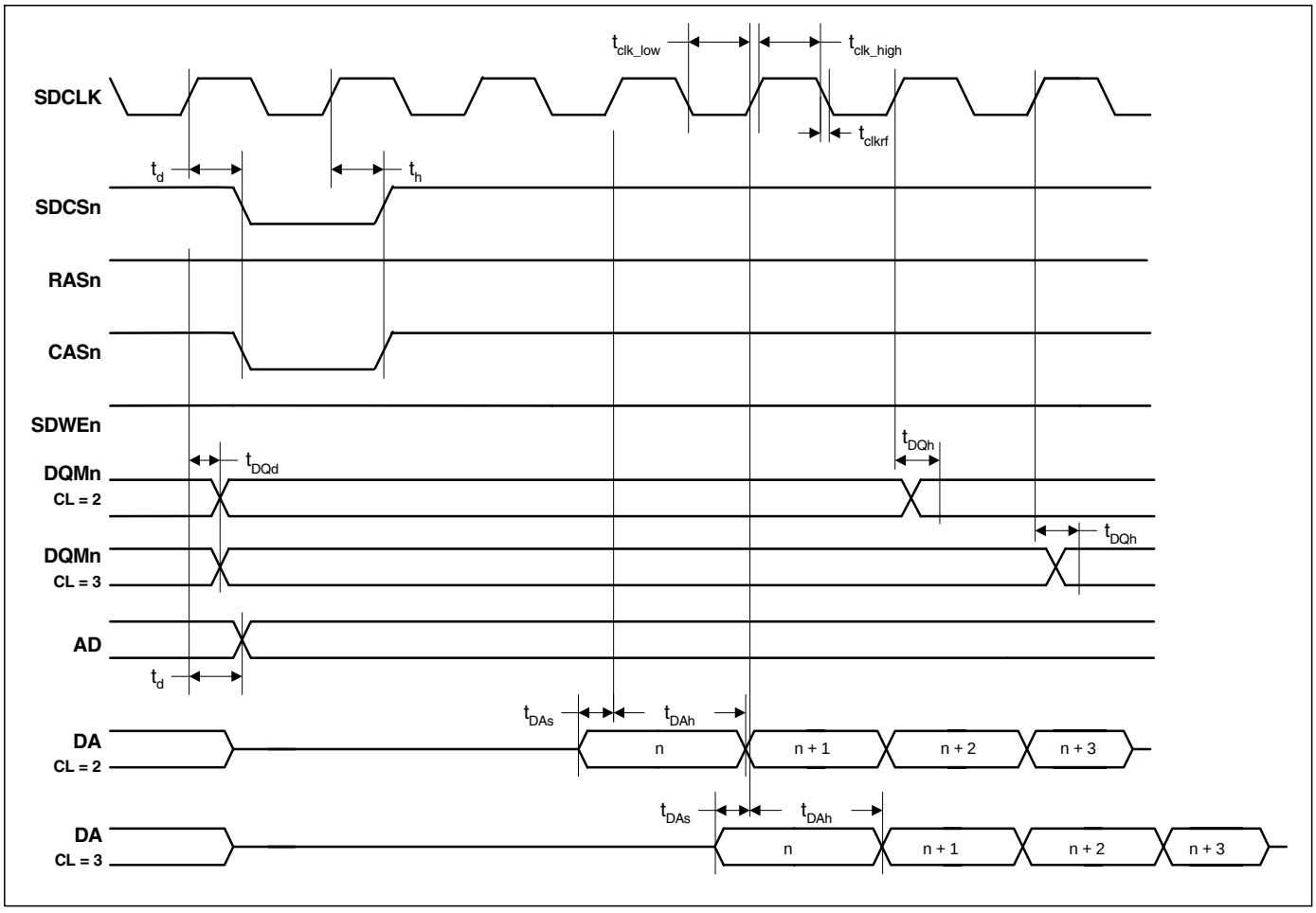

Figure 3. SDRAM Burst Read Cycle Timing Measurement

Static Memory 32-bit Read on 8-bit External Bus

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to CSn assert time	t_{ADs}	t_{HCLK}	-	-	ns
CSn assert to Address transition time	t_{AD1}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
Address assert time	t_{AD2}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
AD transition to CSn deassert time	t_{AD3}	-	$t_{HCLK} \times (WST1 + 2)$	-	ns
AD hold from CSn deassert time	t_{ADh}	t_{HCLK}	-	-	ns
RDn assert time	t_{RDpwL}	-	$t_{HCLK} \times (4 \times WST1 + 5)$	-	ns
CSn to RDn delay time	t_{RDd}	-	-	3	ns
CSn assert to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DA setup to AD transition time	t_{DAs1}	15	-	-	ns
DA setup to RDn deassert time	t_{DAs2}	$t_{HCLK} + 12$	-	-	ns
DA hold from AD transition time	t_{DAh1}	0	-	-	ns
DA hold from RDn deassert time	t_{DAh2}	0	-	-	ns

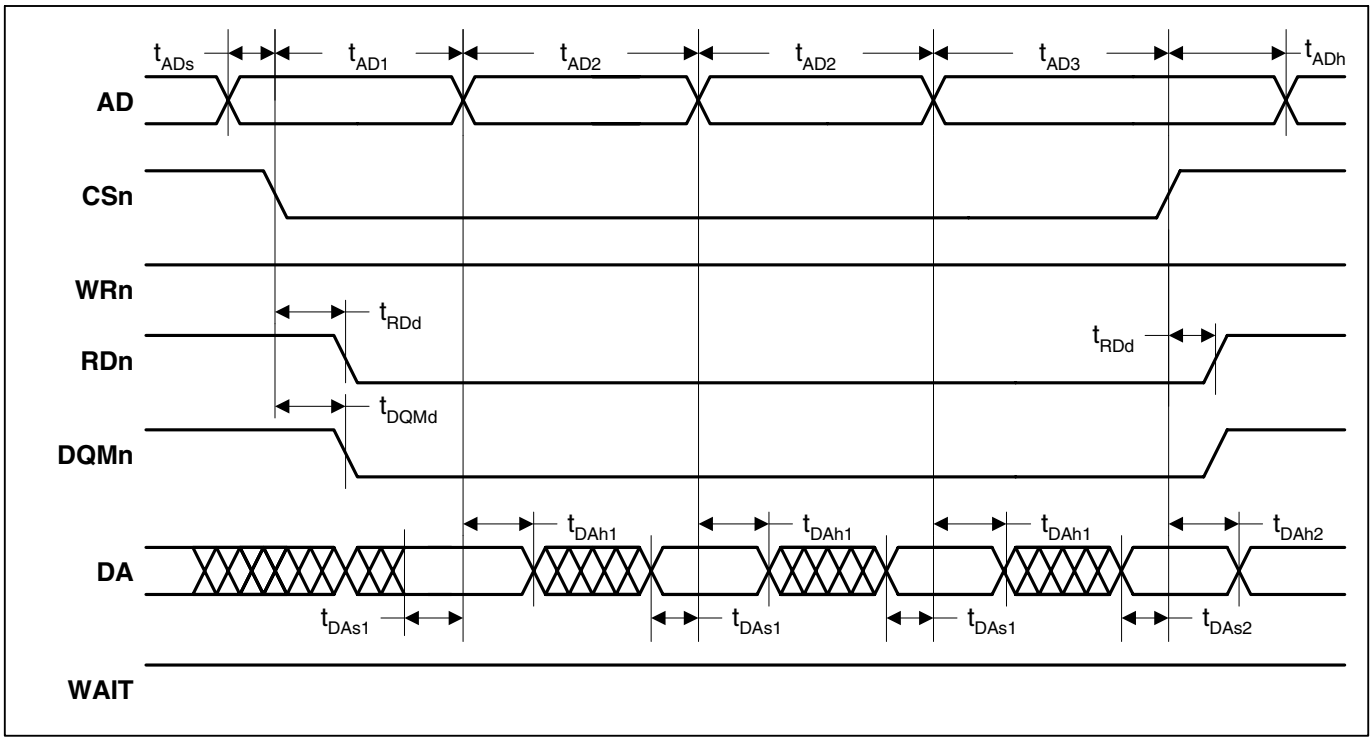

Figure 6. Static Memory Multiple Word Read 8-bit Cycle Timing Measurement

Static Memory 32-bit Write on 8-bit External Bus

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to WRn assert time	t_{ADs}	$t_{HCLK} - 3$	-	-	ns
WRn/DQMn deassert to AD transition time	t_{ADd}	-	-	$t_{HCLK} + 6$	ns
AD hold from WRn deassert time	t_{ADh}	$t_{HCLK} \times 2$	-	-	ns
CSn hold from WRn deassert time	t_{CSh}	7	-	-	ns
CSn to WRn assert delay time	t_{WRd}	-	-	2	ns
WRn assert time	t_{WRpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
WRn deassert time	t_{WRpwH}	-	$t_{HCLK} \times 2$	$(t_{HCLK} \times 2) + 14$	ns
CSn to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DQMn assert time	t_{DQMpwL}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
DQMn deassert time	t_{DQMpwH}	-	-	$(t_{HCLK} \times 2) + 7$	ns
WRn / DQMn deassert to DA transition time	t_{DAh}	t_{HCLK}	-	-	ns
WRn / DQMn assert to DA valid time	t_{DAV}	-	-	8	ns

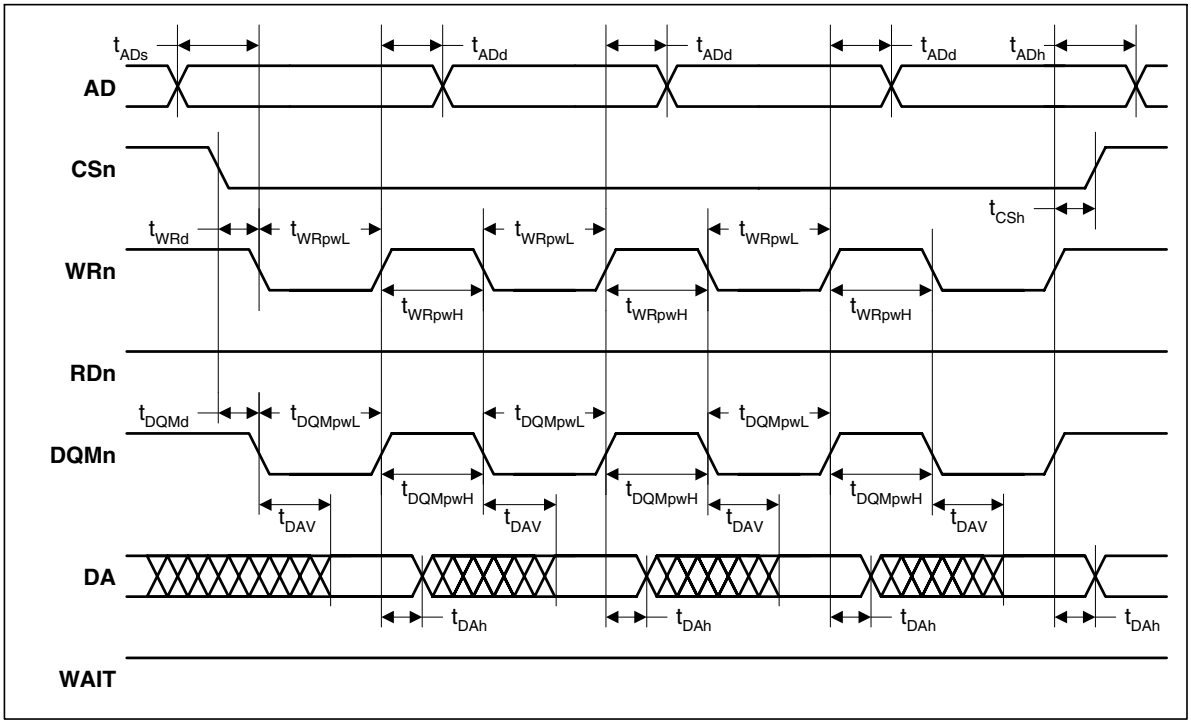

Figure 7. Static Memory Multiple Word Write 8-bit Cycle Timing Measurement

Static Memory Burst Read Cycle

Parameter	Symbol	Min	Typ	Max	Unit
CSn assert to Address 1 transition time	t_{ADd1}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
Address assert time	t_{ADd2}	-	$t_{HCLK} \times (WST2 + 1)$	-	ns
AD transition to CSn deassert time	t_{ADd3}	-	$t_{HCLK} \times (WST1 + 2)$	-	ns
AD hold from CSn deassert time	t_{ADh}	t_{HCLK}	-	-	ns
CSn to RDn delay time	t_{RDd}	-	-	3	ns
CSn to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DA setup to AD transition time	t_{DAs1}	15	-	-	ns
DA setup to CSn deassert time	t_{DAs2}	t_{HCLK} + 12	-	-	ns
DA hold from AD transition time	t_{DAh1}	0	-	-	ns
DA hold from RDn deassert time	t_{DAh2}	0	-	-	ns

Note: These characteristics are valid when the Page Mode Enable (Burst Mode) bit is set. See the User's Guide for details.

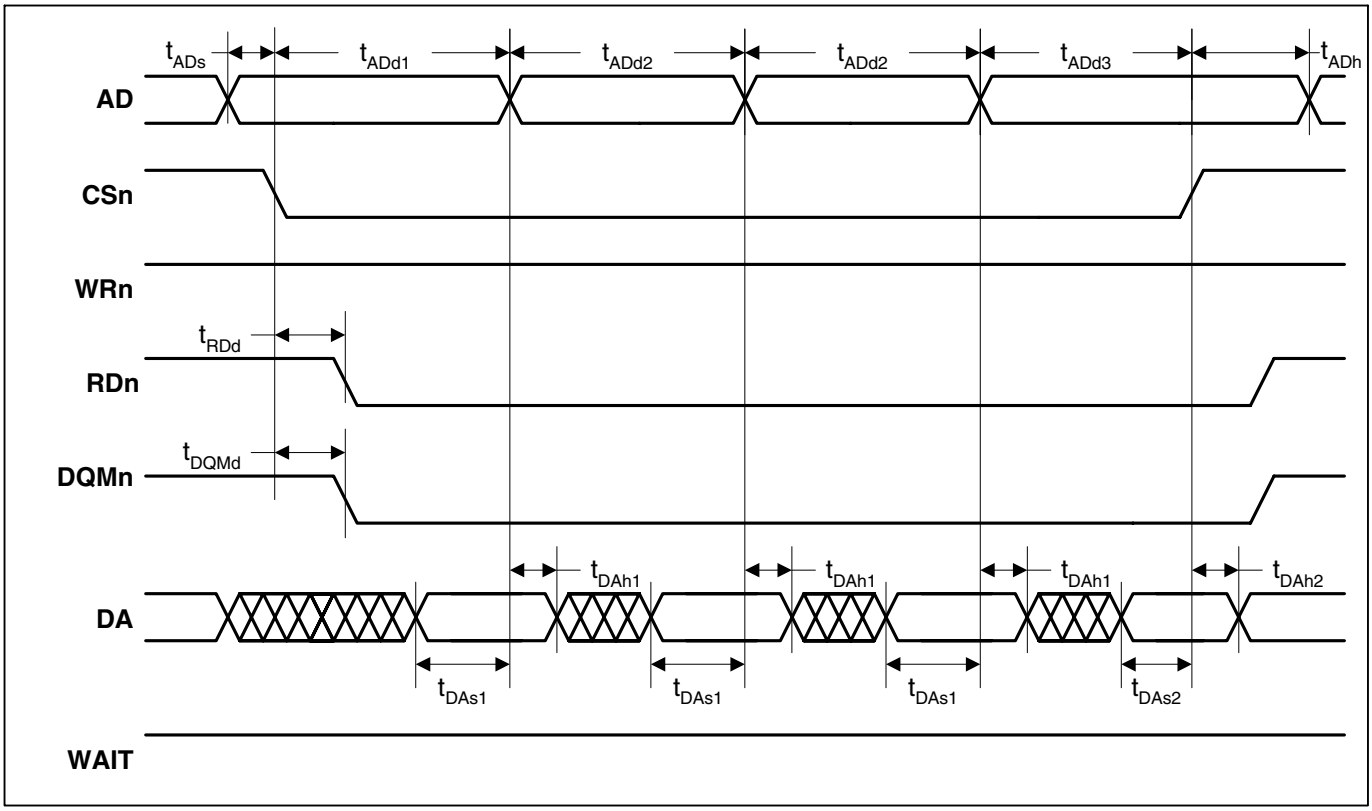

Figure 10. Static Memory Burst Read Cycle Timing Measurement

Static Memory Burst Write Cycle

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to WRn assert time	t_{ADs}	$t_{HCLK} - 3$			ns
AD hold from WRn deassert time	t_{ADh}	$t_{HCLK} \times 2$			ns
WRN/DQMn deassert to AD transition time	t_{ADd}			$t_{HCLK} + 6$	ns
CSn hold from WRn deassert time	t_{CSh}	7			ns
CSn to WRn assert delay time	t_{WRd}			2	ns
CSn to DQMn assert delay time	t_{DQMd}			1	ns
DQMn assert time	t_{DQpwL}		$t_{HCLK} \times (WST1 + 1)$		ns
DQMn deassert time	t_{DQpwH}			$(t_{HCLK} \times 2) + 14$	ns
WRn assert time	t_{WRpwL}		$t_{HCLK} \times (WST1 + 11)$		ns
WRn deassert time	t_{WRpwH}			$(t_{HCLK} \times 2) + 7$	ns
WRn/DQMn deassert to DA transition time	t_{DAh}	t_{HCLK}			ns
WRn/DQMn assert to DA valid time	t_{DAv}			8	ns

Note: These characteristics are valid when the Page Mode Enable (Burst Mode) bit is set. See the User's Guide for details.

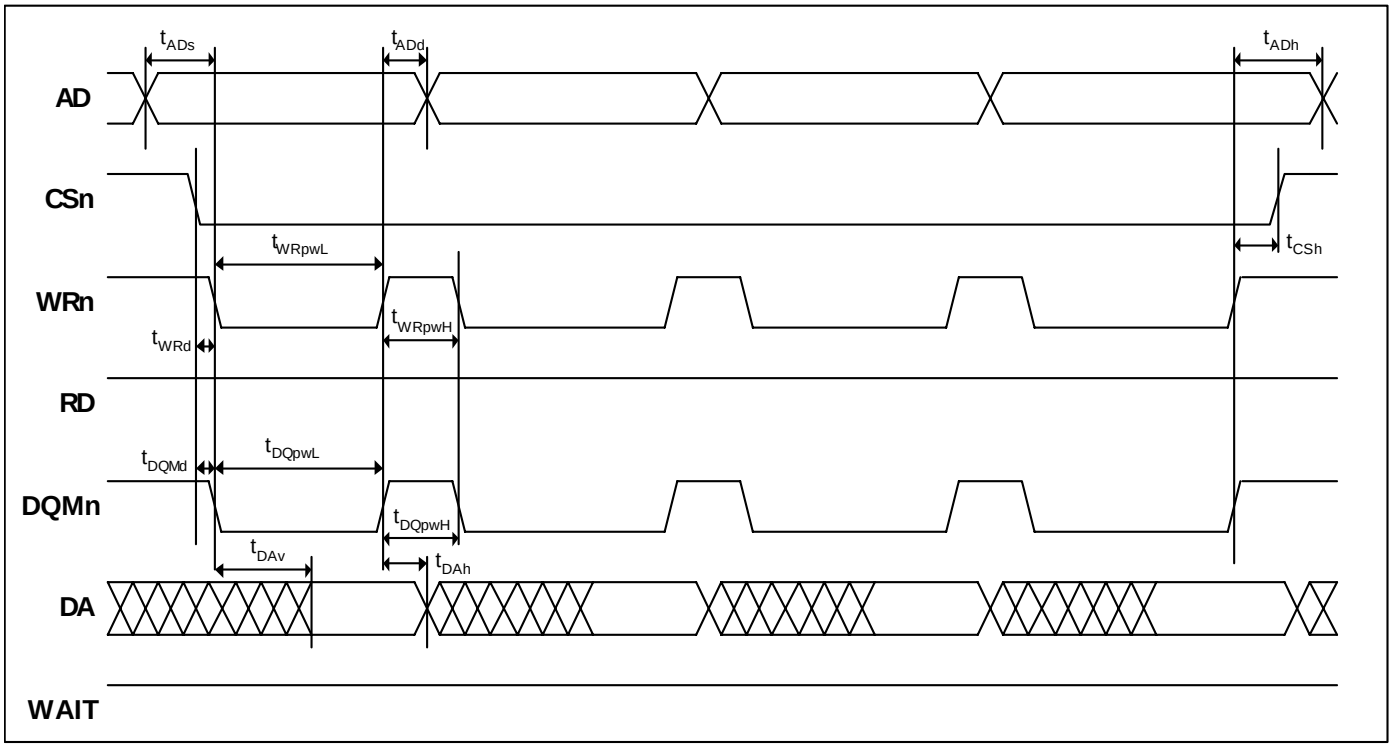

Figure 11. Static Memory Burst Write Cycle Timing Measurement

Static Memory Single Read Wait Cycle

Parameter	Symbol	Min	Typ	Max	Unit
CSn assert to WAIT time	t_{WAITd}	-	-	$t_{HCLK} \times (WST1-2)$	ns
WAIT assert time	t_{WAITpw}	$t_{HCLK} \times 2$	-	$t_{HCLK} \times 510$	ns
WAIT to CSn deassert delay time	t_{CSnd}	$t_{HCLK} \times 3$	-	$t_{HCLK} \times 5$	ns

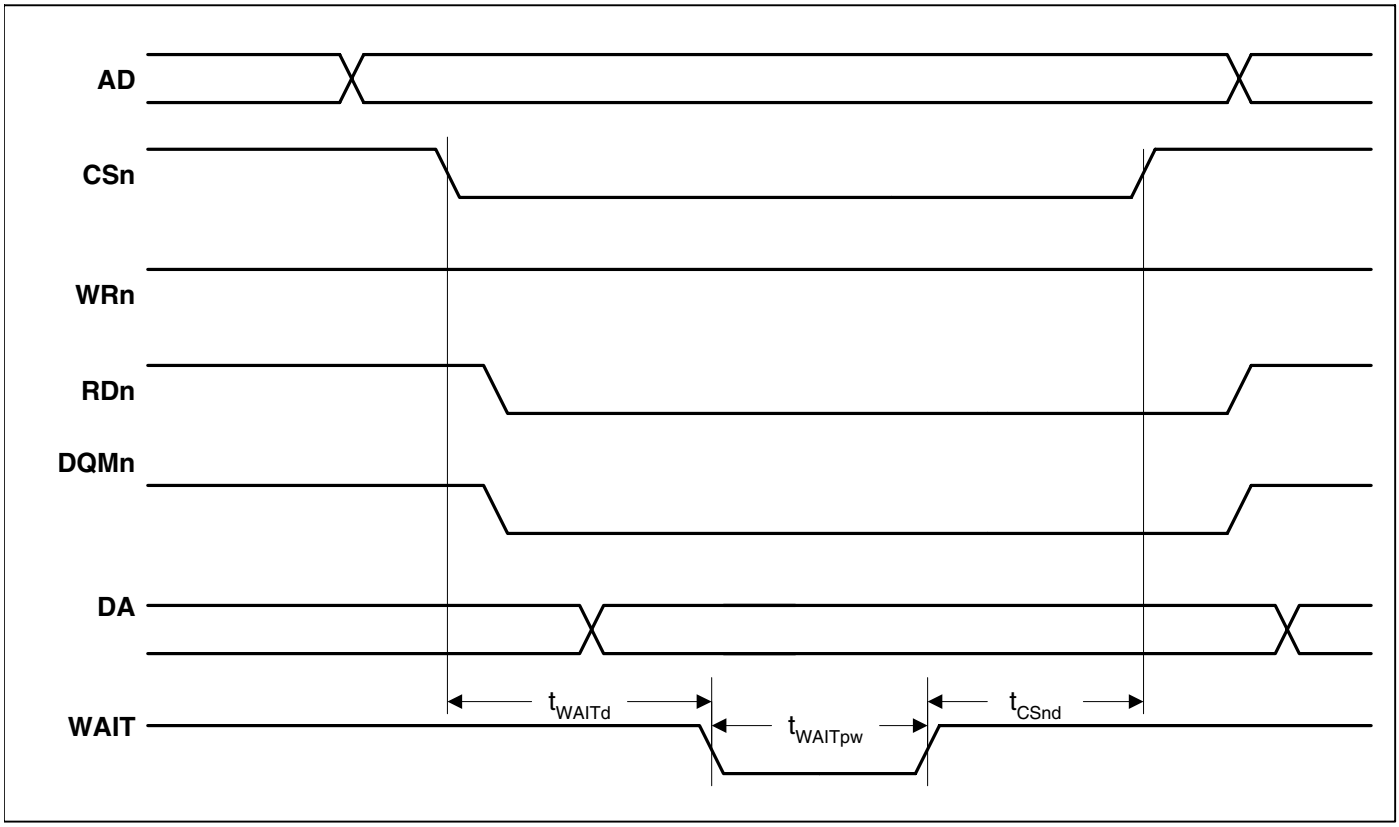

Figure 12. Static Memory Single Read Wait Cycle Timing Measurement

Static Memory Single Write Wait Cycle

Parameter	Symbol	Min	Typ	Max	Unit
WAIT to WRn deassert delay time	t_{WRd}	$t_{HCLK} \times 2$	-	$t_{HCLK} \times 4$	ns
CSn assert to WAIT time	t_{WAITd}	-	-	$t_{HCLK} \times$ (WST1-2)	ns
WAIT assert time	t_{WAITpw}	$t_{HCLK} \times 2$	-	$t_{HCLK} \times 510$	ns
WAIT to CSn deassert delay time	t_{CSnd}	$t_{HCLK} \times 3$	-	$t_{HCLK} \times 5$	ns

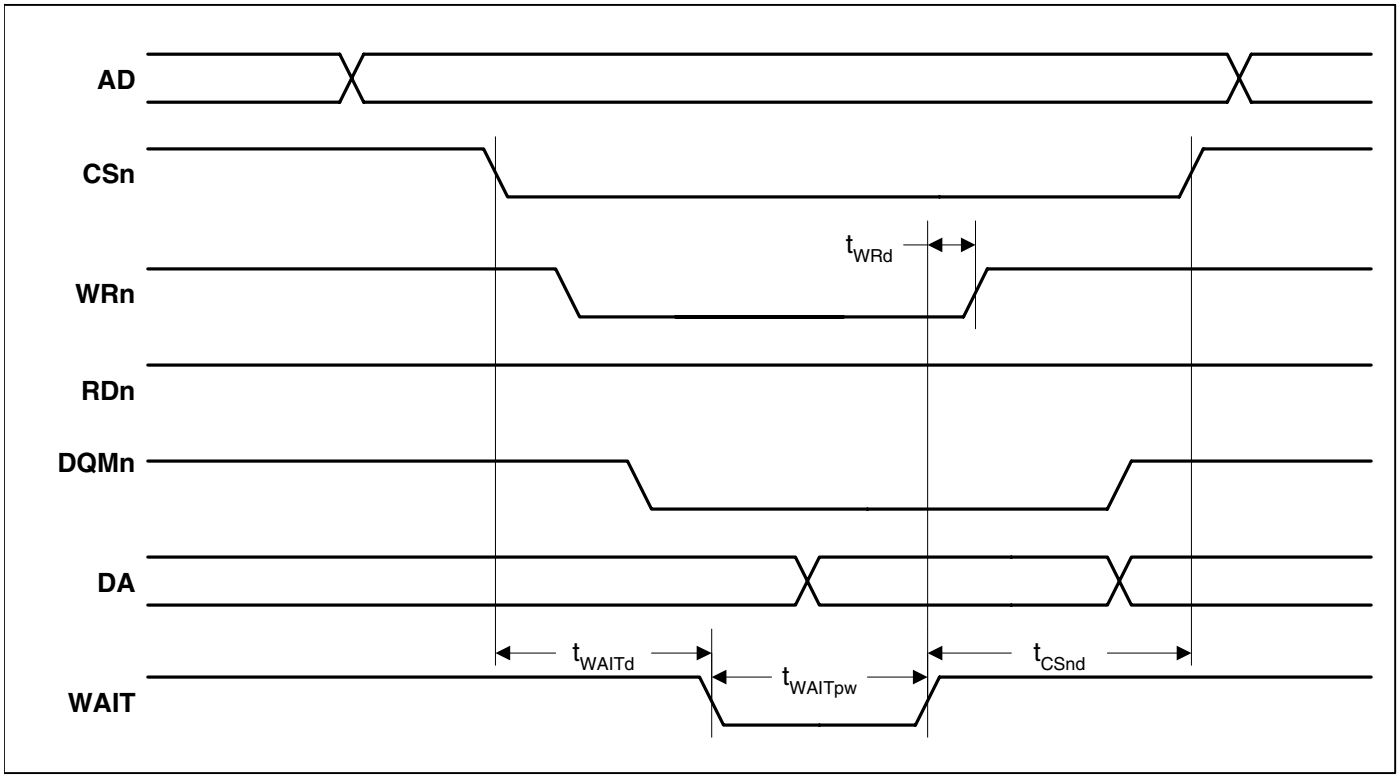

Figure 13. Static Memory Single Write Wait Cycle Timing Measurement

Static Memory Turnaround Cycle

Parameter	Symbol	Min	Typ	Max	Unit
CSnX deassert to CSnY assert time	t_{BTcyc}	-	$t_{HCLK} \times (IDCY+1)$	-	ns

Notes: 1. X and Y represent any two chip select numbers.
2. IDCY occurs on read-to-write and write-to-read.
3. IDCY is honored when going from a asynchronous device (CSx) to a synchronous device (/SDCSy).

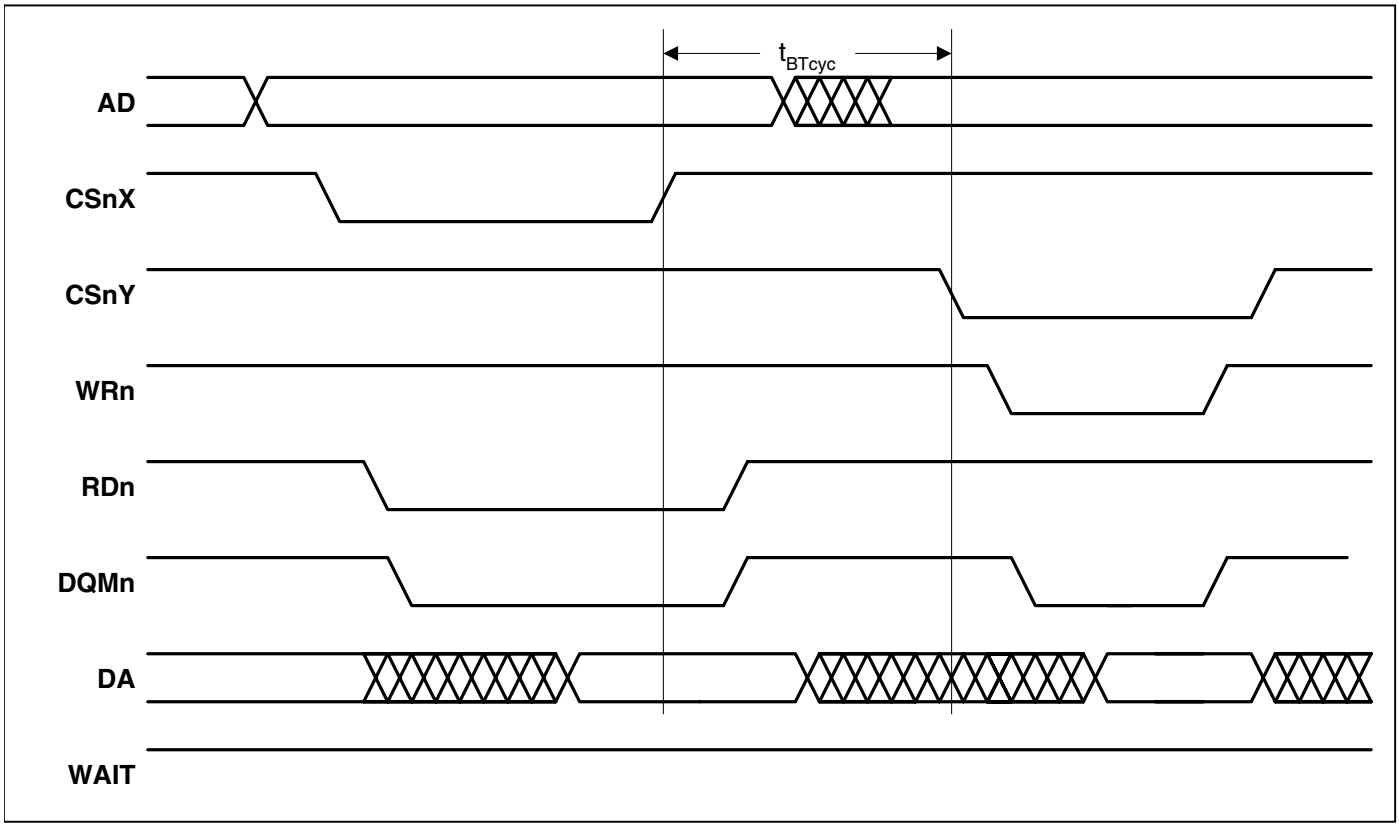

Figure 14. Static Memory Turnaround Cycle Timing Measurement

Ethernet MAC Interface

Parameter	Symbol	Min		Typ		Max		Unit
		10 Mbit mode	100 Mbit mode	10 Mbit mode	100 Mbit mode	10 Mbit mode	100 Mbit mode	
TXCLK cycle time	t_{TX_per}	-	-	400	40	-	-	ns
TXCLK high time	t_{TX_high}	140	14	200	20	260	26	ns
TXCLK low time	t_{TX_low}	140	14	200	20	260	26	ns
TXCLK to signal transition delay time	t_{TXd}	0	0	10	10	25	25	ns
TXCLK rise/fall time	t_{TXrf}	-	-	-	-	5	5	ns
RXCLK cycle time	t_{RX_per}	-	-	400	40	-	-	ns
RXCLK high time	t_{RX_high}	140	14	200	20	260	26	ns
RXCLK low time	t_{RX_low}	140	14	200	20	260	26	ns
RXDVAL / RXERR setup time	t_{RXs}	10	10	-	-	-	-	ns
RXDVAL / RXERR hold time	t_{RXh}	10	10	-	-	-	-	ns
RXCLK rise/fall time	t_{RXrf}	-	-	-	-	5	5	ns
MDC cycle time	t_{MDC_per}	-	-	400	400	-	-	ns
MDC high time	t_{MDC_high}	160	160	-	-	-	-	ns
MDC low time	t_{MDC_low}	160	160	-	-	-	-	ns
MDC rise/fall time	t_{MDCrf}	-	-	-	-	5	5	ns
MDIO setup time (STA sourced)	t_{MDIOs}	10	10	-	-	-	-	ns
MDIO hold time (STA sourced)	t_{MDIOh}	10	10	-	-	-	-	ns
MDC to MDIO signal transition delay time (PHY sourced)	t_{MDIOd}	-	-	-	-	300	300	ns

STA - Station - Any device that contains an IEEE 802.11 conforming Medium Access Control (MAC) and physical layer (PHY) interface to the wireless medium.

PHY - Ethernet physical layer interface.

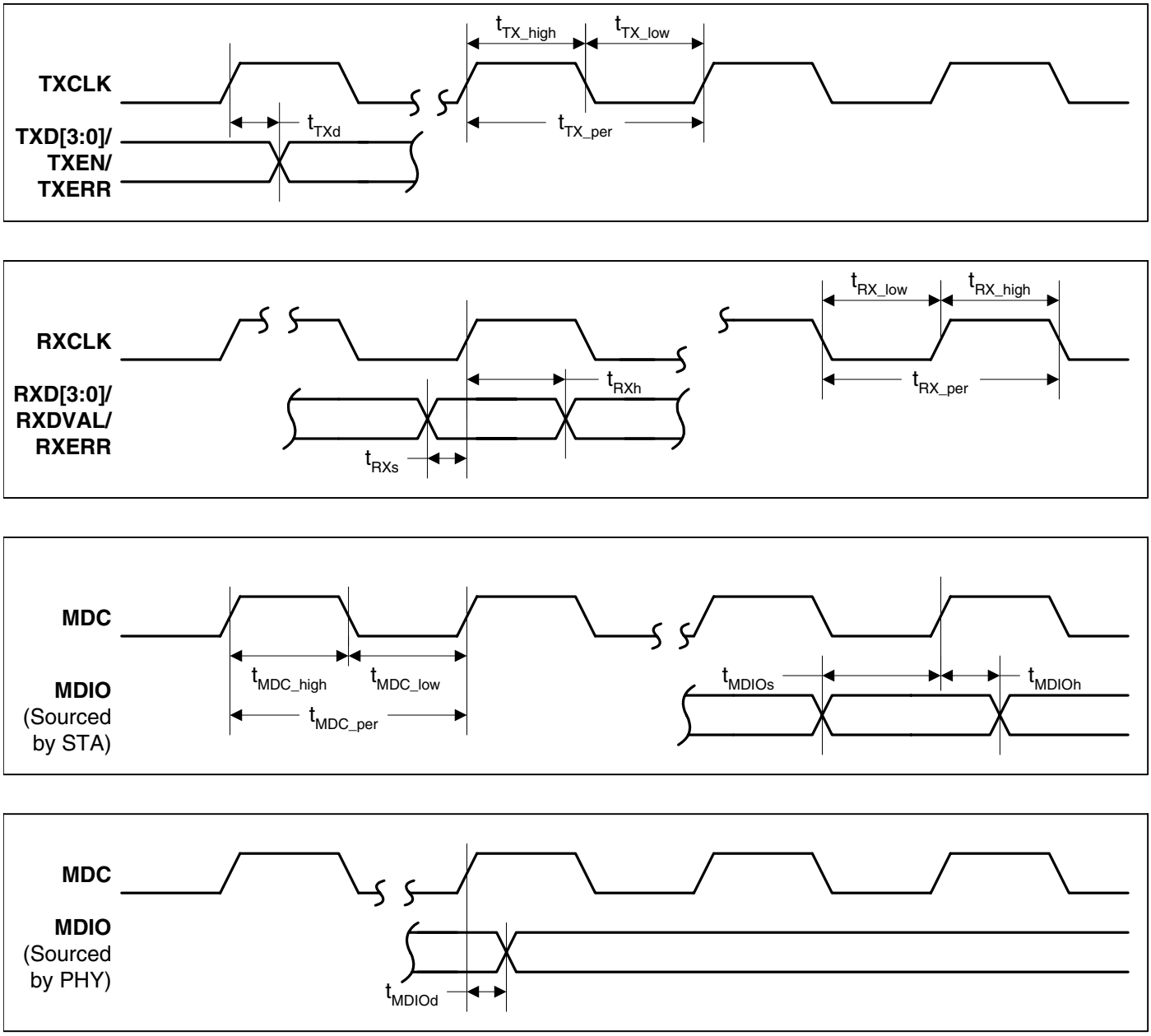

Figure 15. Ethernet MAC Timing Measurement

Audio Interface

The following table contains the values for the timings of each of the SPI modes.

Parameter	Symbol	Min	Typ	Max	Unit
SCLK cycle time	t_{clk_per}	-	tspix_clk	-	ns
SCLK high time	t_{clk_high}	-	(tspix_clk) / 2	-	ns
SCLK low time	t_{clk_low}	-	(tspix_clk) / 2	-	ns
SCLK rise/fall time	t_{clkrf}	1	-	8	ns
Data from master valid delay time	t_{DMd}	-	-	3	ns
Data from master setup time	t_{DMs}	20	-	-	ns
Data from master hold time	t_{DMh}	40	-	-	ns
Data from slave setup time	t_{DSs}	20	-	-	ns
Data from slave hold time	t_{DSh}	40	-	-	ns

Note: The tspix_clk is programmable by the user.

Texas Instruments' Synchronous Serial Format

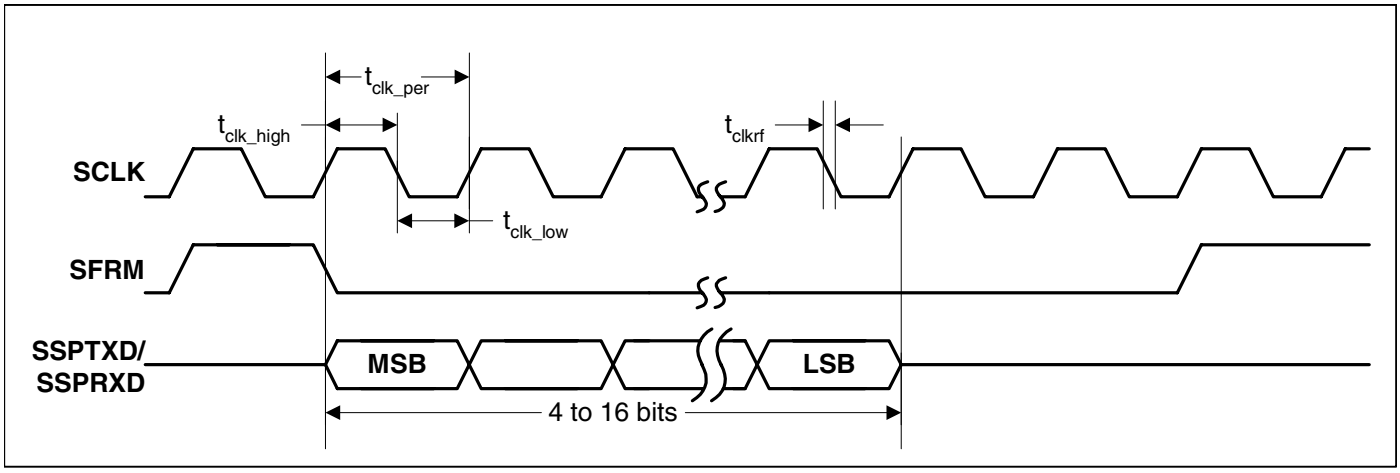

Figure 16. *TI* Single Transfer Timing Measurement

Microwire

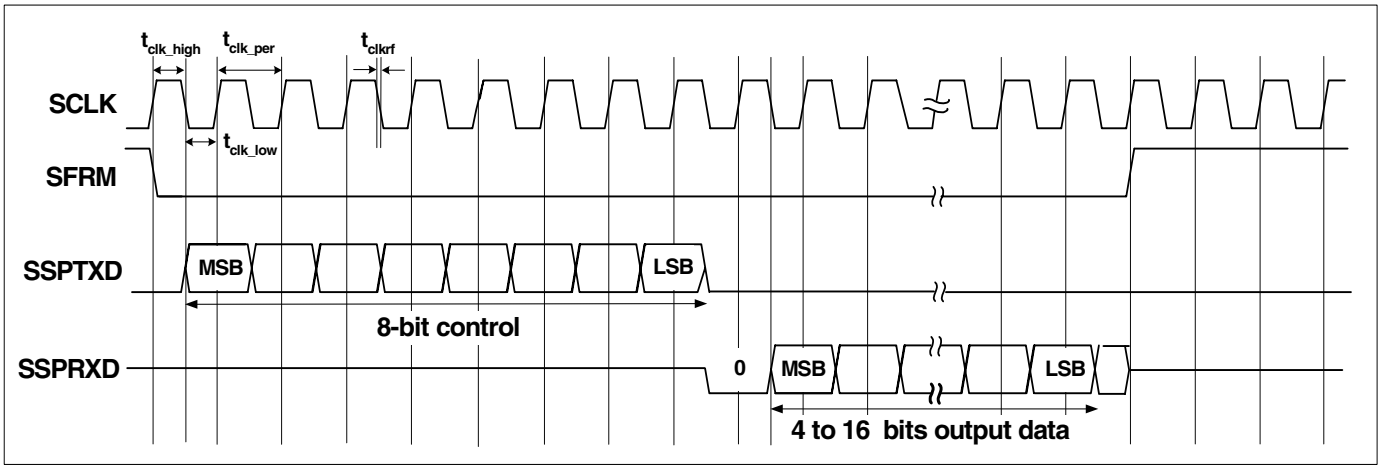

Figure 17. Microwire Frame Format, Single Transfer

Inter-IC Sound - I²S

Parameter	Symbol	Min	Typ	Max	Unit
SCLK cycle time	t_{clk_per}	-	t_{i2s_clk}	-	ns
SCLK high time	t_{clk_high}	-	$(t_{i2s\_clk}) / 2$	-	ns
SCLK low time	t_{clk_low}	-	$(t_{i2s\_clk}) / 2$	-	ns
SCLK rise/fall time	t_{clkrf}	1	4	8	ns
SCLK to LRCLK assert delay time	t_{LRd}	-	-	3	ns
Hold between SCLK assert then LRCLK deassert *or* Hold between LRCLK deassert then SCLK assert	t_{LRh}	0	-	-	ns
SDI to SCLK deassert setup time	t_{SDIs}	12	-	-	ns
SDI from SCLK deassert hold time	t_{SDIh}	0	-	-	ns
SCLK assert to SDO delay time	t_{SDOd}	-	-	9	ns
SDO from SCLK assert hold time	t_{SDOh}	1	-	-	ns

Note: t_{i2s_clk} is programmable by the user.

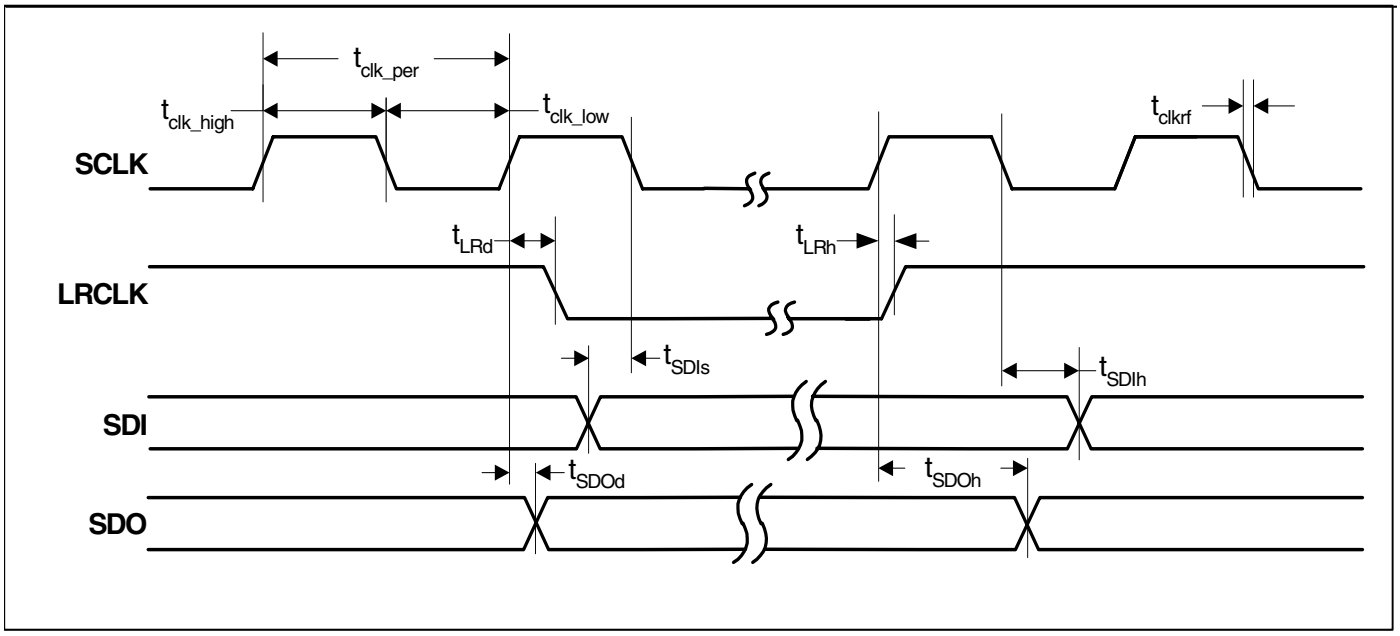

Figure 19. Inter-IC Sound (I^2S) Timing Measurement

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Table Q. Pin Description

Pin Name	Block	Pad Type	Pull Type	Description
TCK	JTAG	I	PD	JTAG clock in
TDI	JTAG	I	PD	JTAG data in
TDO	JTAG	4ma		JTAG data out
TMS	JTAG	I	PD	JTAG test mode select
TRSTn	JTAG	I	PD	JTAG reset
BOOT[1:0]	System	I	PD	Boot mode select in
XTALI	PLL	A		Main oscillator input
XTALO	PLL	A		Main oscillator output
VDD_PLL	PLL	P		Main oscillator power, 1.8V
GND_PLL	PLL	G		Main oscillator ground
RTCXTALI	RTC	A		RTC oscillator input
RTCXTALO	RTC	A		RTC oscillator output
WRn	EBUS	4ma		SRAM Write strobe out
RDn	EBUS	4ma		SRAM Read / OE strobe out
WAITn	EBUS	I	PU	SRAM Wait in
AD[25:0]	EBUS	8ma		Shared Address bus out
DA[15:0]	EBUS	8ma	PU	Shared Data bus in/out
CSn[3:0]	EBUS	4ma	PU	Chip select out
CSn[7:6]	EBUS	4ma	PU	Chip select out
DQMn[1:0]	EBUS	8ma		Shared data mask out
SDCLK	SDRAM	8ma		SDRAM clock out
SDCLKEN	SDRAM	8ma		SDRAM clock enable out
SDCSn[3:0]	SDRAM	4ma		SDRAM chip selects out
RASn	SDRAM	8ma		SDRAM RAS out
CASn	SDRAM	8ma		SDRAM CAS out
SDWEn	SDRAM	8ma		SDRAM write enable out
ADC[4:0]	ADC	A		External Analog Measurement Input
VDD_ADC	ADC	P		ADC power, 3.3V
GND_ADC	ADC	G		ADC ground
USBp[2, 0]	USB	A		USB positive signals
USBm[2, 0]	USB	A		USB negative signals
TXD0	UART1	4ma		Transmit out
RXD0	UART1	I	PU	Receive in
CTSn	UART1	I	PU	Clear to send / transmit enable
DSRn	UART1	I	PU	Data set ready / Data Carrier Detect
DTRn	UART1	4ma		Data Terminal Ready output
RTSn	UART1	4ma		Ready to send
TXD1	UART2	4ma		Transmit / IrDA output
RXD1	UART2	I	PU	Receive / IrDA input
MDC	EMAC	4ma		Management data clock
MDIO	EMAC	4ma	PU	Management data input/output
RXCLK	EMAC	I	PD	Receive clock in
MIIRXD[3:0]	EMAC	I	PD	Receive data in
RXDVAL	EMAC	I	PD	Receive data valid
RXERR	EMAC	I	PD	Receive data error
TXCLK	EMAC	I	PU	Transmit clock in
MIITXD[3:0]	EMAC	4ma	PD	Transmit data out

Table Q. Pin Description (Continued)

Pin Name	Block	Pad Type	Pull Type	Description
TXEN	EMAC	4ma	PD	Transmit enable
TXERR	EMAC	4ma	PD	Transmit error
CRS	EMAC	I	PD	Carrier sense
CLD	EMAC	I	PU	Collision detect
GRLED	LED	12ma		Green LED
RDLED	LED	12ma		Red LED
EECLK	EEPROM	4ma	PU	EEPROM / Two-wire Interface clock
EEDAT	EEPROM	4ma	PU	EEPROM / Two-wire Interface data
ABITCLK	AC97	8ma	PD	AC97 bit clock
ASYNC	AC97	8ma	PD	AC97 frame sync
ASDI	AC97	I	PD	AC97 Primary input
ASDO	AC97	8ma	PU	AC97 output
ARSTn	AC97	8ma		AC97 reset
SCLK1	SPI1	I/O, 8ma	PD	SPI bit clock
SFRM1	SPI1	I/O, 8ma	PD	SPI Frame Clock
SSPRX1	SPI1	I	PD	SPI input
SSPTX1	SPI1	8ma		SPI output
INT[3], INT[1:0]	INT	I	PD	External interrupts
PRSTn	Syscon	I	PU	Power on reset
RSTOn	Syscon	4ma		User Reset in out - open drain
EGPIO[15:0]	GPIO	I/O, 4ma	PU	Enhanced GPIO
FGPIO[3:1]	GPIO	I/O, 8ma	PU	GPIO on Port F
HGPIO[5:2]	GPIO	I/O, 8ma	PU	GPIO on Port H
CGPIO[0]	GPIO	I/O, 8ma	PU	GPIO on Port C
CVDD	Power	P		Digital power, 1.8V
RVDD	Power	P		Digital power, 3.3V
CGND	Ground	G		Digital ground
RGND	Ground	G		Digital ground

Acronyms and Abbreviations

The following tables list abbreviations and acronyms used in this data sheet.

Term	Definition
ADC	Analog-to-Digital Converter
ALT	Alternative
AMBA	Advanced Micro-controller Bus Architecture
ATAPI	ATA Packet Interface
CODEC	COder / DECoder
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
DMA	Direct-Memory Access
EEPROM	Electronically Erasable Programmable Read Only Memory
EMAC	Ethernet Media Access Controller
EBUS	External Memory Bus
FIFO	First In / First Out
FIQ	Fast Interrupt Request
FLASH	Flash memory
GPIO	General Purpose I/O
HDLC	High-level Data Link Control
I/F	Interface
I^2S	Inter-IC Sound
IC	Integrated Circuit
ICE	In-Circuit Emulator
IDE	Integrated Drive Electronics
IEEE	Institute of Electronics and Electrical Engineers
IrDA	Infrared Data Association
IRQ	Standard Interrupt Request
ISO	International Standards Organization
JTAG	Joint Test Action Group
LFSR	Linear Feedback Shift Register
MII	Media Independent Interface
MMU	Memory Management Unit
OHCI	Open Host Controller Interface
PHY	Ethernet PHYsical layer interface
PIO	Programmed I/O
RISC	Reduced Instruction Set Computer
SDMI	Secure Digital Music Initiative
SDRAM	Synchronous Dynamic RAM
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
STA	Station - Any device that contains an IEEE 802.11 conforming Medium Access Control (MAC) and physical layer (PHY) interface to the wireless medium
TFT	Thin Film Transistor
TLB	Translation Lookaside Buffer
USB	Universal Serial Bus

Units of Measurement

Symbol	Unit of Measure
^{o}C	degree Celsius
Hz	Hertz = cycle per second
kbps	Kilobits per second
kbyte	Kilobyte
KHz	KiloHertz = 1000 Hz
Mbps	Megabits per second
MHz	MegaHertz = 1,000 KiloHertz
µA	microAmpere = 10^{-6} Ampere
µs	microsecond = 1,000 nanoseconds = 10^{-6} seconds
mA	milliAmpere = 10^{-3} Ampere
ms	millisecond = 1,000 microseconds = 10^{-3} seconds
mW	milliWatt = 10^{-3} Watts
ns	nanosecond = 10^{-9} seconds
pF	picoFarad = 10^{-12} Farads
V	Volt
W	Watt