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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	166MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	1/10/100Mbps (1)
SATA	-
USB	USB 2.0 (2)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Hardware ID
Package / Case	208-LQFP
Supplier Device Package	208-LQFP
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep9301-iq

OVERVIEW

The EP9301 is an ARM920T-based system-on-a-chip design with a large peripheral set targeted to a variety of applications:

- Industrial controls
- Digital media servers
- Integrated home media gateways
- Digital audio jukeboxes
- Streaming audio players
- Set-top boxes
- Point-of-sale terminals
- Thin clients
- Biometric security systems
- GPS & fleet management systems
- Educational toys
- Industrial computers
- Industrial hand-held devices
- Voting machines
- Medical equipment

The EP9301 is one of a series of ARM920T-based devices. Other members of the family have different peripheral sets, a coprocessor, and different package configurations.

The ARM920T microprocessor core has a separate 16-kbyte, 64-way set-associative instruction and data caches.

The MaverickKey™ unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

A high-performance 1/10/100 Mbps Ethernet media access controller (EMAC) is included along with external interfaces to SPI, AC'97 and I^2S audio. A two-port USB 2.0 Full-speed Host (OHCI) (12 Mbits per second), two UARTs, and a analog voltage measurement analog-to-digital converter (ADC) are included as well.

The EP9301 is a high-performance, low-power RISC-based, single-chip computer built around an ARM920T microprocessor core with a maximum operating clock rate of 166 MHz. The ARM core operates from a 1.8 V supply, while the I/O operates at 3.3 V with power usage between 100 mW and 675 mW.

Table A. Change History

Revision	Date	Changes
1	October 2003	Initial Release.
2	February 2004	Update timing specifications.
3	July 2004	Update AC data.
4	July 2004	Add ADC data.
5	March 2005	Update with most-current characterization data.

List of Tables

Universal Asynchronous Receiver/Transmitters (UARTs)

Two 16550-compatible UARTs are supplied. One provides asynchronous HDLC (High-level Data Link Control) protocol support for full duplex transmit and receive. The HDLC receiver handles framing, address matching, CRC checking, control-octet transparency, and optionally passes the CRC to the host at the end of the packet. The HDLC transmitter handles framing, CRC generation, and control-octet transparency. The host must assemble the frame in memory before transmission. The HDLC receiver and transmitter use the UART FIFOs to buffer the data streams. The second UART provides IrDA® compatibility.

- UART1 supports modem bit rates up to 115.2 kbps, supports HDLC and includes a 16 byte FIFO for receive and a 16 byte FIFO for transmit. Interrupts are generated on Rx, Tx and modem status change.
- UART2 contains an IrDA encoder operating at either the slow (up to 115 kbps), medium (0.576 or 1.152 Mbps), or fast (4 Mbps) IR data rates. It also has a 16 byte FIFO for receive and a 16 byte FIFO for transmit.

Table F. Universal Asynchronous Receiver/Transmitters Pin Assignments

Pin Mnemonic	Pin Name - Description
TXD0	UART1 Transmit
RXD0	UART1 Receive
CTSn	UART1 Clear To Send / Transmit Enable
DSRn / DCDn	UART1 Data Set Ready / Data Carrier Detect
DTRn	UART1 Data Terminal Ready
RTSn	UART1 Ready To Send
EGPIO[0] / RI	UART1 Ring Indicator
TXD1 / SIROUT	UART2 Transmit / IrDA Output
RXD1 / SIRIN	UART2 Receive / IrDA Input

Dual Port USB Host

The USB Open Host Controller Interface (Open HCI) provides full speed serial communications ports at a baud rate of 12 Mbits/sec. Up to 127 USB devices (printer, mouse, camera, keyboard, etc.) and USB hubs can be connected to the USB host in the USB “tiered-start” topology.

This includes the following feature:

- Compliance with the USB 2.0 specification
- Compliance with the Open HCI Rev 1.0 specification
- Supports both low speed (1.5 Mbps) and full speed (12 Mbps) USB device connections
- Root HUB integrated with 2 downstream USB ports
- Transceiver buffers integrated, over-current protection on ports
- Supports power management
- Operates as a master on the bus

The Open HCI host controller initializes the master DMA transfer with the AHB bus:

- Fetches endpoint descriptors and transfer descriptors
- Accesses endpoint data from system memory
- Accesses the HC communication area
- Writes status and retire transfer descriptor

Table G. Dual Port USB Host Pin Assignments

Pin Mnemonic	Pin Name - Description
USBp[2,0]	USB Positive signals
USBm[2,0]	USB Negative Signals

Note: USBm[1] and USBp[1] are not bonded out.

Two-Wire Interface With EEPROM Support

The two-wire interface provides communication and control for synchronous-serial-driven devices.

Table H. Two-Wire Port with EEPROM Support Pin Assignments

Pin Mnemonic	Pin Name - Description	Alternative Usage
EECLK	Two-wire Interface Clock	General Purpose I/O
EEDATA	Two-wire Interface Data	General Purpose I/O

Real-Time Clock with Software Trim

The software trim feature on the real time clock (RTC) provides software controlled digital compensation of the 32.768 KHz input clock. This compensation is accurate to ± 1.24 sec/month.

Note: A real time clock must be connected to RTCXTALI or the EP9301device will not boot.

Table I. Real-Time Clock with Pin Assignments

Pin Mnemonic	Pin Name - Description
RTCXTALI	Real-Time Clock Oscillator Input
RTCXTALO	Real-Time Clock Oscillator Output

Reset and Power Management

The chip may be reset through the PRSTn pin or through the open drain common reset pin, RSTOn.

Clocks are managed on a peripheral-by-peripheral basis and may be turned off to conserve power.

The processor clock is dynamically adjustable from 0 to 166 MHz.

Table N. Reset and Power Management Pin Assignments

Pin Mnemonic	Pin Name - Description
PRSTn	Power On Reset
RSTOn	User Reset In/Out – Open Drain – Preserves Real Time Clock value

Hardware Debug Interface

The JTAG interface allows use of ARM's Multi-ICE or other in-circuit emulators.

Table O. Hardware Debug Interface

Pin Mnemonic	Pin Name - Description
TCK	JTAG Clock
TDI	JTAG Data In
TDO	JTAG Data Out
TMS	JTAG Test Mode Select
TRSTn	JTAG Port Reset

12-channel DMA Controller

The DMA module contains 12 separate DMA channels. Ten of these may be used for peripheral-to-memory or memory-to-peripheral access. Two of these are dedicated to memory-to-memory transfers. Each DMA channel is connected to the 16-bit DMA request bus.

The request bus is a collection of requests, Serial Audio and UARTs. Each DMA channel can be used independently or dedicated to any request signal. For each DMA channel, source and destination addressing can be independently programmed to increment, decrement, or stay at the same value. All DMA addresses are physical, not virtual addresses.

Internal Boot ROM

The Internal 16 kbyte ROM allows booting from FLASH memory, SPI or UART. Consult the EP93xx User's Manual for operational details.

Electrical Specifications

Absolute Maximum Ratings

(All grounds = 0 V, all voltages with respect to 0 V)

Parameter		Symbol	Min	Max	Unit
Power Supplies		RVDD CVDD VDD_PLL VDD_ADC	- - - -	3.96 2.16 2.16 3.96	V V V V
Total Power Dissipation	(Note 1)		-	2	W
Input Current per Pin, DC (Except supply pins)			-	±10	mA
Output current per pin, DC			-	±50	mA
Digital Input voltage	(Note 2)		-0.3	RVDD+0.3	V
Storage temperature			-40	+125	°C

Note: 1. Includes all power generated by AC and/or DC output loading.
2. The power supply pins are at recommended maximum values.
3. At ambient temperatures above 70° C, total power dissipation must be limited to less than 2.5 Watts.

WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Recommended Operating Conditions

(All grounds = 0 V, all voltages with respect to 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supplies	RVDD CVDD VDD_PLL VDD_ADC	3.0 1.65 1.65 3.0	3.3 1.80 1.80 3.3	3.6 1.94 1.94 3.6	V V V V
Operating Ambient Temperature - Commercial	T_A	0	+25	+70	°C
Operating Ambient Temperature - Industrial	T_A	-40	+25	+85	°C
Processor Clock Speed - Commercial	FCLK	-	-	166	MHz
Processor Clock Speed - Industrial	FCLK	-	-	166	MHz
System Clock Speed - Commercial	HCLK	-	-	66	MHz
System Clock Speed - Industrial	HCLK	-	-	66	MHz

Memory Interface

Figure 2 through Figure 5 define the timings associated with all phases of the SDRAM. The following table contains the values for the timings of each of the SDRAM modes.

Parameter	Symbol	Min	Typ	Max	Unit
SDCLK high time	t_{clk_high}	-	$(t_{HCLK}) / 2$	-	ns
SDCLK low time	t_{clk_low}	-	$(t_{HCLK}) / 2$	-	ns
SDCLK rise/fall time	t_{clkrf}	-	2	4	ns
Signal delay from SDCLK rising edge time	t_d	-	-	8	ns
Signal hold from SDCLK rising edge time	t_h	1	-	-	ns
DQMn delay from SDCLK rising edge time	t_{DQd}	-	-	8	ns
DQMn hold from SDCLK rising edge time	t_{DQh}	1	-	-	ns
DA valid setup to SDCLK rising edge time	t_{DAs}	2	-	-	ns
DA valid hold from SDCLK rising edge time	t_{DAh}	3	-	-	ns

SDRAM Load Mode Register Cycle

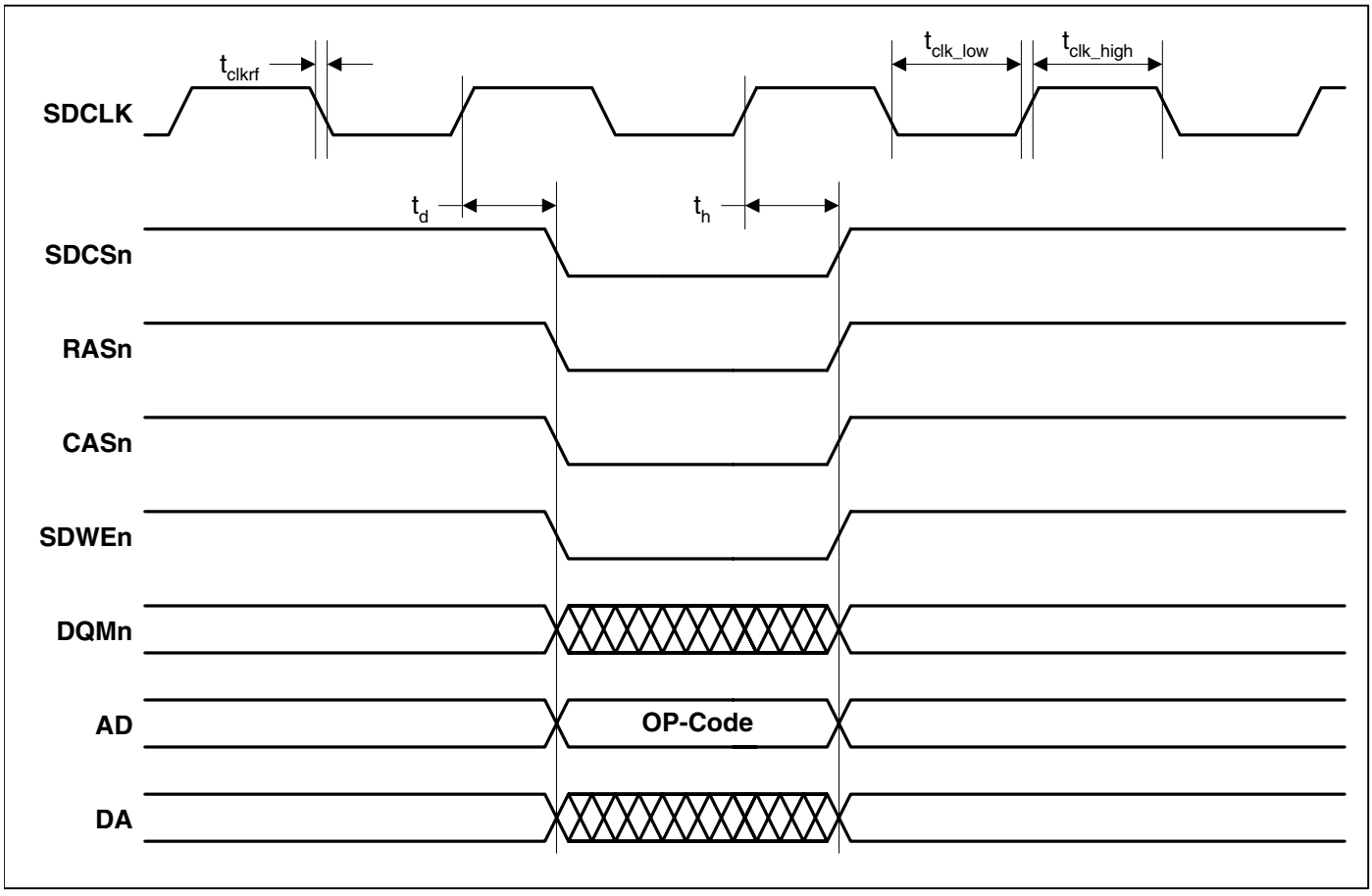
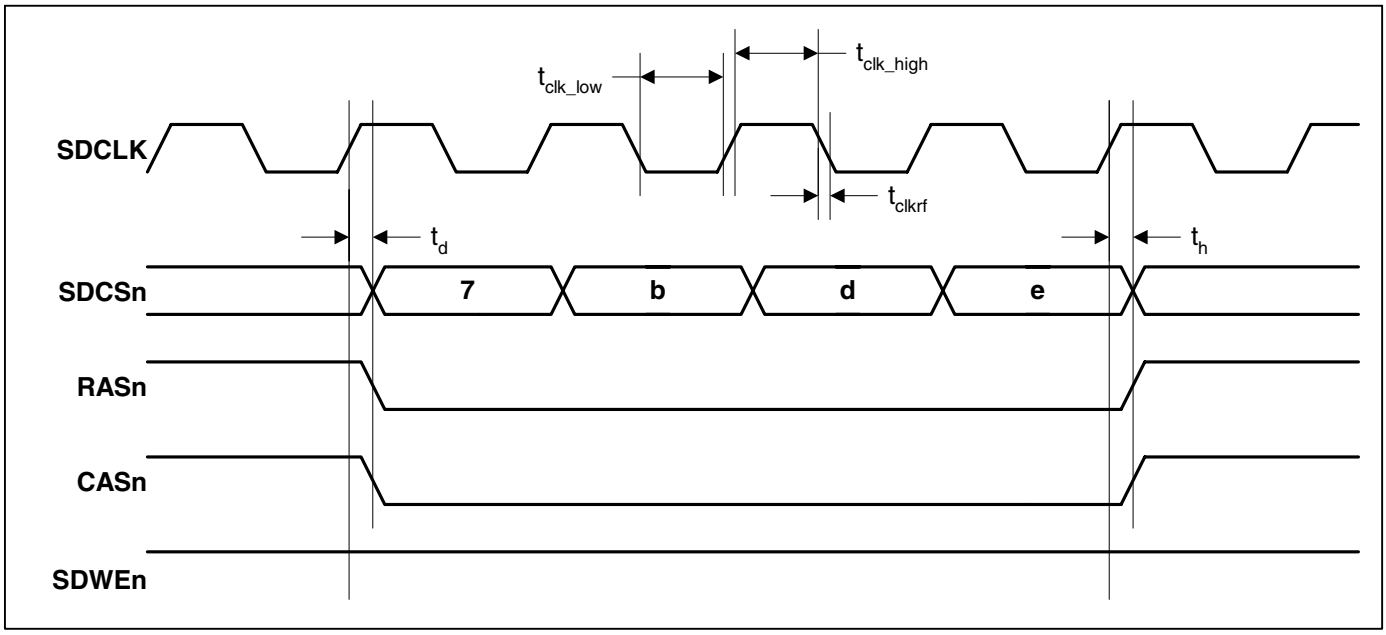


Figure 2. SDRAM Load Mode Register Cycle Timing Measurement

SDRAM Auto Refresh Cycle



Note: Chip select shown as bus to illustrate multiple devices being put into auto refresh in one access

Figure 5. SDRAM Auto Refresh Cycle Timing Measurement

Static Memory Burst Read Cycle

Parameter	Symbol	Min	Typ	Max	Unit
CSn assert to Address 1 transition time	t_{ADd1}	-	$t_{HCLK} \times (WST1 + 1)$	-	ns
Address assert time	t_{ADd2}	-	$t_{HCLK} \times (WST2 + 1)$	-	ns
AD transition to CSn deassert time	t_{ADd3}	-	$t_{HCLK} \times (WST1 + 2)$	-	ns
AD hold from CSn deassert time	t_{ADh}	t_{HCLK}	-	-	ns
CSn to RDn delay time	t_{RDd}	-	-	3	ns
CSn to DQMn assert delay time	t_{DQMd}	-	-	1	ns
DA setup to AD transition time	t_{DAs1}	15	-	-	ns
DA setup to CSn deassert time	t_{DAs2}	t_{HCLK} + 12	-	-	ns
DA hold from AD transition time	t_{DAh1}	0	-	-	ns
DA hold from RDn deassert time	t_{DAh2}	0	-	-	ns

Note: These characteristics are valid when the Page Mode Enable (Burst Mode) bit is set. See the User's Guide for details.

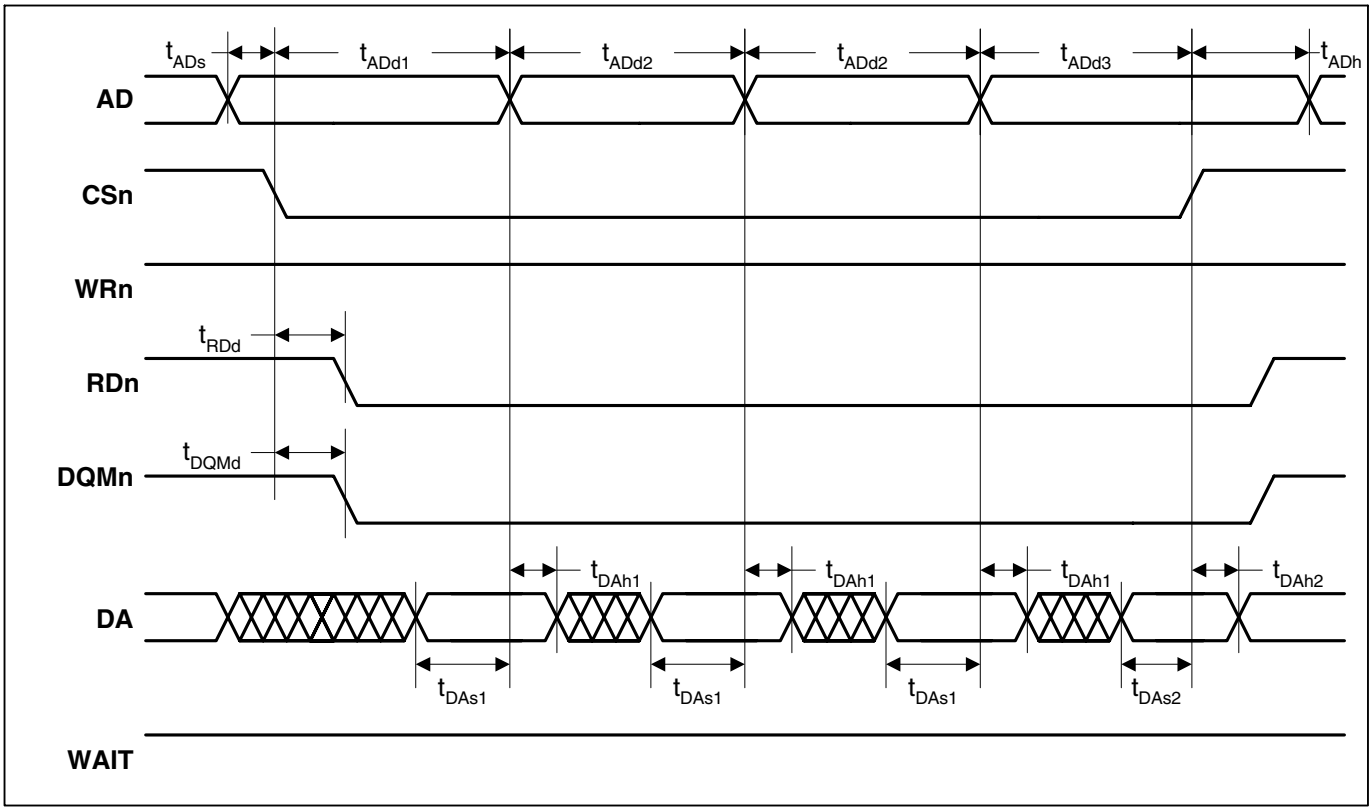


Figure 10. Static Memory Burst Read Cycle Timing Measurement

Static Memory Burst Write Cycle

Parameter	Symbol	Min	Typ	Max	Unit
AD setup to WRn assert time	t_{ADs}	$t_{HCLK} - 3$			ns
AD hold from WRn deassert time	t_{ADh}	$t_{HCLK} \times 2$			ns
WRN/DQMn deassert to AD transition time	t_{ADd}			$t_{HCLK} + 6$	ns
CSn hold from WRn deassert time	t_{CSh}	7			ns
CSn to WRn assert delay time	t_{WRd}			2	ns
CSn to DQMn assert delay time	t_{DQMd}			1	ns
DQMn assert time	t_{DQpwL}		$t_{HCLK} \times (WST1 + 1)$		ns
DQMn deassert time	t_{DQpwH}			$(t_{HCLK} \times 2) + 14$	ns
WRn assert time	t_{WRpwL}		$t_{HCLK} \times (WST1 + 11)$		ns
WRn deassert time	t_{WRpwH}			$(t_{HCLK} \times 2) + 7$	ns
WRn/DQMn deassert to DA transition time	t_{DAh}	t_{HCLK}			ns
WRn/DQMn assert to DA valid time	t_{DAv}			8	ns

Note: These characteristics are valid when the Page Mode Enable (Burst Mode) bit is set. See the User's Guide for details.

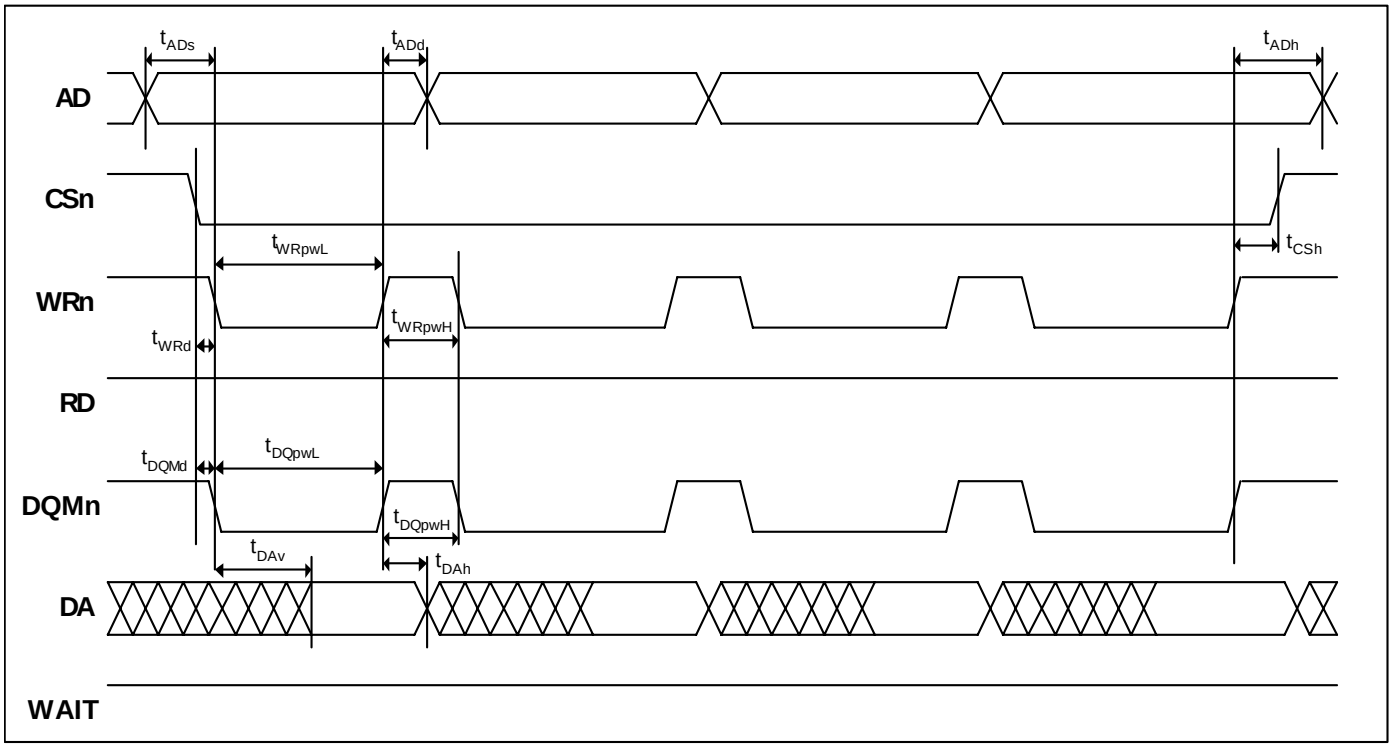


Figure 11. Static Memory Burst Write Cycle Timing Measurement

Static Memory Single Write Wait Cycle

Parameter	Symbol	Min	Typ	Max	Unit
WAIT to WRn deassert delay time	t_{WRd}	$t_{HCLK} \times 2$	-	$t_{HCLK} \times 4$	ns
CSn assert to WAIT time	t_{WAITd}	-	-	$t_{HCLK} \times$ (WST1-2)	ns
WAIT assert time	t_{WAITpw}	$t_{HCLK} \times 2$	-	$t_{HCLK} \times 510$	ns
WAIT to CSn deassert delay time	t_{CSnd}	$t_{HCLK} \times 3$	-	$t_{HCLK} \times 5$	ns

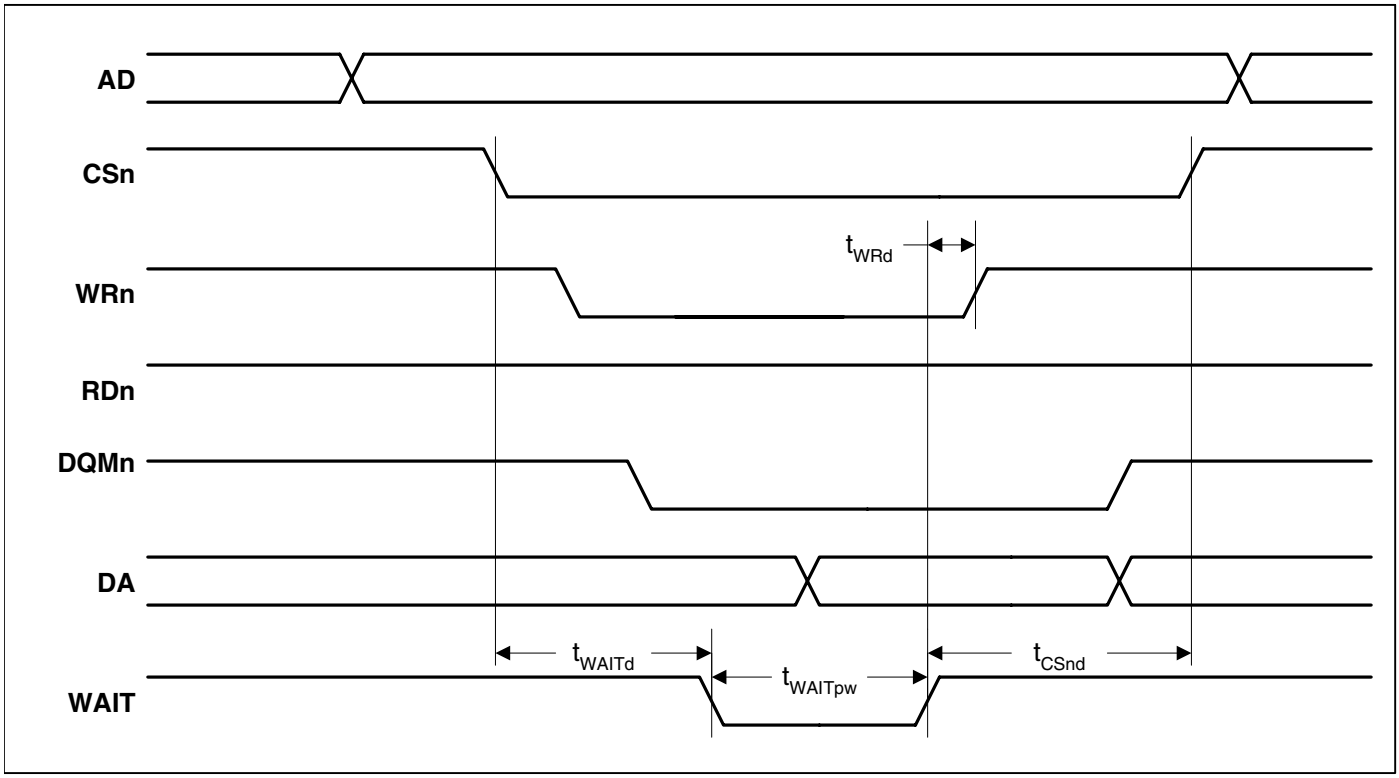


Figure 13. Static Memory Single Write Wait Cycle Timing Measurement

Ethernet MAC Interface

Parameter	Symbol	Min		Typ		Max		Unit
		10 Mbit mode	100 Mbit mode	10 Mbit mode	100 Mbit mode	10 Mbit mode	100 Mbit mode	
TXCLK cycle time	t_{TX_per}	-	-	400	40	-	-	ns
TXCLK high time	t_{TX_high}	140	14	200	20	260	26	ns
TXCLK low time	t_{TX_low}	140	14	200	20	260	26	ns
TXCLK to signal transition delay time	t_{TXd}	0	0	10	10	25	25	ns
TXCLK rise/fall time	t_{TXrf}	-	-	-	-	5	5	ns
RXCLK cycle time	t_{RX_per}	-	-	400	40	-	-	ns
RXCLK high time	t_{RX_high}	140	14	200	20	260	26	ns
RXCLK low time	t_{RX_low}	140	14	200	20	260	26	ns
RXDVAL / RXERR setup time	t_{RXs}	10	10	-	-	-	-	ns
RXDVAL / RXERR hold time	t_{RXh}	10	10	-	-	-	-	ns
RXCLK rise/fall time	t_{RXrf}	-	-	-	-	5	5	ns
MDC cycle time	t_{MDC_per}	-	-	400	400	-	-	ns
MDC high time	t_{MDC_high}	160	160	-	-	-	-	ns
MDC low time	t_{MDC_low}	160	160	-	-	-	-	ns
MDC rise/fall time	t_{MDCrf}	-	-	-	-	5	5	ns
MDIO setup time (STA sourced)	t_{MDIOs}	10	10	-	-	-	-	ns
MDIO hold time (STA sourced)	t_{MDIOh}	10	10	-	-	-	-	ns
MDC to MDIO signal transition delay time (PHY sourced)	t_{MDIOd}	-	-	-	-	300	300	ns

STA - Station - Any device that contains an IEEE 802.11 conforming Medium Access Control (MAC) and physical layer (PHY) interface to the wireless medium.

PHY - Ethernet physical layer interface.

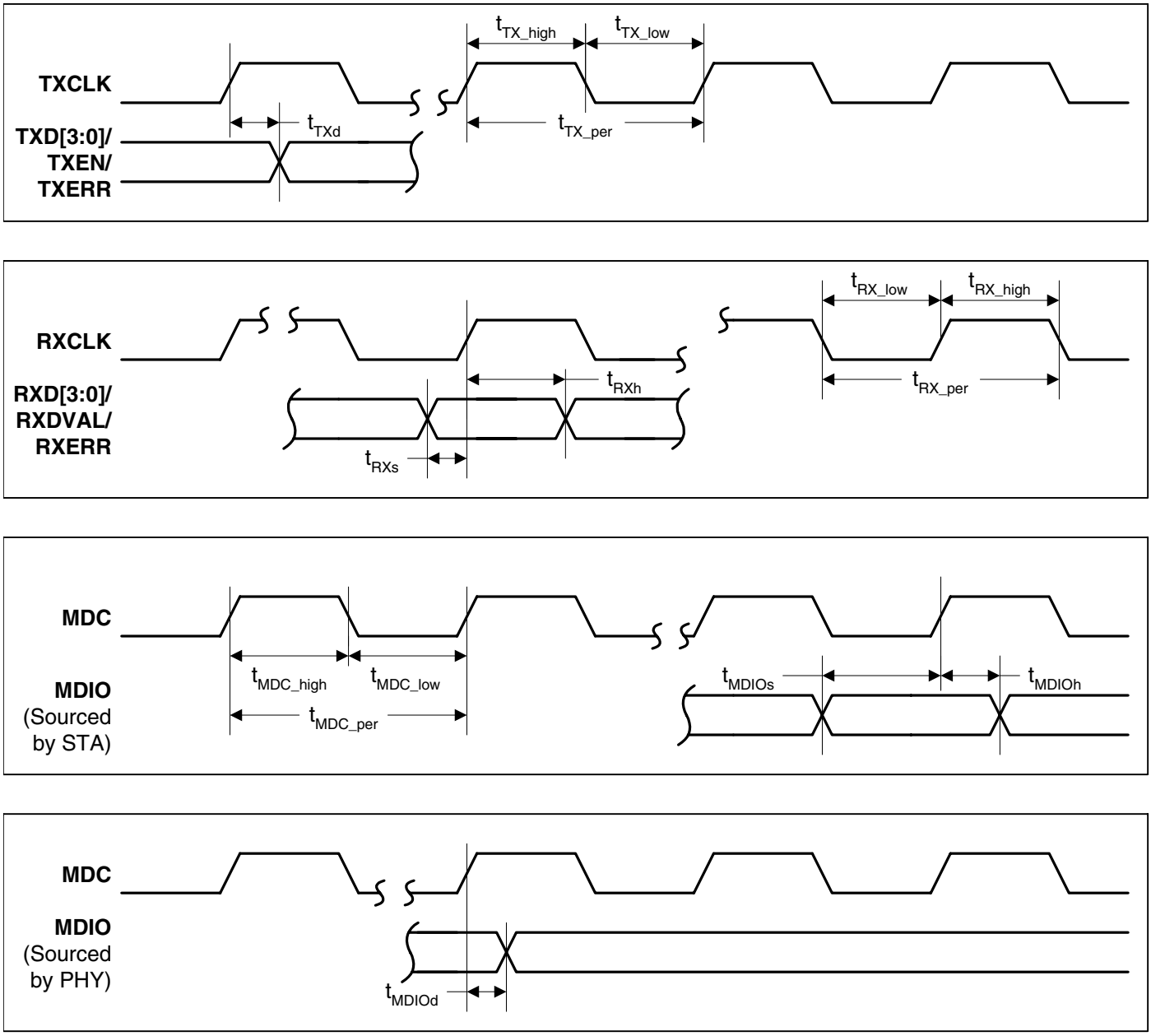


Figure 15. Ethernet MAC Timing Measurement

Audio Interface

The following table contains the values for the timings of each of the SPI modes.

Parameter	Symbol	Min	Typ	Max	Unit
SCLK cycle time	t_{clk_per}	-	tspix_clk	-	ns
SCLK high time	t_{clk_high}	-	(tspix_clk) / 2	-	ns
SCLK low time	t_{clk_low}	-	(tspix_clk) / 2	-	ns
SCLK rise/fall time	t_{clkrf}	1	-	8	ns
Data from master valid delay time	t_{DMd}	-	-	3	ns
Data from master setup time	t_{DMs}	20	-	-	ns
Data from master hold time	t_{DMh}	40	-	-	ns
Data from slave setup time	t_{DSs}	20	-	-	ns
Data from slave hold time	t_{DSh}	40	-	-	ns

Note: The tspix_clk is programmable by the user.

Texas Instruments' Synchronous Serial Format

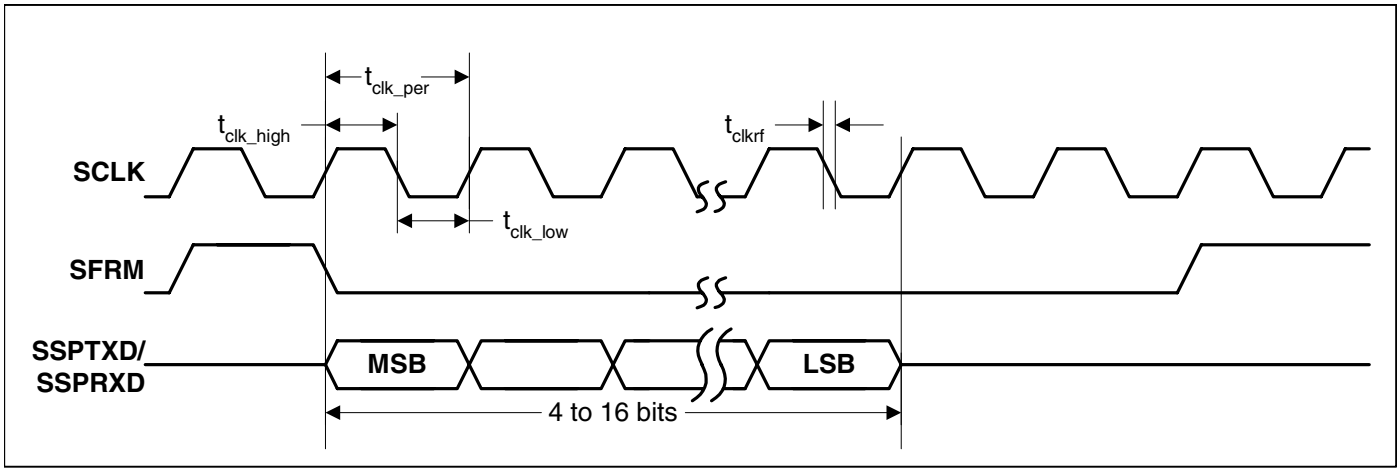


Figure 16. *TI* Single Transfer Timing Measurement

Microwire

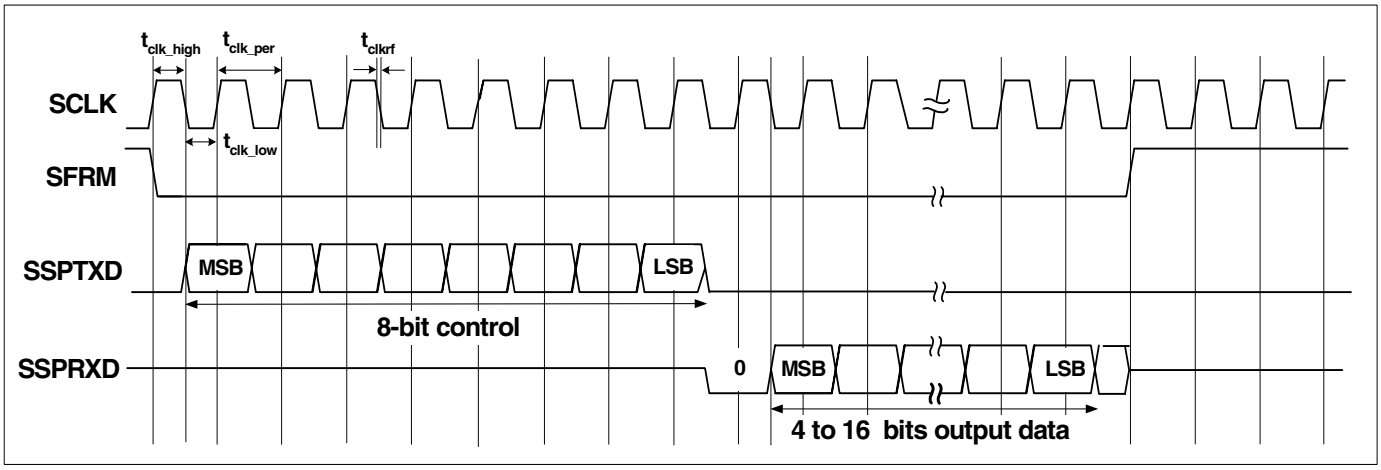


Figure 17. Microwire Frame Format, Single Transfer

AC'97

Parameter	Symbol	Min	Typ	Max	Unit
ABITCLK input cycle time	t_{clk_per}	-	81.4	-	ns
ABITCLK input high time	t_{clk_high}	36	-	45	ns
ABITCLK input low time	t_{clk_low}	36	-	45	ns
ABITCLK input rise/fall time	t_{clkrf}	2	-	6	ns
ASDI setup to ABITCLK falling	t_s	10	-	-	ns
ASDI hold after ABITCLK falling	t_h	10	-	-	ns
ASDI input rise/fall time	t_{rfin}	2	-	6	ns
ABITCLK rising to ASDO / ASYNC valid, C_L = 55 pF	t_{co}	2	-	15	ns
ASYNC / ASDO rise/fall time, C_L = 55 pF	t_{rfout}	2	-	6	ns

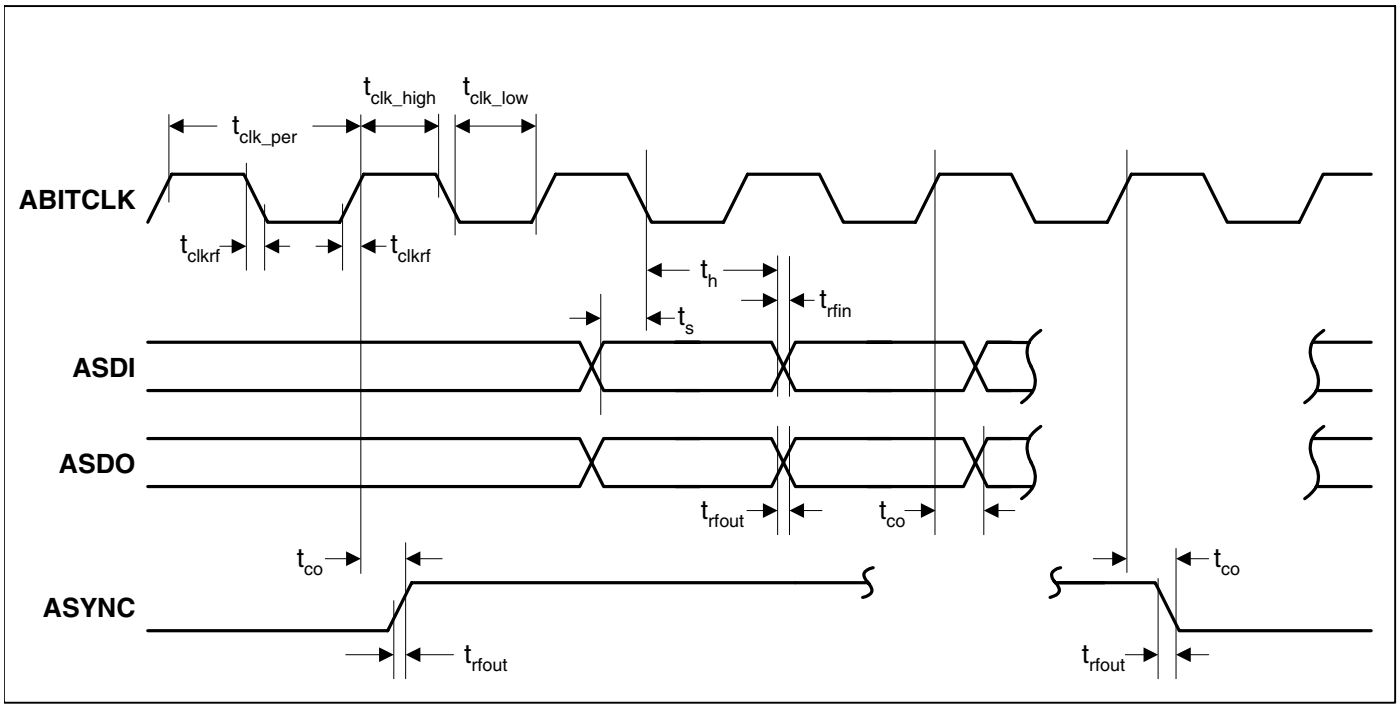
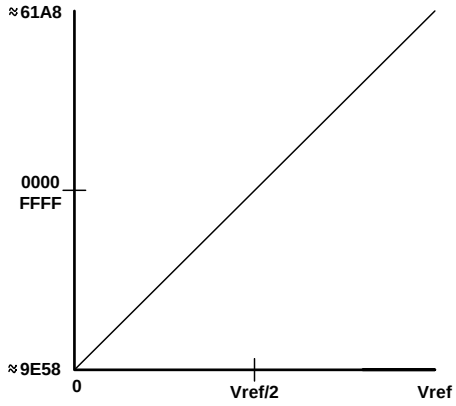


Figure 20. AC '97 Configuration Timing Measurement

ADC

Parameter	Comment	Value	Units
Resolution	No missing codes Range of 0 to 3.3 V	50K counts (approximate)	
Integral non-linearity		0.01%	
Offset error		±15	mV
Full scale error		0.2%	
Maximum sample rate	ADIV = 0 ADIV = 1	3750 925	Samples per second Samples per second
Channel switch settling time	ADIV = 0 ADIV = 1	500 2	µs ms
Noise (RMS) - typical		120	µV

Note: ADIV refers to bit 16 in the KeyTchClkDiv register.
ADIV = 0 means the input clock to the ADC module is equal to the external 14.7456 MHz clock divided by 4.
ADIV = 1 means the input clock to the ADC module is equal to the external 14.7456 MHz clock divided by 16.



A/D Converter Transfer Function
(approximately ±25,000 counts)

Figure 21. ADC Transfer Function

Using the ADC:

This ADC has a state-machine based conversion engine that automates the conversion process. The initiator for a conversion is the read access of the TSXYResult register by the CPU. The data returned from reading this register contains the result as well as the status bit indicating the state of the ADC. However, this peripheral requires a delay between each successful conversion and the issue of the next conversion command, or else the returned value of successive samples may not reflect the analog input. Since the state of the ADC state machine is returned through the same channel used to initiate the conversion process, there must be a delay inserted after every complete conversion. Note that reading TSXYResult during a conversion will not affect the result of the ongoing process.

The following is a recommended procedure for safely polling the ADC from software:

1. Read the TSXYResult register into a local variable to initiate a conversion.
2. If the value of bit 31 of the local variable is '0' then repeat step 1.
3. Delay long enough to meet the maximum sample rate as shown above.
4. Mask the local variable with 0xFFFF to remove extraneous data.
5. If signed mode is used, do a sign extend of the lower halfword.
6. Return the sampled value.

JTAG

Parameter	Symbol	Min	Max	Units
TCK clock period	t_{clk_per}	100	-	ns
TCK clock high time	t_{clk_high}	50	-	ns
TCK clock low time	t_{clk_low}	50	-	ns
TMS / TDI to clock rising setup time	t_{JPs}	20	-	ns
Clock rising to TMS / TDI hold time	t_{JPh}	45	-	ns
JTAG port clock to output	t_{JPco}	-	30	ns
JTAG port high impedance to valid output	t_{JPzx}	-	30	ns
JTAG port valid output to high impedance	t_{JPxz}	-	30	ns

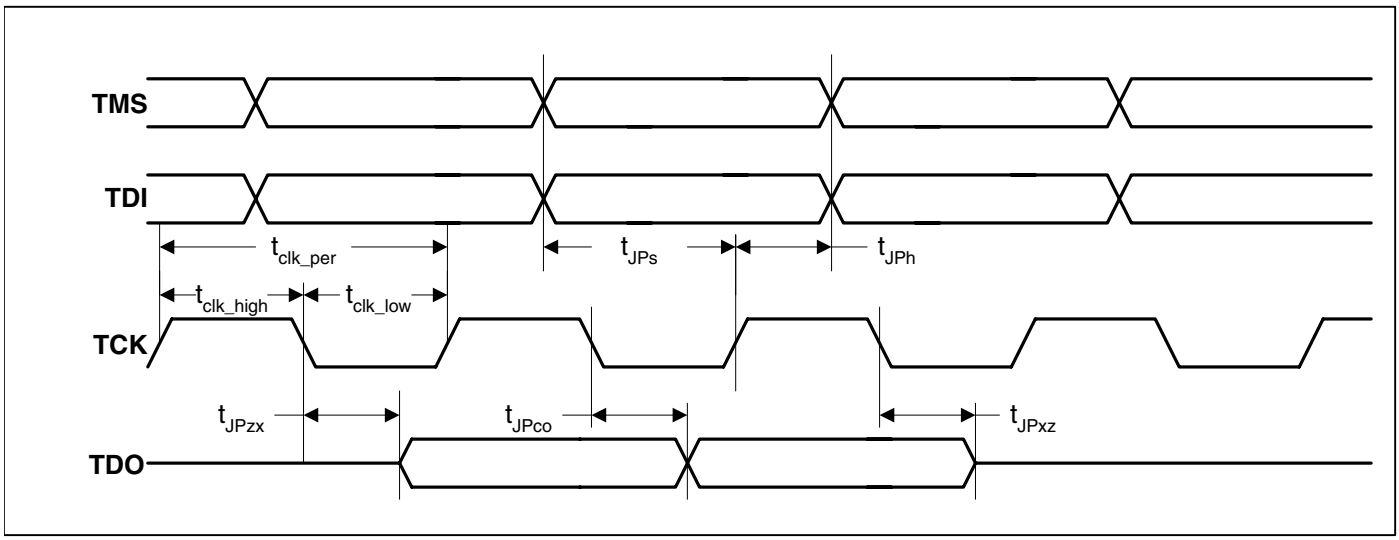
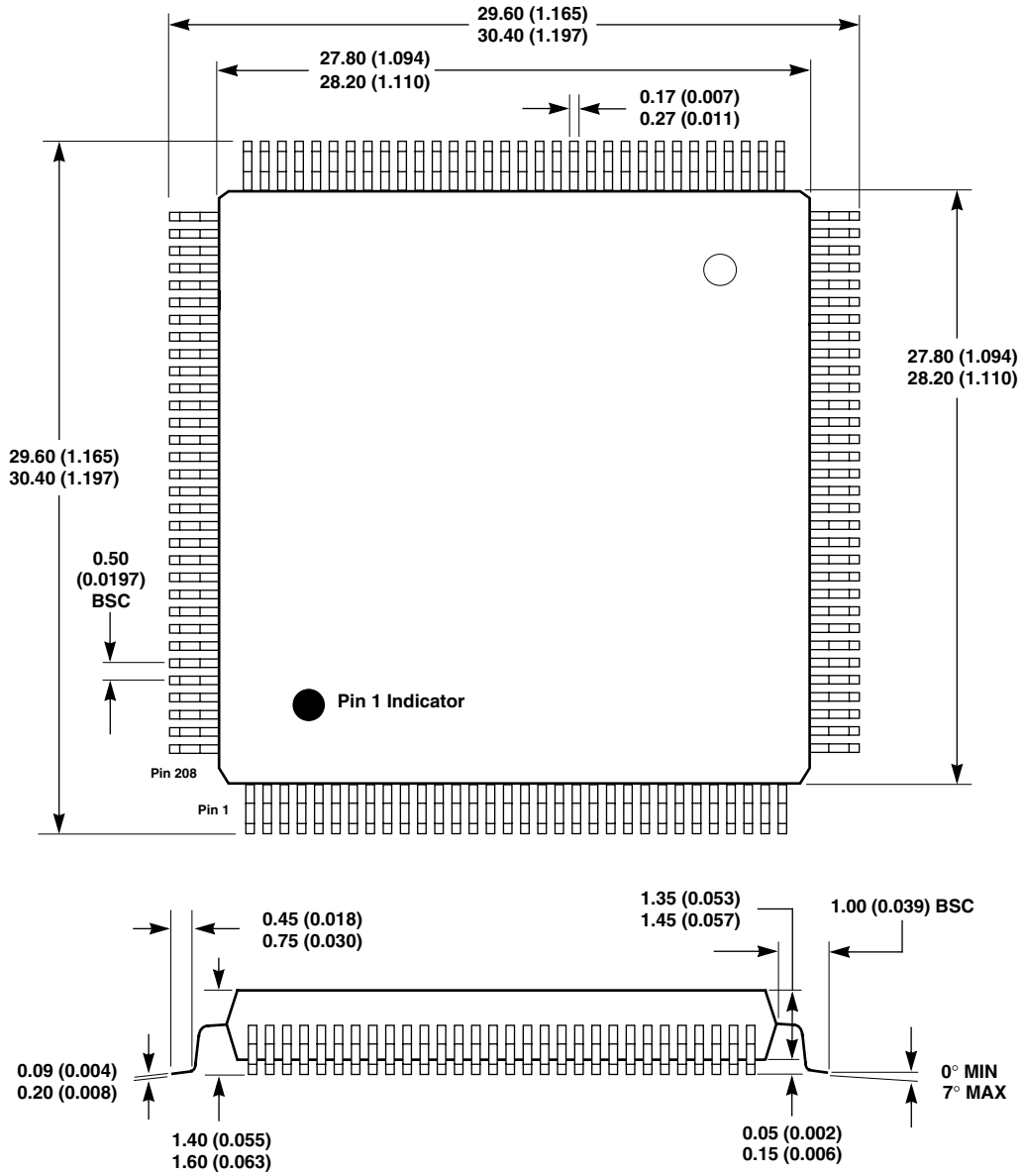


Figure 22. JTAG Timing Measurement

208 Pin LQFP Package Outline

208-Pin LQFP (28 × 28 × 1.40-mm Body)



NOTES:

1) Dimensions are in millimeters, and controlling dimension is millimeter.
2) Package body dimensions do not include mold protrusion, which is 0.25 mm (0.010 in).
3) Pin 1 identification may be either ink dot or dimple.
4) Package top dimensions can be smaller than bottom dimensions by 0.20 mm (0.008 in).
5) The 'lead width with plating' dimension does not include a total allowable dambar protrusion of 0.08 mm (at maximum material condition).
6) Ejector pin marks in molding are present on every package.
7) Drawing above does not reflect exact package pin count.

.

Table Q. Pin Description

Pin Name	Block	Pad Type	Pull Type	Description
TCK	JTAG	I	PD	JTAG clock in
TDI	JTAG	I	PD	JTAG data in
TDO	JTAG	4ma		JTAG data out
TMS	JTAG	I	PD	JTAG test mode select
TRSTn	JTAG	I	PD	JTAG reset
BOOT[1:0]	System	I	PD	Boot mode select in
XTALI	PLL	A		Main oscillator input
XTALO	PLL	A		Main oscillator output
VDD_PLL	PLL	P		Main oscillator power, 1.8V
GND_PLL	PLL	G		Main oscillator ground
RTCXTALI	RTC	A		RTC oscillator input
RTCXTALO	RTC	A		RTC oscillator output
WRn	EBUS	4ma		SRAM Write strobe out
RDn	EBUS	4ma		SRAM Read / OE strobe out
WAITn	EBUS	I	PU	SRAM Wait in
AD[25:0]	EBUS	8ma		Shared Address bus out
DA[15:0]	EBUS	8ma	PU	Shared Data bus in/out
CSn[3:0]	EBUS	4ma	PU	Chip select out
CSn[7:6]	EBUS	4ma	PU	Chip select out
DQMn[1:0]	EBUS	8ma		Shared data mask out
SDCLK	SDRAM	8ma		SDRAM clock out
SDCLKEN	SDRAM	8ma		SDRAM clock enable out
SDCSn[3:0]	SDRAM	4ma		SDRAM chip selects out
RASn	SDRAM	8ma		SDRAM RAS out
CASn	SDRAM	8ma		SDRAM CAS out
SDWEn	SDRAM	8ma		SDRAM write enable out
ADC[4:0]	ADC	A		External Analog Measurement Input
VDD_ADC	ADC	P		ADC power, 3.3V
GND_ADC	ADC	G		ADC ground
USBp[2, 0]	USB	A		USB positive signals
USBm[2, 0]	USB	A		USB negative signals
TXD0	UART1	4ma		Transmit out
RXD0	UART1	I	PU	Receive in
CTSn	UART1	I	PU	Clear to send / transmit enable
DSRn	UART1	I	PU	Data set ready / Data Carrier Detect
DTRn	UART1	4ma		Data Terminal Ready output
RTSn	UART1	4ma		Ready to send
TXD1	UART2	4ma		Transmit / IrDA output
RXD1	UART2	I	PU	Receive / IrDA input
MDC	EMAC	4ma		Management data clock
MDIO	EMAC	4ma	PU	Management data input/output
RXCLK	EMAC	I	PD	Receive clock in
MIIRXD[3:0]	EMAC	I	PD	Receive data in
RXDVAL	EMAC	I	PD	Receive data valid
RXERR	EMAC	I	PD	Receive data error
TXCLK	EMAC	I	PU	Transmit clock in
MIITXD[3:0]	EMAC	4ma	PD	Transmit data out

Table Q. Pin Description (Continued)

Pin Name	Block	Pad Type	Pull Type	Description
TXEN	EMAC	4ma	PD	Transmit enable
TXERR	EMAC	4ma	PD	Transmit error
CRS	EMAC	I	PD	Carrier sense
CLD	EMAC	I	PU	Collision detect
GRLED	LED	12ma		Green LED
RDLED	LED	12ma		Red LED
EECLK	EEPROM	4ma	PU	EEPROM / Two-wire Interface clock
EEDAT	EEPROM	4ma	PU	EEPROM / Two-wire Interface data
ABITCLK	AC97	8ma	PD	AC97 bit clock
ASYNC	AC97	8ma	PD	AC97 frame sync
ASDI	AC97	I	PD	AC97 Primary input
ASDO	AC97	8ma	PU	AC97 output
ARSTn	AC97	8ma		AC97 reset
SCLK1	SPI1	I/O, 8ma	PD	SPI bit clock
SFRM1	SPI1	I/O, 8ma	PD	SPI Frame Clock
SSPRX1	SPI1	I	PD	SPI input
SSPTX1	SPI1	8ma		SPI output
INT[3], INT[1:0]	INT	I	PD	External interrupts
PRSTn	Syscon	I	PU	Power on reset
RSTOn	Syscon	4ma		User Reset in out - open drain
EGPIO[15:0]	GPIO	I/O, 4ma	PU	Enhanced GPIO
FGPIO[3:1]	GPIO	I/O, 8ma	PU	GPIO on Port F
HGPIO[5:2]	GPIO	I/O, 8ma	PU	GPIO on Port H
CGPIO[0]	GPIO	I/O, 8ma	PU	GPIO on Port C
CVDD	Power	P		Digital power, 1.8V
RVDD	Power	P		Digital power, 3.3V
CGND	Ground	G		Digital ground
RGND	Ground	G		Digital ground

Table R illustrates the pin signal multiplexing and configuration options.

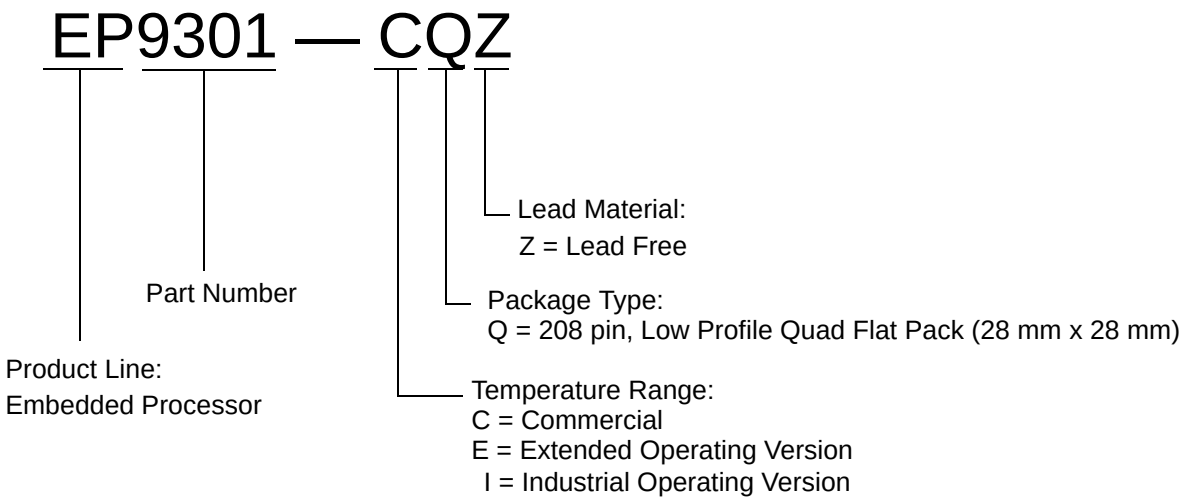
Table R. Pin Multiplex Usage Information

Physical Pin Name	Description	Multiplex signal name
EGPIO[0]	Ring Indicator Input	RI
EGPIO[1]	1Hz clock monitor	CLK1HZ
EGPIO[3]	HDLC Clock	HDLCCLK1
EGPIO[4]	I2S Transmit Data 1	SDO1
EGPIO[5]	I2S Receive Data 1	SDI1
EGPIO[6]	I2S Transmit Data 2	SDO2
EGPIO[7]	DMA Request 0	DREQ0
EGPIO[8]	DMA Acknowledge 0	DACK0
EGPIO[9]	DMA EOT 0	DEOT0
EGPIO[10]	DMA Request 1	DREQ1
EGPIO[11]	DMA Acknowledge 1	DACK1
EGPIO[12]	DMA EOT 1	DEOT1
EGPIO[13]	I2S Receive Data 2	SDI2
EGPIO[14]	PWM1 Output	PWMOUT1
EGPIO[15]	Device active / present	DASP
ABITCLK	I2S Serial clock	SCLK
ASYNC	I2S Frame Clock	LRCK
ASDO	I2S Transmit Data 0	SDO0
ASDI	I2S Receive Data 0	SDI0
ARSTn	I2S Master clock	MCLK
SCLK1	I2S Serial clock	SCLK
SFRM1	I2S Frame Clock	LRCK
SSPTX1	I2S Transmit Data 0	SDO0
SSPRX1	I2S Receive Data 0	SDI0

ORDERING INFORMATION

The order numbers for the device are:

EP9301-CQ	0°C to +70°C	208-pin LQFP	
EP9301-CQZ	0°C to +70°C	208-pin LQFP	Lead Free
EP9301-IQ	-40°C to +85°C	208-pin LQFP	
EP9301-IQZ	-40°C to +85°C	208-pin LQFP	Lead Free



Note: Go to the Cirrus Logic Internet site at http://www.cirrus.com to find contact information for your local sales representative.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to **www.cirrus.com**