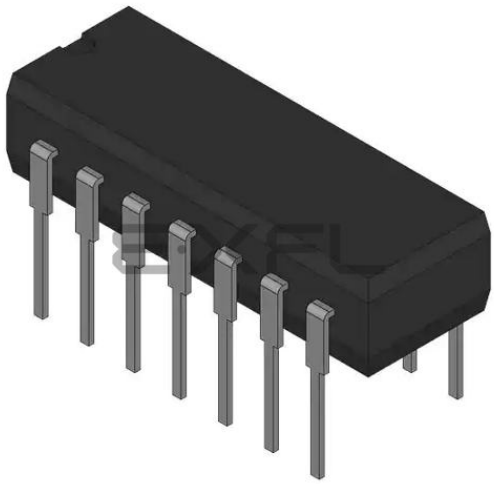

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 8051 |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | SPI |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 12 |
| Program Memory Size | 2KB (2K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 128 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.4V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 14-DIP (0.300", 7.62mm) |
| Supplier Device Package | 14-PDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/atmel/at89lp213-20pu |

**Table 3-2.** **AT89LP214** Pin Description

| Pin | Symbol | Type | Description |
|---|---|---|---|
| 1 | P1.5 | I/O<br>I/O<br><br>I | **P1.5**: User-configurable I/O Port 1 bit 5.<br>**MOSI**: SPI master-out/slave-in. When configured as master, this pin is an output. When configured as slave, this pin is an input.<br>**GPI5**: General-purpose Interrupt input 5. |
| 2 | P1.7 | I/O<br>I/O<br><br>I | **P1.7**: User-configurable I/O Port 1 bit 7.<br>**SCK**: SPI Clock. When configured as master, this pin is an output. When configured as slave, this pin is an input.<br>**GPI7**: General-purpose Interrupt input 7. |
| 3 | P1.3 | I/O<br>I<br>I<br>I | **P1.3**: User-configurable I/O Port 1 bit 3 (if Reset Fuse is disabled).<br>**$\overline{\text{RST}}$**: External **Active-Low** Reset input (if Reset Fuse is enabled. See “External Reset” on page 16).<br>**GPI3**: General-purpose Interrupt input 3.<br>**DCL**: Serial Clock input for On-chip Debug Interface. |
| 4 | GND | I | Ground |
| 5 | P1.2 | I/O<br>I | **P1.2**: User-configurable I/O Port 1 bit 2.<br>**GPI2**: General-purpose Interrupt input 2. |
| 6 | P3.0 | I/O<br>I | **P3.0**: User-configurable I/O Port 3 bit 0.<br>**RXD**: Serial Port Receiver input. |
| 7 | P3.2 | I/O<br>I<br><br>I/O | **P3.2**: User-configurable I/O Port 3 bit 2.<br>**XTAL1**: Input to the inverting oscillator amplifier and internal clock generation circuits. It may be used as a port pin if the internal RC oscillator is selected as the clock source.<br>**DDA**: Serial Data input/output for On-chip Debug Interface when OCD is enabled and the internal RC oscillator is selected as the clock source. |
| 8 | P3.3 | I/O<br>O<br><br>O<br><br>I/O | **P3.3**: User-configurable I/O Port 3 bit 3.<br>**XTAL2**: Output from inverting oscillator amplifier. It may be used as a port pin if the internal RC oscillator is selected as the clock source.<br>**CLKOUT**: When the internal RC oscillator is selected as the clock source, may be used to output the internal clock divided by 2.<br>**DDA**: Serial Data input/output for On-chip Debug Interface when OCD is enabled and the external clock is selected as the clock source.\ |
| 9 | P3.1 | I/O<br>O | **P3.1**: User-configurable I/O Port 3 bit 1.<br>**TXD**: Serial Port Transmitter output. |
| 10 | VCC | I | Supply Voltage |
| 11 | P1.0 | I/O<br>I<br>I | **P1.0**: User-configurable I/O Port 1 bit 0.<br>**AIN0**: Analog Comparator Positive input.<br>**GPI0**: General-purpose Interrupt input 0. |
| 12 | P1.1 | I/O<br>I<br>I | **P1.1**: User-configurable I/O Port 1 bit 1.<br>**AIN1**: Analog Comparator Negative input.<br>**GPI1**: General-purpose Interrupt input 1 |
| 13 | P1.4 | I/O<br>I<br>I | **P1.4**: User-configurable I/O Port 1 bit 4.<br>**$\overline{\text{SS}}$**: SPI slave select input.<br>**GPI4**: General-purpose Interrupt input 4. |
| 14 | P1.6 | I/O<br>I/O<br><br>I | **P1.6**: User-configurable I/O Port 1 bit 6.<br>**MISO**: SPI master-in/slave-out. When configured as master, this pin is an input. When configured as slave, this pin is an output.<br>**GPI6**: General-purpose Interrupt input 6. |

# 7. Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 7-1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect. User software should not write to these unlisted locations, since they may be used in future products to invoke new features.

**Table 7-1.** AT89LP213/214 SFR Map and Reset Values

| | 8 | 9 | A | B | C | D | E | F | |
|---|---|---|---|---|---|---|---|---|---|
| 0F8H | | | | | | | | | 0FFH |
| 0F0H | B<br>0000 0000 | | | | | | | | 0F7H |
| 0E8H | SPSR<br>000x x000 | SPCR<br>0000 0000 | SPDR<br>xxxx xxxx | | | | | | 0EFH |
| 0E0H | ACC<br>0000 0000 | | | | | | | | 0E7H |
| 0D8H | | | | | | | | | 0DFH |
| 0D0H | PSW<br>0000 0000 | | | | | | | | 0D7H |
| 0C8H | | | | | | | | | 0CFH |
| 0C0H | | | P1M0[2] | P1M1<br>xx00 0000 | | | P3M0[2] | P3M1<br>xx00 0000 | 0C7H |
| 0B8H | IP<br>x000 0000 | SADEN<br>0000 0000 | | | | | | | 0BFH |
| 0B0H | P3<br>xx11 1111 | | | | | | | IPH<br>x000 0000 | 0B7H |
| 0A8H | IE<br>0000 0000 | SADDR<br>0000 0000 | | | | | | | 0AFH |
| 0A0H | | | AUXR1<br>xxxx 0xxx | | | | WDTRST<br>(write-only) | WDTCON<br>0000 x000 | 0A7H |
| 98H | SCON<br>0000 0000 | SBUF<br>xxxx xxxx | GPMOD<br>0000 0000 | GPLS<br>0000 0000 | GPIEN<br>0000 0000 | GPIF<br>0000 0000 | | | 9FH |
| 90H | P1<br>1111 1111 | TCONB<br>0010 0100 | RL0<br>0000 0000 | RL1<br>0000 0000 | RH0<br>0000 0000 | RH1<br>0000 0000 | | ACSR<br>xx00 0000 | 97H |
| 88H | TCON<br>0000 0000 | TMOD<br>0000 0000 | TL0<br>0000 0000 | TL1<br>0000 0000 | TH0<br>0000 0000 | TH1<br>0000 0000 | | CLKREG<br>0000 x000 | 8FH |
| 80H | | SP<br>0000 0111 | DPL<br>0000 0000 | DPH<br>0000 0000 | | | | PCON<br>0000 0000 | 87H |
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | |

Notes: 1. All SFRs in the left-most column are bit-addressable.

2. Reset value is xx11 1111B when Tristate-Port Fuse is enabled and xx00 0000B when disabled.

# 8. Enhanced CPU

The AT89LP213/214 uses an enhanced 8051 CPU that runs at 6 to 12 times the speed of standard 8051 devices (or 3 to 6 times the speed of X2 8051 devices). The increase in performance is due to two factors. First, the CPU fetches one instruction byte from the code memory every clock cycle. Second, the CPU uses a simple two-stage pipeline to fetch and execute instructions in parallel. This basic pipelining concept allows the CPU to obtain up to 1 MIPS per MHz. A simple example is shown in Figure 8-1.

The MCS-51 instruction set allows for instructions of variable length from 1 to 3 bytes. In a single-clock-per-byte-fetch system this means each instruction takes at least as many clocks as it has bytes to execute. The majority of instructions in the AT89LP213/214 follow this rule: the instruction execution time in clock cycles equals the number of bytes per instruction with a few exceptions. Branches and Calls require an additional cycle to compute the target address and some other complex instructions require multiple cycles. See “Instruction Set Summary” on page 60 for more detailed information on individual instructions. Figures 8-2 and 8-3 show examples of 1- and 2-byte instructions.

**Figure 8-1.** Parallel Instruction Fetches and Executions

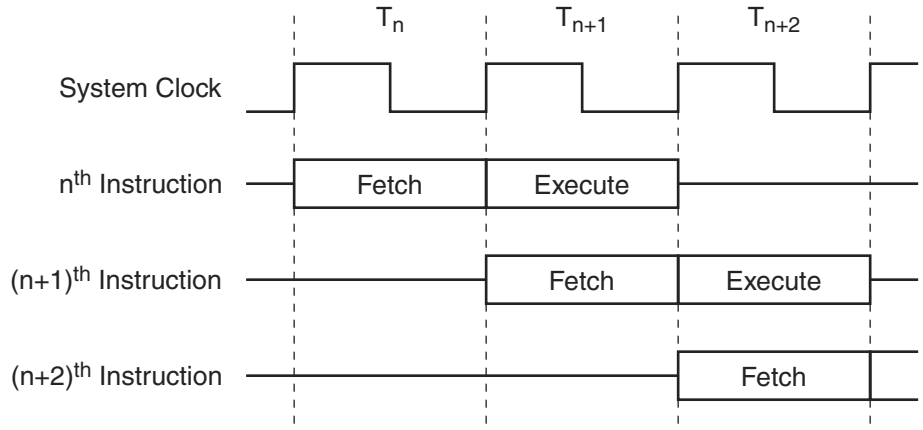
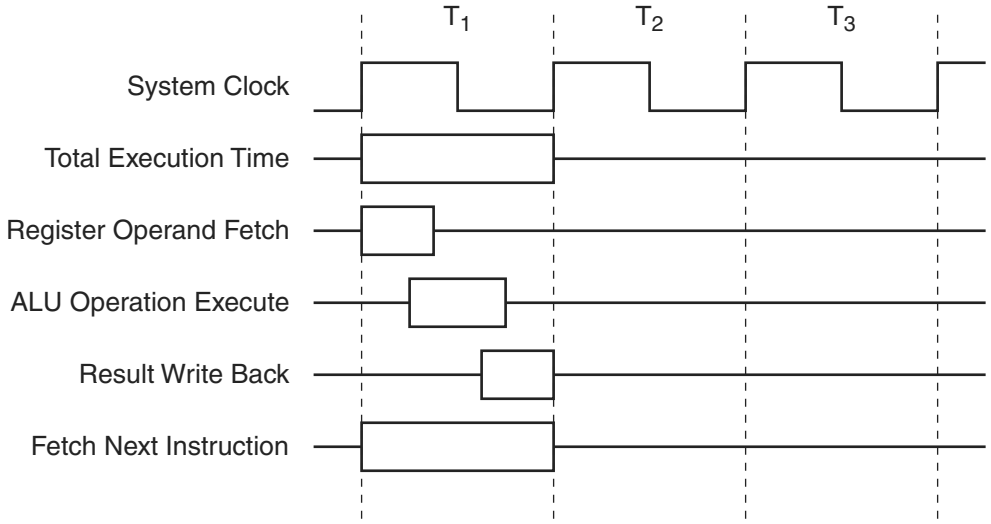


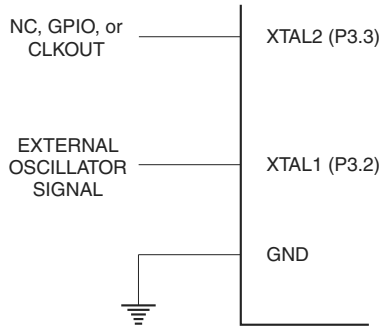

**Figure 8-2.** Single-cycle ALU Operation (Example: INC R0)



## 9.2 External Clock Source

The external clock option disables the oscillator amplifier and allows XTAL1 to be driven directly by the clock source as shown in Figure 9-2. XTAL2 may be left unconnected, used as P3.3 I/O, or configured to output a divided version of the system clock.

**Figure 9-2.** External Clock Drive Configuration




## 9.3 Internal RC Oscillator

The AT89LP213/214 has an internal RC oscillator tuned to 8.0 MHz ±1.0% at 5.0V and 25° C. When enabled as the clock source, XTAL1 and XTAL2 may be used as P3.2 and P3.3 respectively. XTAL2 may also be configured to output a divided version of the system clock. The frequency of the oscillator may be adjusted by changing the RC Adjust Fuses. (See “User Configuration Fuses” on page 72). A copy of the initial factory setting is stored at location 0007h of the Atmel SIgnature.

## 9.4 System Clock Out

When the AT89LP213/214 is configured to use either an external clock or the internal RC oscillator, a divided version of the system clock may be output on XTAL2 (P3.3). The Clock Out feature is enabled by setting the COE bit in CLKREG. The two CDV bits determine the clock divide ratio. For example, setting COE = “1” and CDIV = “00” when using the internal oscillator will result in a 4.0 MHz clock output on P3.3. P3.3 must be configured as an output in order to use the clock out feature.

**Table 9-2.** CLKREG – Clock Control Register

CLKREG = 8FH — Reset Value = 0000 0000B

Not Bit Addressable

| | TPS3 | TPS2 | TPS1 | TPS0 | – | CDV1 | CDV0 | COE |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| Symbol | Function |
|---|---|
| TPS3<br>TPS2<br>TPS1<br>TPS0 | Timer Prescaler. The Timer Prescaler selects the time base for Timer 0, Timer 1 and the Watchdog Timer. The prescaler is implemented as a 4-bit binary down counter. When the counter reaches zero it is reloaded with the value stored in the TPS bits to give a division ratio between 1 and 16. By default the timers will count every clock cycles (TPS = 0000B). To configure the timers to count at a standard 8051 rate of once every 12 clock cycles, TPS should be set to 1011B. |
| CDV1<br>CDV0 | Clock Out Division. Determines the frequency of the clock output relative to the system clock.<br>CDIV1 CDIV0 Clock Out Frequency<br>0 0 f/2<br>0 1 f/4<br>1 0 f/8<br>1 1 f/16 |
| COE | Clock Out Enable. Set COE to output a divided version of the system clock on XTAL2 (P3.3). The internal RC oscillator or external clock source must be selected in order to use this feature. |

# 10. Reset

During reset, all I/O Registers are set to their initial values, the port pins are tristated, and the program starts execution from the Reset Vector, 0000H. The AT89LP213/214 has five sources of reset: power-on reset, brown-out reset, external reset, watchdog reset, and software reset.

## 10.1 Power-on Reset

A Power-on Reset (POR) is generated by an on-chip detection circuit. The detection level is nominally 1.4V. The POR is activated whenever $V_{CC}$ is below the detection level. The POR circuit can be used to trigger the start-up reset or to detect a supply voltage failure in devices without a brown-out detector. The POR circuit ensures that the device is reset from power-on. A power-on sequence is shown in Figure 10-1 on page 15. When $V_{CC}$ reaches the Power-on Reset threshold voltage $V_{POR}$, an initialization sequence lasting $t_{POR}$ is started. When the initialization sequence completes, the start-up timer determines how long the device is kept in POR after $V_{CC}$ rise. The POR signal is activated again, without any delay, when $V_{CC}$ falls below the POR threshold level. A Power-on Reset (i.e. a cold reset) will set the POF flag in PCON. The internally generated reset can be extended beyond the power-on period by holding the $\overline{RST}$ pin low longer than the time-out.

**Table 12-2.** IE – Interrupt Enable Register

IE = A8H — Reset Value = 0000 0000B

Bit Addressable

| | EA | EC | EGP | ES | ET1 | EX1 | ET0 | EX0 |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| Symbol | Function |
|---|---|
| EA | Global enable/disable. All interrupts are disabled when EA = 0. When EA = 1, each interrupt source is enabled/disabled by setting /clearing its own enable bit. |
| EC | Comparator Interrupt Enable |
| EGP | General-purpose Interrupt Enable |
| ES | Serial Port Interrupt Enable |
| ET1 | Timer 1 Interrupt Enable |
| EX1 | External Interrupt 1 Enable |
| ET0 | Timer 0 Interrupt Enable |
| EX0 | External Interrupt 0 Enable |

**Table 12-3.** IP – Interrupt Priority Register

IP = B8H — Reset Value = X000 0000B

Bit Addressable

| | – | – | PGP | PS | PT1 | PX1 | PT0 | PX0 |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| Symbol | Function |
|---|---|
| PGP | General-purpose Interrupt Priority Low |
| PS | Serial Port Interrupt Priority Low |
| PT1 | Timer 1 Interrupt Priority Low |
| PX1 | External Interrupt 1 Priority Low |
| PT0 | Timer 0 Interrupt Priority Low |
| PX0 | External Interrupt 0 Priority Low |

## 13.1 Port Configuration

All port pins on the AT89LP213/214 may be configured to one of four modes: quasi-bidirectional (standard 8051 port outputs), push-pull output, open-drain output, or input-only. Port modes may be assigned in software on a pin-by-pin basis as shown in Table 13-2. The Tristate-Port User Fuse determines the default state of the port pins. When the fuse is enabled, all port pins default to input-only mode after reset, with the exception of P1.4 which starts in quasi-bidirectional mode. When the fuse is disabled, all port pins, with the exception of P1.0 and P1.1, default to quasi-bidirectional mode after reset and are weakly pulled high. Each port pin also has a Schmitt-triggered input for improved input noise rejection. During Power-down all the Schmitt-triggered inputs are disabled with the exception of P1.3, P3.2 and P3.3, which may be used to wake up the device. Therefore P1.3, P3.2 and P3.3 should not be left floating during Power-down. It is recommended that P3.1–0 on AT89LP213 and P3.4–5 on AT89LP214 be configured for either quasi-bidirectional or push-pull output mode.

**Table 13-2.** Configuration Modes for Port x, Bit y

| PxM0.y | PxM1.y | Port Mode |
|---|---|---|
| 0 | 0 | Quasi-bidirectional |
| 0 | 1 | Push-pull Output |
| 1 | 0 | Input Only (High Impedance) |
| 1 | 1 | Open-drain Output |

### 13.1.1 Quasi-bidirectional Output

Port pins in quasi-bidirectional output mode function similar to standard 8051 port pins. A Quasi-bidirectional port can be used both as an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low. When the pin is driven low, it is driven strongly and able to sink a large current. There are three pull-up transistors in the quasi-bidirectional output that serve different purposes. One of these pull-ups, called the “very weak” pull-up, is turned on whenever the port latch for the pin contains a logic “1”. This very weak pull-up sources a very small current that will pull the pin high if it is left floating.

A second pull-up, called the “weak” pull-up, is turned on when the port latch for the pin contains a logic “1” and the pin itself is also at a logic “1” level. This pull-up provides the primary source current for a quasi-bidirectional pin that is outputting a “1”. If this pin is pulled low by an external device, this weak pull-up turns off, and only the very weak pull-up remains on. In order to pull the pin low under these conditions, the external device has to sink enough current to overpower the weak pull-up and pull the port pin below its input threshold voltage.

The third pull-up is referred to as the “strong” pull-up. This pull-up is used to speed up low-to-high transitions on a quasi-bidirectional port pin when the port latch changes from a logic “0” to a logic “1”. When this occurs, the strong pull-up turns on for two CPU clocks quickly pulling the port pin high. The quasi-bidirectional port configuration is shown in Figure 13-1. The input circuitry of P1.3, P3.2 and P3.3 is not disabled during Power-down (see Figure 13-3).

## 15. External Interrupts

When the AT89LP213/214 is configured to use the internal RC Oscillator, XTAL1 and XTAL2 may be used as the $\overline{INT0}$ and $\overline{INT1}$ external interrupt sources. When the external clock source is used, XTAL2 is available as $\overline{INT1}$. Neither interrupt is available in crystal oscillator mode. The external interrupts can be programmed to be level-activated or transition-activated by setting or clearing bit IT1 or IT0 in Register TCON. If ITx = 0, external interrupt x is triggered by a detected low at the $\overline{INTx}$ pin. If ITx = 1, external interrupt x is edge-triggered. In this mode if successive samples of the $\overline{INTx}$ pin show a high in one cycle and a low in the next cycle, interrupt request flag IEx in TCON is set. Flag bit IEx then requests the interrupt. Since the external interrupt pins are sampled once each clock cycle, an input high or low should hold for at least 2 oscillator periods to ensure sampling. If the external interrupt is transition-activated, the external source has to hold the request pin high for at least two clock cycles, and then hold it low for at least two clock cycles to ensure that the transition is seen so that interrupt request flag IEx will be set. IEx will be automatically cleared by the CPU when the service routine is called if generated in edge-triggered mode. If the external interrupt is level-activated, the external source has to hold the request active until the requested interrupt is actually generated. Then the external source must deactivate the request before the interrupt service routine is completed, or else another interrupt will be generated.

## 16. General-purpose Interrupts

The General-purpose Interrupt (GPI) function provides 8 configurable external interrupts on Port 1. Each port pin can detect high/low levels or positive/negative edges. The GPIEN register select which bits of Port 1 are enabled to generate an interrupt. The GPMOD and GPLS registers determine the mode for each individual pin. GPMOD selects between level-sensitive and edge-triggered mode. GPLS selects between high/low in level mode and positive/negative in edge mode. The pins of Port 1 are sampled every clock cycle. In level-sensitive mode, a valid level must appear in two successive samples before generating the interrupt. In edge-triggered mode, a transition will be detected if the value changes from one sample to the next. When an interrupt condition on a pin is detected, and that pin is enabled, the appropriate flag in the GPIF register is set. The flags in GPIF must be cleared by software.

**Table 16-1.** GPMOD – General-purpose Interrupt Mode Register

GPMOD = 9AH — Reset Value = 0000 0000B

Not Bit Addressable

| | GPMOD7 | GPMOD6 | GPMOD5 | GPMOD4 | GPMOD3 | GPMOD2 | GPMOD1 | GPMOD0 |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

GPMOD.x 0 = level-sensitive interrupt for P1.x

1 = edge-triggered interrupt for P1.x

## 17.3 More About Mode 0

Serial data enters and exits through RXD. TXD outputs the shift clock. Eight data bits are transmitted/received, with the LSB first. The baud rate is fixed at 1/2 the oscillator frequency. Figure 17-1 on page 43 shows a simplified functional diagram of the serial port in Mode 0 and associated timing.

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal also loads a “1” into the 9th position of the transmit shift register and tells the TX Control Block to begin a transmission. The internal timing is such that one full machine cycle will elapse between “write to SBUF” and activation of SEND.

SEND transfers the output of the shift register to the alternate output function line of P3.0, and also transfers Shift Clock to the alternate output function line of P3.1. At the falling edge of Shift Clock the contents of the transmit shift register are shifted one position to the right.

As data bits shift out to the right, “0”s come in from the left. When the MSB of the data byte is at the output position of the shift register, the “1” that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contain “0”s. This condition flags the TX Control block to do one last shift, then deactivate SEND and set TI.

Reception is initiated by the condition REN = 1 and R1 = 0. At the next clock cycle, the RX Control unit writes the bits 11111110 to the receive shift register and activates RECEIVE in the next clock phase.

RECEIVE enables Shift Clock to the alternate output function line of P3.1. At the falling edge of Shift Clock the contents of the receive shift register are shifted one position to the left. The value that comes in from the right is the value that was sampled at the P3.0 pin at rising edge of Shift Clock.

As data bits come in from the right, “1”s shift out to the left. When the “0” that was initially loaded into the right-most position arrives at the left-most position in the shift register, it flags the RX Control block to do one last shift and load SBUF. Then RECEIVE is cleared and RI is set.

## 17.5 More About Modes 2 and 3

Eleven bits are transmitted (through TXD), or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmit, the 9th data bit (TB8) can be assigned the value of “0” or “1”. On receive, the 9th data bit goes into RB8 in SCON. The baud rate is programmable to either 1/16 or 1/32 of the oscillator frequency in Mode 2. Mode 3 may have a variable baud rate generated from Timer 1.

Figures 17-3 and 17-4 show a functional diagram of the serial port in Modes 2 and 3. The receive portion is exactly the same as in Mode 1. The transmit portion differs from Mode 1 only in the 9th bit of the transmit shift register.

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal also loads TB8 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. Thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SBUF” signal.

The transmission begins when $\overline{\text{SEND}}$ is activated, which puts the start bit at TXD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TXD. The first shift pulse occurs one bit time after that. The first shift clocks a “1” (the stop bit) into the 9th bit position of the shift register. Thereafter, only “0”s are clocked in. Thus, as data bits shift out to the right, “0”s are clocked in from the left. When TB8 is at the output position of the shift register, then the stop bit is just to the left of TB8, and all positions to the left of that contain “0”s. This condition flags the TX Control unit to do one last shift, then deactivate SEND and set TI. This occurs at the 11th divide-by-16 rollover after “write to SBUF.”

Reception is initiated by a 1-to-0 transition detected at RXD. For this purpose, RXD is sampled at a rate of 16 times the established baud rate. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written to the input shift register.

At the 7th, 8th and 9th counter states of each bit time, the bit detector samples the value of RXD. The value accepted is the value that was seen in at least 2 of the 3 samples. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit continues looking for another l-to-0 transition. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame proceeds.

As data bits come in from the right, “1”s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in Modes 2 and 3 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8 and to set RI is generated if, and only if, the following conditions are met at the time the final shift pulse is generated:

RI = 0, and

Either SM2 = 0 or the received 9th data bit = 1

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set. If both conditions are met, the received 9th data bit goes into RB8, and the first 8 data bits go into SBUF. One bit time later, whether the above conditions were met or not, the unit continues looking for a 1-to-0 transition at the RXD input.

Note that the value of the received stop bit is irrelevant to SBUF, RB8, or RI.

## 17.6 Framing Error Detection

In addition to all of its usual modes, the UART can perform framing error detection by looking for missing stop bits, and automatic address recognition. When used for framing error detect, the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6 (SMOD0). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE, SCON.7 can only be cleared by software. The FE bit will be set by a framing error regardless of the state of SMOD0.

## 17.7 Automatic Address Recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9th bit UART modes, Mode 2 and Mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the “Given” address or the “Broadcast” address. The 9th bit mode requires that the 9th information bit to be a “1” to indicate that the received information is an address and not data.

The 8th bit mode is called Mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8th address bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave’s address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are “don’t care”. The SADEN mask can be logically ANDed with the SADDR to create the “Given” address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples show the versatility of this scheme:

Slave 0 SADDR = 1100 0000

SADEN = 1111 1101

Given = 1100 00X0

Slave 1 SADDR = 1100 0000

SADEN = 1111 1110

Given = 1100 000X

In the previous example, SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a “0” in bit 0 and it ignores bit 1. Slave 1 requires a “0” in bit 1 and bit 0 is ignored. A unique address for slave 0 would be 1100 0010 since slave 1 requires a “0” in bit 1. A unique address for slave 1 would be 1100 0001 since a “1” in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

**Table 21-1.** Instruction Execution Times and Exceptions (Continued)

| Data Transfer | Bytes | Clock Cycles | | Hex Code |
|---|---|---|---|---|
| | | 8051 | AT89LP | |
| MOV A, Rn | 1 | 12 | 1 | E8-EF |
| MOV A, direct | 2 | 12 | 2 | E5 |
| MOV A, @Ri | 1 | 12 | 2 | E6-E7 |
| MOV A, #data | 2 | 12 | 2 | 74 |
| MOV Rn, A | 1 | 12 | 1 | F8-FF |
| MOV Rn, direct | 2 | 24 | 2 | A8-AF |
| MOV Rn, #data | 2 | 12 | 2 | 78-7F |
| MOV direct, A | 2 | 12 | 2 | F5 |
| MOV direct, Rn | 2 | 24 | 2 | 88-8F |
| MOV direct, direct | 3 | 24 | 3 | 85 |
| MOV direct, @Ri | 2 | 24 | 2 | 86-87 |
| MOV direct, #data | 3 | 24 | 3 | 75 |
| MOV @Ri, A | 1 | 12 | 1 | F6-F7 |
| MOV @Ri, direct | 2 | 24 | 2 | A6-A7 |
| MOV @Ri, #data | 2 | 12 | 2 | 76-77 |
| MOV DPTR, #data16 | 3 | 24 | 3 | 90 |
| MOVC A, @A+DPTR | 1 | 24 | 3 | 93 |
| MOVC A, @A+PC | 1 | 24 | 3 | 83 |
| MOVX A, @Ri | 1 | 24 | 4 | E2-E3 |
| MOVX A, @DPTR | 1 | 24 | 4 | E0 |
| MOVX @Ri, A | 1 | 24 | 4 | F2-F3 |
| MOVX @DPTR, A | 1 | 24 | 4 | F0 |
| PUSH direct | 2 | 24 | 2 | C0 |
| POP direct | 2 | 24 | 2 | D0 |
| XCH A, Rn | 1 | 12 | 1 | C8-CF |
| XCH A, direct | 2 | 12 | 2 | C5 |
| XCH A, @Ri | 1 | 12 | 2 | C6-C7 |
| XCHD A, @Ri | 1 | 12 | 2 | D6-D7 |

# 22. On-chip Debug System

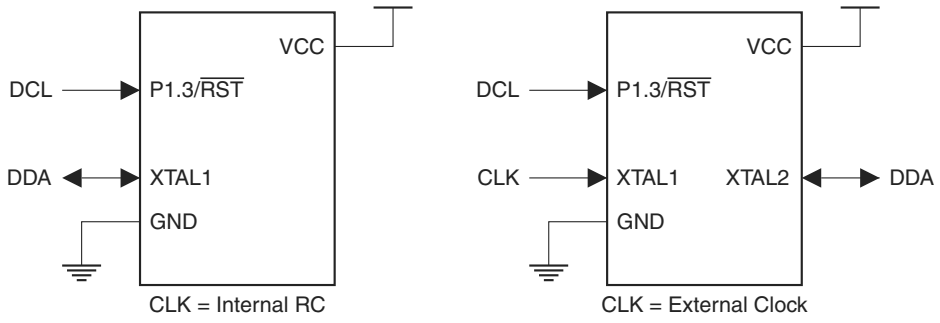
The AT89LP213/214 On-chip Debug (OCD) System uses a two-wire serial interface to control program flow; read, modify, and write the system state; and program the nonvolatile memory. The OCD System has the following features:

- Complete program flow control
- Read-modify-write access to all internal SFRs and data memories
- Four hardware program address breakpoints
- Unlimited program software breakpoints using BREAK instruction
- Break on stack overflow/underflow
- Break on Watchdog overflow
- Non-intrusive operation
- Programming of nonvolatile memory

## 22.1 Physical Interface

The On-chip Debug System uses a two-wire synchronous serial interface to establish communication between the target device and the controlling emulator system. The OCD interface is controlled by two User Fuses. OCD is enabled by clearing the OCD $\overline{\text{Enable}}$ Fuse. When OCD is enabled, the $\overline{\text{RST}}$ port pin is configured as an input for the Debug Clock (DCL). Either the XTAL1 or XTAL2 pin is configured as a bi-directional data line for the Debug Data (DDA) depending on the clock source selected. If the External Clock is selected, XTAL2 is configured as DDA. If the Internal RC Oscillator is selected, XTAL1 is configured as DDA. The OCD device connections are shown in Figure 22-1. The OCD Interface Select User Fuse should always be set for the fast two-wire interface (FTWI). It is the duty of the user to program these fuses to the correct settings before using the device in their debug system (see “User Configuration Fuses” on page 72).

**Figure 22-1.** AT89LP213/214 On-chip Debug Connections




When designing a system where On-chip Debug will be used, the following observations must be considered for correct operation:

- P1.3/$\overline{\text{RST}}$ cannot be connected directly to $V_{CC}$ and any external capacitors connect to $\overline{\text{RST}}$ must be removed.
- All external reset sources must be removed.
- The quartz crystal and any capacitors on XTAL1 or XTAL2 must be removed and an external clock signal must be driven on XTAL1 if the user does not wish to use the internal RC oscillator. Some emulator systems may provide a user-configurable clock for this purpose.

### 22.2 Software Breakpoints

The AT89LP213/214 microcontroller includes a BREAK instruction for implementing program memory breakpoints in software. A software breakpoint can be inserted manually by placing the BREAK instruction in the program code. Some emulator systems may allow for automatic insertion/deletion of software breakpoints. The Flash memory must be re-programmed each time a software breakpoint is changed. Frequent insertions/deletions of software breakpoints will reduce the data retention of the nonvolatile memory. Devices used for debugging purposes should not be shipped to end customers. The BREAK instruction is treated as a two-cycle NOP when OCD is disabled.

### 22.3 Limitations of On-chip Debug

The AT89LP213/214 is a low-cost, low-pincount yet fully-featured microcontroller that multiplexes several functions on its limited I/O pins. Some device functionality must be sacrificed to provide resources for On-chip Debugging. The On-chip Debug System has the following limitations:

- The Debug Clock pin (DCL) is physically located on that same pin as Port Pin P1.3 and the External Reset ($\overline{RST}$). Therefore, neither P1.3 nor an external reset source may be emulated when OCD is enabled.
- The Debug Data pin (DDA) is physically located on either the XTAL1/P3.2 or XTAL2/P3.3 pin. The crystal oscillator is therefore not supported during debug. The user must select either the Internal RC Oscillator or the External Clock source to provide the system clock. Devices fused for the crystal oscillator will default to external clock mode when OCD is enabled.
- When using the Internal RC Oscillator during debug, DDA is located on the XTAL1/P3.2 pin. The $\overline{INT0}$ function cannot be emulated in this mode.
- When using the External Clock during debug, DDA is located on the XTAL2/P3.3 pin and the system clock drives XTAL1/P3.2. The $\overline{INT0}$, $\overline{INT1}$ and CLKOUT functions cannot be emulated in this mode.
- The AT89LP213/214 does not support In-Application Programming and therefore the device must be reset before changing the program code during debugging. This includes the insertion/deletion of software breakpoints.
- When using the watchdog to generate a break, the state of the watchdog will not be reset. An OCD reset command should be sent to the device prior to resuming normal execution to ensure correct watchdog behavior.

## 23. Programming the Flash Memory

The Atmel AT89LP213/214 microcontroller features 2KB of on-chip In-System Programmable Flash program memory. In-System Programming (ISP) allows programming and reprogramming of the microcontroller positioned inside the end system. Using a simple 4-wire SPI interface, the In-System programmer communicates serially with the AT89LP213/214 microcontroller, reprogramming all nonvolatile memories on the chip. In-System programming eliminates the need for physical removal of the chips from the system. This will save time and money, both during development in the lab, and when updating the software or parameters in the field. The ISP interface of the AT89LP213/214 includes the following features:

- Four Wire SPI Programming Interface
- Active-low Reset Entry into Programming
- Slave Select allows multiple devices on same interface
- User Signature Array

### 24.3.3 Internal Oscillator Frequency

**Figure 24-5.** Internal Oscillator Frequency vs. VCC

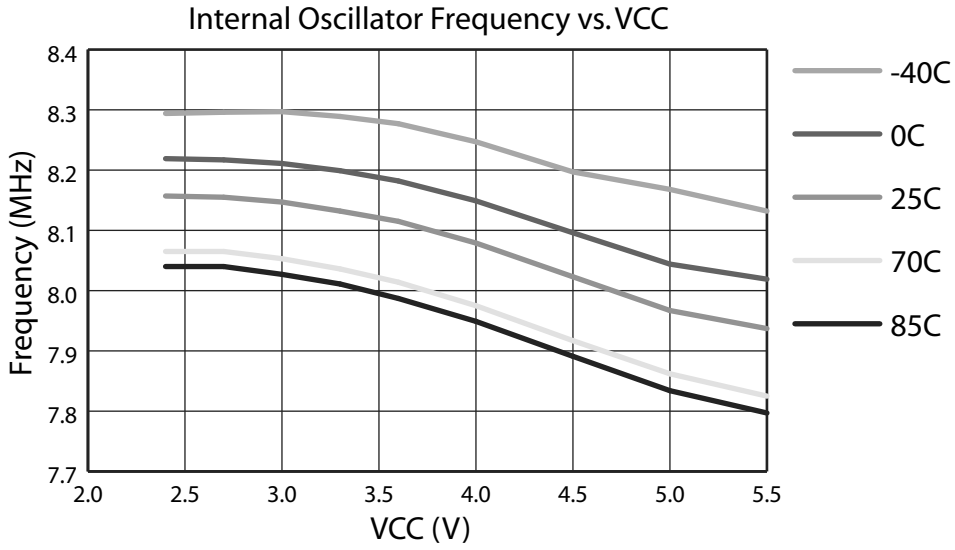



**Table 24-1.** Typical Internal Oscillator Behavior

| Symbol | Parameter | Condition | Min | Max | Units |
|---|---|---|---|---|---|
| $\Delta f_{IRC}$ | Relative Frequency Error (MAX–MIN) / (MAX+MIN) | $T_A$ = -40–85°C; $V_{CC}$ = 2.4–5.5V | | ±4 | % |
| | | $T_A$ = -40–85°C; $V_{CC}$ = 4.5–5.5V | | ±3 | % |
| | | $T_A$ = -40–85°C; $V_{CC}$ = 2.4–3.6V | | ±3 | % |
| | | $T_A$ = 0–70°C; $V_{CC}$ = 2.4–5.5V | | ±3 | % |
| | | $T_A$ = 0–70°C; $V_{CC}$ = 4.5–5.5V | | ±2 | % |
| | | $T_A$ = 0–70°C; $V_{CC}$ = 2.4–3.6V | | ±2 | % |
| $f_{IRC}$ | Frequency (Calibrated at 25°C; 5V) | $T_A$ = -40–85°C; $V_{CC}$ = 2.4–5.5V | 7.8 | 8.4 | MHz |
| | | $T_A$ = -40–85°C; $V_{CC}$ = 4.5–5.5V | 7.8 | 8.2 | MHz |
| | | $T_A$ = -40–85°C; $V_{CC}$ = 2.4–3.6V | 8.0 | 8.4 | MHz |
| | | $T_A$ = 0–70°C; $V_{CC}$ = 2.4–5.5V | 7.8 | 8.3 | MHz |
| | | $T_A$ = 0–70°C; $V_{CC}$ = 4.5–5.5V | 7.8 | 8.1 | MHz |
| | | $T_A$ = 0–70°C; $V_{CC}$ = 2.4–3.6V | 8.0 | 8.3 | MHz |

Note: The data in this table was characterized on factory calibrated devices. It is not tested during manufacturing and is provided for reference only. Devices may need to be recalibrated to target different operating conditions than the single-point factory calibration.

### 24.3.6 Crystal Oscillator

**Figure 24-10.** Quartz Crystal Input at 5V

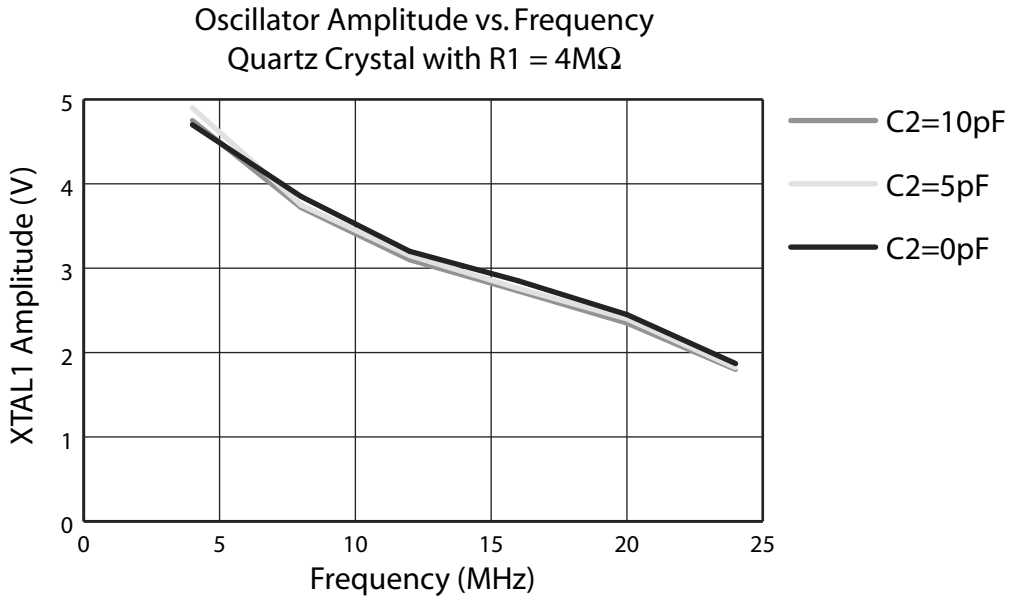



**Figure 24-11.** Ceramic Resonator Input at 5V

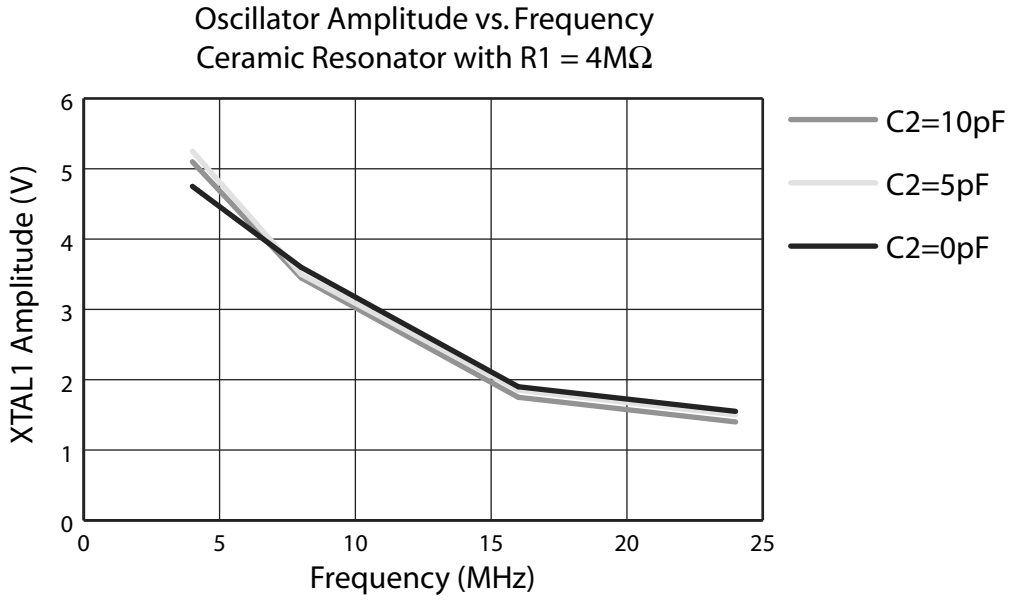


**Figure 24-13.** SPI Master Timing (CPHA = 0)

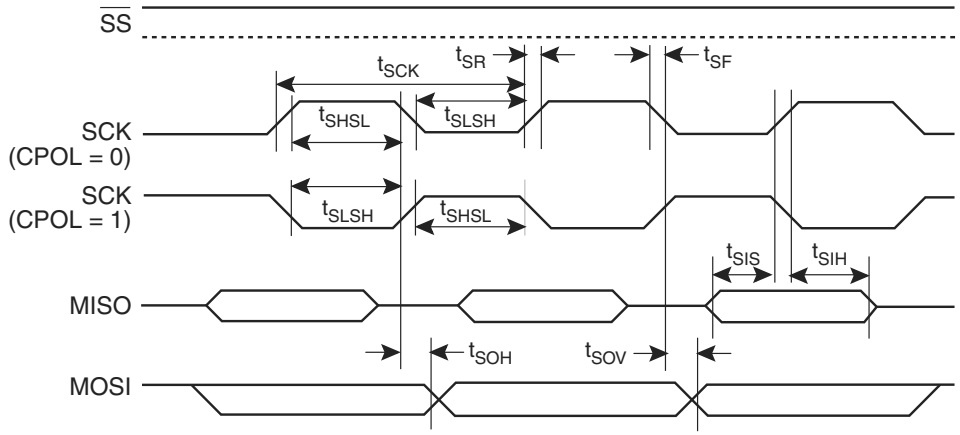



**Figure 24-14.** SPI Slave Timing (CPHA = 0)

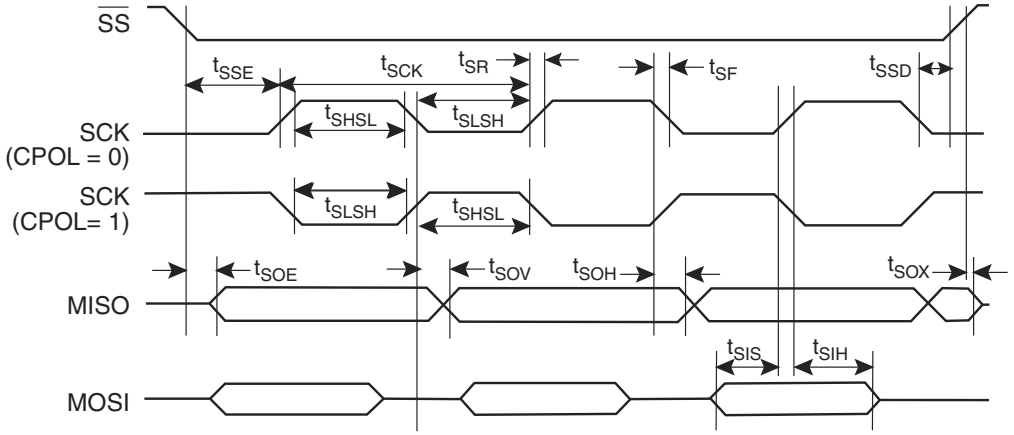
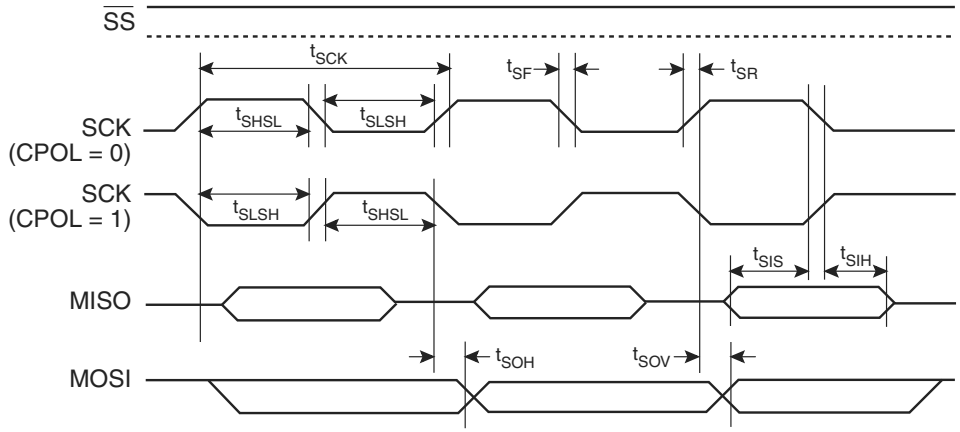
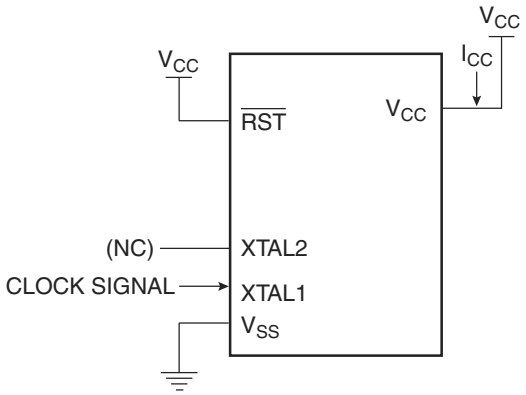


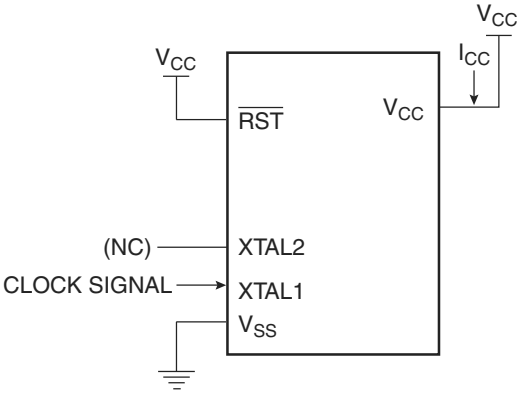

**Figure 24-15.** SPI Master Timing (CPHA = 1)



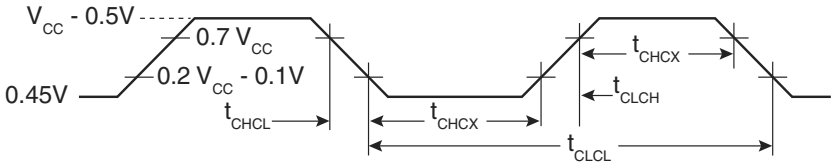
### 24.7.3 $I_{CC}$ Test Condition, Active Mode, All Other Pins are Disconnected



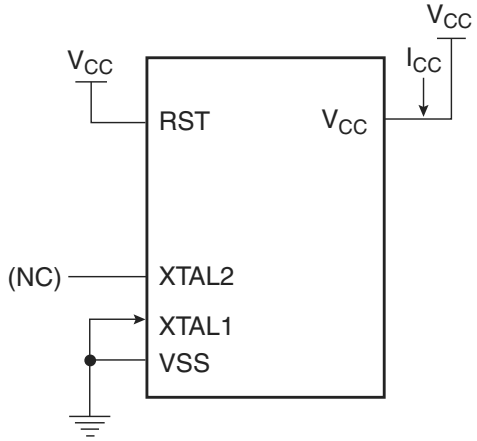

### 24.7.4 $I_{CC}$ Test Condition, Idle Mode, All Other Pins are Disconnected




### 24.7.5 Clock Signal Waveform for $I_{CC}$ Tests in Active and Idle Modes, $t_{CLCH} = t_{CHCL} = 5$ ns




### 24.7.6 $I_{CC}$ Test Condition, Power-down Mode, All Other Pins are Disconnected, $V_{CC}$ = 2V to 5.5V



# 25. Ordering Information

## 25.1 Green Package Option (Pb/Halide-free)

| Speed (MHz) | Power Supply | Ordering Code | Package | Operation Range |
|---|---|---|---|---|
| 20 | 2.4V to 5.5V | AT89LP213-20PU<br>AT89LP213-20XU | 14P3<br>14X | Industrial (-40° C to 85° C) |
| | | AT89LP214-20PU<br>AT89LP214-20XU | 14P3<br>14X | |

| Package Type | |
|---|---|
| **14P3** | 14-lead, 0.300” Wide, Plastic Dual In-line Package (PDIP) |
| **14X** | 14-lead, 0.173” Wide, Plastic Thin Shrink Small Outline Package (TSSOP) |

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