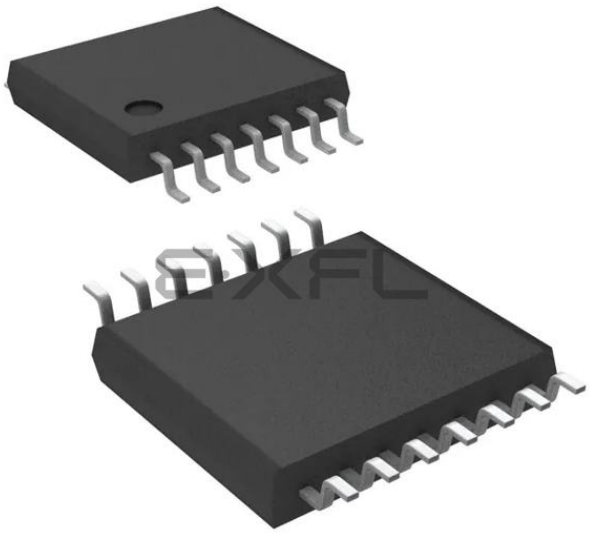

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89lp214-20xu

need only 1 to 4 clock cycles providing 6 to 12 times more throughput than the standard 8051. Seventy percent of instructions need only as many clock cycles as they have bytes to execute, and most of the remaining instructions require only one additional clock. The enhanced CPU core is capable of 20 MIPS throughput whereas the classic 8051 CPU can deliver only 4 MIPS at the same current consumption. Conversely, at the same throughput as the classic 8051, the new CPU core runs at a much lower speed and thereby greatly reduces power consumption.

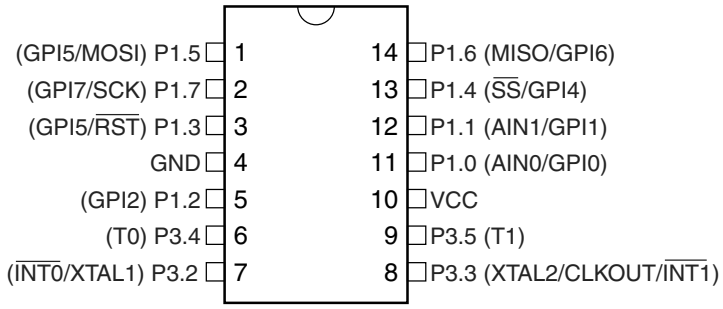
The AT89LP213/214 provides the following standard features: 2K bytes of In-System Programmable Flash memory, 128 bytes of RAM, up to 12 I/O lines, two 16-bit timer/counters, two PWM outputs (AT89LP213 only), a programmable watchdog timer, a full duplex serial port (AT89LP214 only), a serial peripheral interface, an internal 8 MHz RC oscillator, on-chip crystal oscillator, and a four-level, six-vector interrupt system.

The two timer/counters in the AT89LP213/214 are enhanced with two new modes. Mode 0 can be configured as a variable 9- to 16-bit timer/counter and Mode 1 can be configured as a 16-bit auto-reload timer/counter. In addition, the timer/counters on the AT89LP213 may independently drive a pulse width modulation output.

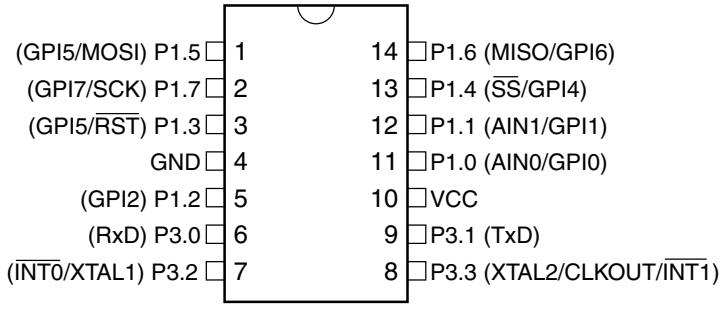
The I/O ports of the AT89LP213/214 can be independently configured in one of four operating modes. In quasi-bidirectional mode, the ports operate as in the classic 8051. In input mode, the ports are tristated. Push-pull output mode provides full CMOS drivers and open-drain mode provides just a pull-down. In addition, all 8 pins of Port 1 can be configured to generate an interrupt using the general-purpose interrupt interface. The I/O pins of the AT89LP213/214 tolerate voltages higher than the device's own power supply, up to 5.5V. When the device is supplied at 2.4V and all I/O ports receive 5.5V, the total back flowing current in all I/Os is less than 100 µA.

2. Pin Configuration

2.1 AT89LP213: 14-lead TSSOP/PDIP



2.2 AT89LP214: 14-lead TSSOP/PDIP



3. Pin Description

Table 3-1. **AT89LP213** Pin Description

Pin	Symbol	Type	Description
1	P1.5	I/O I/O I	**P1.5**: User-configurable I/O Port 1 bit 5. **MOSI**: SPI master-out/slave-in. When configured as master, this pin is an output. When configured as slave, this pin is an input. **GPI5**: General-purpose Interrupt input 5.
2	P1.7	I/O I/O I	**P1.7**: User-configurable I/O Port 1 bit 7. **SCK**: SPI Clock. When configured as master, this pin is an output. When configured as slave, this pin is an input. **GPI7**: General-purpose Interrupt input 7.
3	P1.3	I/O I I I	**P1.3**: User-configurable I/O Port 1 bit 3 (if Reset Fuse is disabled). **$\overline{\text{RST}}$**: External **Active-Low** Reset input (if Reset Fuse is enabled. See “External Reset” on page 16). **GPI3**: General-purpose Interrupt input 3. **DCL**: Serial Clock input for On-chip Debug Interface when OCD is enabled.
4	GND	I	Ground
5	P1.2	I/O I	**P1.2**: User-configurable I/O Port 1 bit 2. **GPI2**: General-purpose Interrupt input 2.
6	P3.4	I/O I/O	**P3.4**: User-configurable I/O Port 3 bit 4. **T0**: Timer/Counter 0 External Input or PWM Output.
7	P3.2	I/O I I/O	**P3.2**: User-configurable I/O Port 3 bit 2. **XTAL1**: Input to the inverting oscillator amplifier and internal clock generation circuits. It may be used as a port pin if the internal RC oscillator is selected as the clock source. **DDA**: Serial Data input/output for On-chip Debug Interface when OCD is enabled and the internal RC oscillator is selected as the clock source.
8	P3.3	I/O O O I/O	**P3.3**: User-configurable I/O Port 3 bit 3. **XTAL2**: Output from inverting oscillator amplifier. It may be used as a port pin if the internal RC oscillator is selected as the clock source. **CLKOUT**: When the internal RC oscillator is selected as the clock source, may be used to output the internal clock divided by 2. **DDA**: Serial Data input/output for On-chip Debug Interface when OCD is enabled and the external clock is selected as the clock source.
9	P3.5	I/O I/O	**P3.5**: User-configurable I/O Port 3 bit 5. **T1**: Timer/Counter 1 External input or PWM output.
10	VCC	I	Supply Voltage
11	P1.0	I/O I I	**P1.0**: User-configurable I/O Port 1 bit 0. **AIN0**: Analog Comparator Positive input. **GPI0**: General-purpose Interrupt input 0.
12	P1.1	I/O I I	**P1.1**: User-configurable I/O Port 1 bit 1. **AIN1**: Analog Comparator Negative input. **GPI1**: General-purpose Interrupt input 1
13	P1.4	I/O I I	**P1.4**: User-configurable I/O Port 1 bit 4. **$\overline{\text{SS}}$**: SPI slave select input. **GPI4**: General-purpose Interrupt input 4.
14	P1.6	I/O I/O I	**P1.6**: User-configurable I/O Port 1 bit 6. **MISO**: SPI master-in/slave-out. When configured as master, this pin is an input. When configured as slave, this pin is an output. **GPI6**: General-purpose Interrupt input 6.

4. Block Diagram

Figure 4-1. AT89LP213 Block Diagram

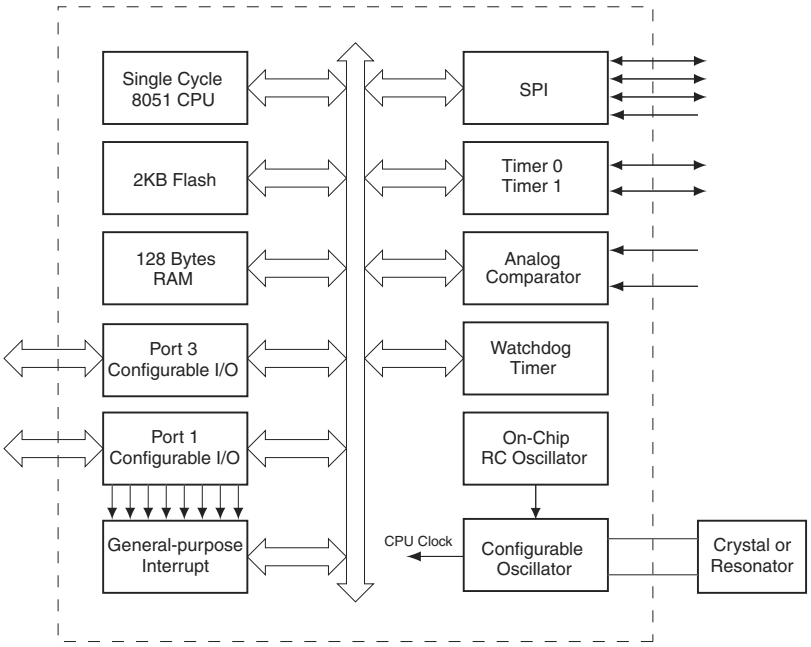
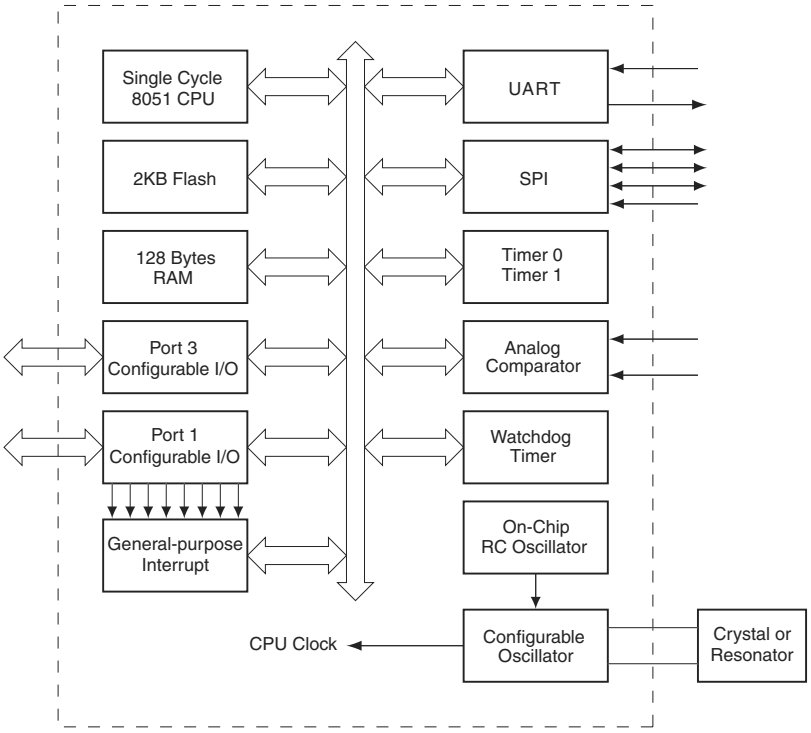


Figure 4-2. AT89LP214 Block Diagram



7. Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 7-1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect. User software should not write to these unlisted locations, since they may be used in future products to invoke new features.

Table 7-1. AT89LP213/214 SFR Map and Reset Values

	8	9	A	B	C	D	E	F	
0F8H									0FFH
0F0H	B 0000 0000								0F7H
0E8H	SPSR 000x x000	SPCR 0000 0000	SPDR xxxx xxxx						0EFH
0E0H	ACC 0000 0000								0E7H
0D8H									0DFH
0D0H	PSW 0000 0000								0D7H
0C8H									0CFH
0C0H			P1M0[2]	P1M1 xx00 0000			P3M0[2]	P3M1 xx00 0000	0C7H
0B8H	IP x000 0000	SADEN 0000 0000							0BFH
0B0H	P3 xx11 1111							IPH x000 0000	0B7H
0A8H	IE 0000 0000	SADDR 0000 0000							0AFH
0A0H			AUXR1 xxxx 0xxx				WDTRST (write-only)	WDTCON 0000 x000	0A7H
98H	SCON 0000 0000	SBUF xxxx xxxx	GPMOD 0000 0000	GPLS 0000 0000	GPIEN 0000 0000	GPIF 0000 0000			9FH
90H	P1 1111 1111	TCONB 0010 0100	RL0 0000 0000	RL1 0000 0000	RH0 0000 0000	RH1 0000 0000		ACSR xx00 0000	97H
88H	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000		CLKREG 0000 x000	8FH
80H		SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 0000 0000	87H
	0	1	2	3	4	5	6	7	

Notes: 1. All SFRs in the left-most column are bit-addressable.

2. Reset value is xx11 1111B when Tristate-Port Fuse is enabled and xx00 0000B when disabled.

Table 9-2. CLKREG – Clock Control Register

CLKREG = 8FH — Reset Value = 0000 0000B

Not Bit Addressable

	TPS3	TPS2	TPS1	TPS0	–	CDV1	CDV0	COE
Bit	7	6	5	4	3	2	1	0

Symbol	Function
TPS3 TPS2 TPS1 TPS0	Timer Prescaler. The Timer Prescaler selects the time base for Timer 0, Timer 1 and the Watchdog Timer. The prescaler is implemented as a 4-bit binary down counter. When the counter reaches zero it is reloaded with the value stored in the TPS bits to give a division ratio between 1 and 16. By default the timers will count every clock cycles (TPS = 0000B). To configure the timers to count at a standard 8051 rate of once every 12 clock cycles, TPS should be set to 1011B.
CDV1 CDV0	Clock Out Division. Determines the frequency of the clock output relative to the system clock. CDIV1 CDIV0 Clock Out Frequency 0 0 f/2 0 1 f/4 1 0 f/8 1 1 f/16
COE	Clock Out Enable. Set COE to output a divided version of the system clock on XTAL2 (P3.3). The internal RC oscillator or external clock source must be selected in order to use this feature.

10. Reset

During reset, all I/O Registers are set to their initial values, the port pins are tristated, and the program starts execution from the Reset Vector, 0000H. The AT89LP213/214 has five sources of reset: power-on reset, brown-out reset, external reset, watchdog reset, and software reset.

10.1 Power-on Reset

A Power-on Reset (POR) is generated by an on-chip detection circuit. The detection level is nominally 1.4V. The POR is activated whenever V_{CC} is below the detection level. The POR circuit can be used to trigger the start-up reset or to detect a supply voltage failure in devices without a brown-out detector. The POR circuit ensures that the device is reset from power-on. A power-on sequence is shown in Figure 10-1 on page 15. When V_{CC} reaches the Power-on Reset threshold voltage V_{POR}, an initialization sequence lasting t_{POR} is started. When the initialization sequence completes, the start-up timer determines how long the device is kept in POR after V_{CC} rise. The POR signal is activated again, without any delay, when V_{CC} falls below the POR threshold level. A Power-on Reset (i.e. a cold reset) will set the POF flag in PCON. The internally generated reset can be extended beyond the power-on period by holding the $\overline{RST}$ pin low longer than the time-out.

Table 12-2. IE – Interrupt Enable Register

IE = A8H — Reset Value = 0000 0000B

Bit Addressable

	EA	EC	EGP	ES	ET1	EX1	ET0	EX0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
EA	Global enable/disable. All interrupts are disabled when EA = 0. When EA = 1, each interrupt source is enabled/disabled by setting /clearing its own enable bit.
EC	Comparator Interrupt Enable
EGP	General-purpose Interrupt Enable
ES	Serial Port Interrupt Enable
ET1	Timer 1 Interrupt Enable
EX1	External Interrupt 1 Enable
ET0	Timer 0 Interrupt Enable
EX0	External Interrupt 0 Enable

Table 12-3. IP – Interrupt Priority Register

IP = B8H — Reset Value = X000 0000B

Bit Addressable

	–	–	PGP	PS	PT1	PX1	PT0	PX0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
PGP	General-purpose Interrupt Priority Low
PS	Serial Port Interrupt Priority Low
PT1	Timer 1 Interrupt Priority Low
PX1	External Interrupt 1 Priority Low
PT0	Timer 0 Interrupt Priority Low
PX0	External Interrupt 0 Priority Low

14.5.4 Mode 3 – Split 8-bit PWM

Timer 1 in PWM Mode 3 simply holds its count. The effect is the same as setting TR1 = 0. Timer 0 in PWM Mode 3 establishes TL0 and TH0 as two separate PWM counters in a manner similar to normal Mode 3. PWM Mode 3 on Timer 0 is shown in Figure 14-10. Only the Timer Prescaler is available to change the output frequency during PWM Mode 3. TL0 can use the Timer 0 control bits: GATE, TR0, $\overline{\text{INT0}}$, PWM0EN and TF0. TH0 is locked into a timer function and uses TR1, PWM1EN and TF1. RL0 provides the duty cycle for TL0 and RH0 provides the duty cycle for TH0.

PWM Mode 3 is for applications requiring a single PWM channel and two timers, or two PWM channels and an extra timer or counter. With Timer 0 in PWM Mode 3, the AT89LP213 can appear to have three Timer/Counters. When Timer 0 is in PWM Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3. In this case, Timer 1 can still be used by the serial port as a baud rate generator or in any application not requiring an interrupt. The following formulas give the output frequency and duty cycle for Timer 0 in PWM Mode 3.

$$\text{Mode 3:} \qquad f_{out} = \frac{\text{Oscillator Frequency}}{256} \times \frac{1}{\text{TPS} + 1}$$

$$\text{Mode 3, T0:} \qquad \text{Duty Cycle \%} = 100 \times \frac{\text{RL0}}{256}$$

$$\text{Mode 3, T1:} \qquad \text{Duty Cycle \%} = 100 \times \frac{\text{RH0}}{256}$$

Figure 14-10. Timer/Counter 0 PWM Mode 3

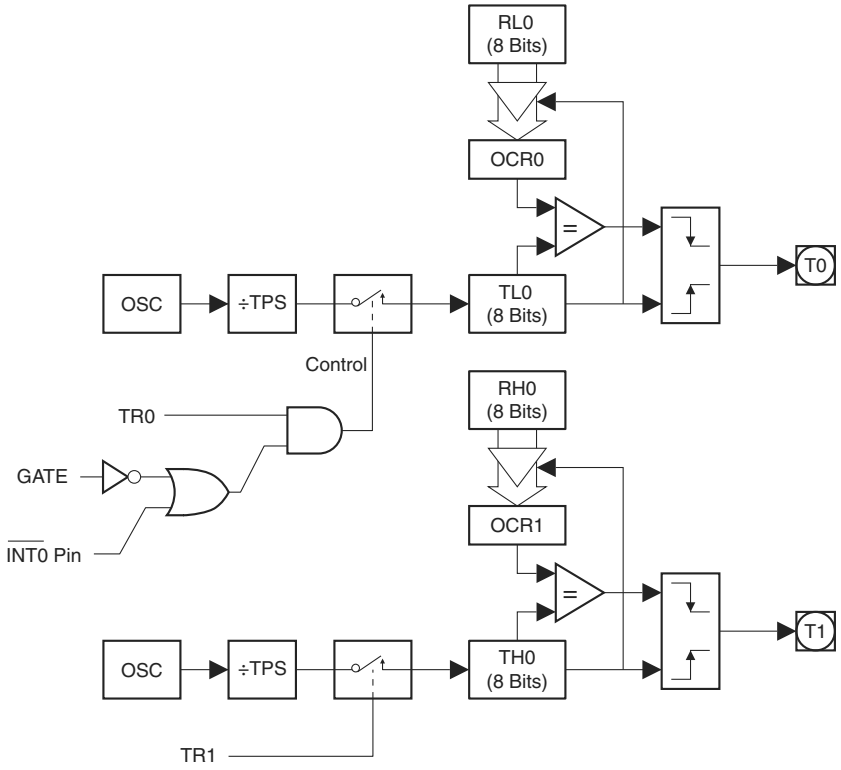


Table 16-2. GPLS – General-purpose Interrupt Level Select Register

GPLS = 9BH — Reset Value = 0000 0000B

Not Bit Addressable

	GPLS7	GPLS6	GPLS5	GPLS4	GPLS3	GPLS2	GPLS1	GPLS0
Bit	7	6	5	4	3	2	1	0

GPMOD.x 0 = detect low level or negative edge on P1.x

1 = detect high level or positive edge on P1.x

Table 16-3. GPIEN – General-purpose Interrupt Enable Register

GPIEN = 9CH — Reset Value = 0000 0000B

Not Bit Addressable

	GPIEN7	GPIEN6	GPIEN5	GPIEN4	GPIEN3	GPIEN2	GPIEN1	GPIEN0
Bit	7	6	5	4	3	2	1	0

GPIEN.x 0 = interrupt for P1.x disabled

1 = interrupt for P1.x enabled

Table 16-4. GPIF – General-purpose Interrupt Flag Register

GPIF = 9DH — Reset Value = 0000 0000B

Not Bit Addressable

	GPIF7	GPIF6	GPIF5	GPIF4	GPIF3	GPIF2	GPIF1	GPIF0
Bit	7	6	5	4	3	2	1	0

GPIF.x 0 = interrupt on P1.x inactive

1 = interrupt on P1.x active. Must be cleared by software.

17. Serial Interface

The serial interface on the AT89LP214 implements a Universal Asynchronous Receiver/Transmitter (UART). The UART has the following features:

- Full Duplex Operation
- 8 or 9 Data Bits
- Framing Error Detection
- Multiprocessor Communication Mode with Automatic Address Recognition
- Baud Rate Generator Using Timer 1
- Interrupt on Receive Buffer Full or Transmission Complete

The serial interface is full duplex, which means it can transmit and receive simultaneously. It is also receive-buffered, which means it can begin receiving a second byte before a previously received byte has been read from the receive register. (However, if the first byte still has not been read when reception of the second byte is complete, one of the bytes will be lost.) The serial port receive and transmit registers are both accessed at the Special Function Register SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register. The serial port can operate in the following four modes.

- **Mode 0:** Serial data enters and exits through RXD. TXD outputs the shift clock. Eight data bits are transmitted/received, with the LSB first. The baud rate is fixed at 1/2 the oscillator frequency.
- **Mode 1:** 10 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in the Special Function Register SCON. The baud rate is variable based on Timer 1.
- **Mode 2:** 11 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmit, the 9th data bit (TB8 in SCON) can be assigned the value of “0” or “1”. For example, the parity bit (P, in the PSW) can be moved into TB8. On receive, the 9th data bit goes into RB8 in the Special Function Register SCON, while the stop bit is ignored. The baud rate is programmable to either 1/16 or 1/32 the oscillator frequency.
- **Mode 3:** 11 bits are transmitted (through TXD) or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). In fact, Mode 3 is the same as Mode 2 in all respects except the baud rate, which is variable based on Timer 1 in Mode 3.

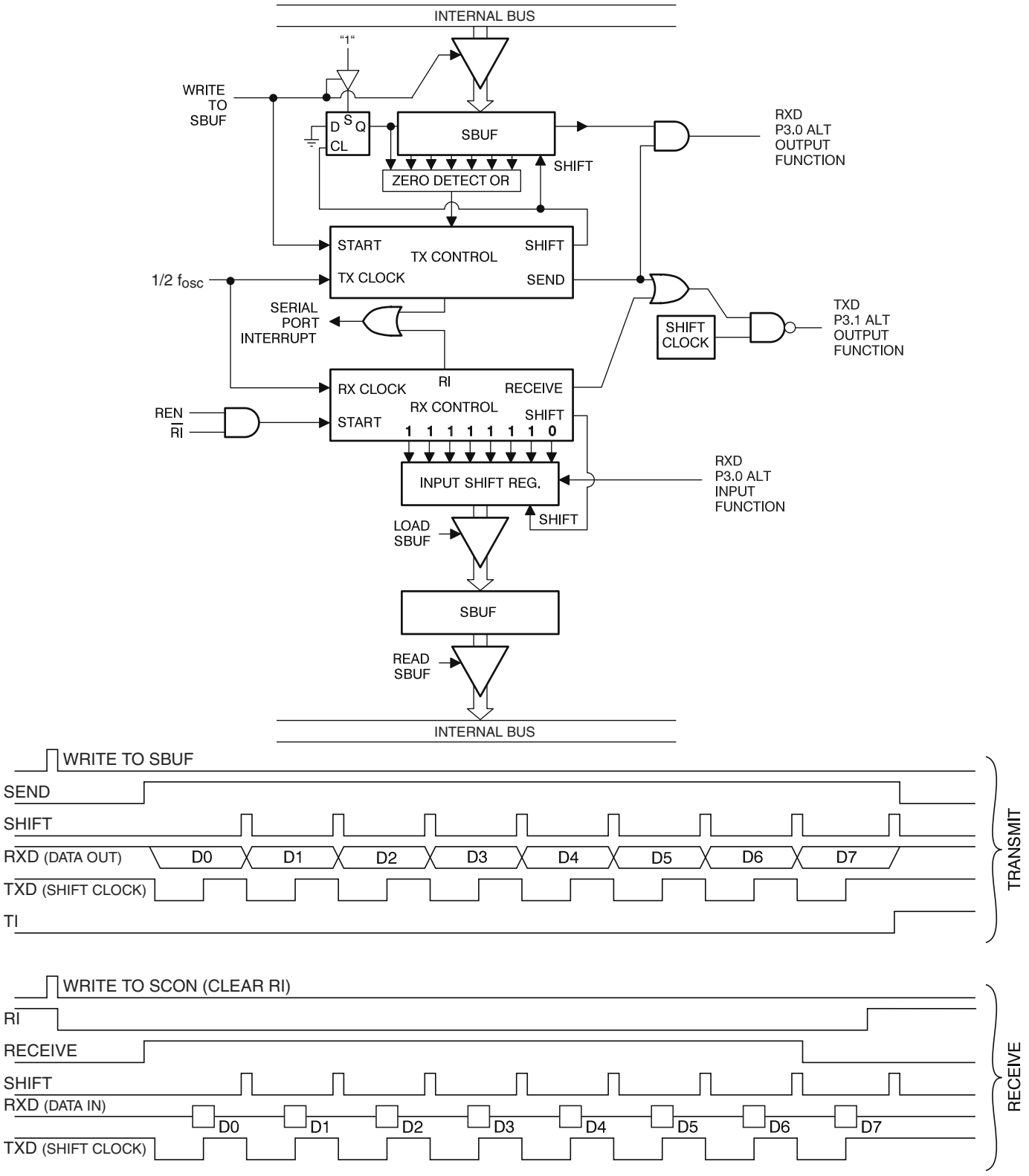
In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

17.1 Multiprocessor Communications

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received, followed by a stop bit. The 9th bit goes into RB8. Then comes a stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt is activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON.

The following example shows how to use the serial interrupt for multiprocessor communications. When the master processor must transmit a block of data to one of several slaves, it first sends out an address byte that identifies the target slave. An address byte differs from a data byte in that the 9th bit is “1” in an address byte and “0” in a data byte. With SM2 = 1, no slave is interrupted by a data byte. An address byte, however, interrupts all slaves. Each slave can examine the received byte and see if it is being addressed. The addressed slave clears its SM2

Figure 17-1. Serial Port Mode 0



19. Analog Comparator

A single analog comparator is provided on the AT89LP213/214. The analog comparator has the following features:

- Comparator Output Flag and Interrupt
- Selectable Interrupt Condition
  - High- or Low-level
  - Rising- or Falling-edge
  - Output Toggle
- Hardware Debouncing Modes

Comparator operation is such that the output is a logic “1” when the positive input AIN0 (P1.0]) is greater than the negative input AIN1 (P1.1). Otherwise the output is a zero. Setting the CEN bit in ACSR enables the comparator. When the comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 µs. The corresponding comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service. Before enabling the comparator the analog inputs should be tristated by putting P1.0 and P1.1 into input-only mode. See “Port 1 Analog Functions” on page 26.

The comparator may be configured to cause an interrupt under a variety of output value conditions by setting the CM bits in ACSR. The comparator interrupt flag CF in ACSR is set whenever the comparator output matches the condition specified by CM. The flag may be polled by software or may be used to generate an interrupt and must be cleared by software.

19.1 Comparator Interrupt with Debouncing

The comparator output is sampled every clock cycle. The conditions on the analog inputs may be such that the comparator output will toggle excessively. This is especially true if applying slow moving analog inputs. Three debouncing modes are provided to filter out this noise. In debouncing mode, the comparator uses Timer 1 to modulate its sampling time. When a relevant transition occurs, the comparator waits until two Timer 1 overflows have occurred before resampling the output. If the new sample agrees with the expected value, CF is set. Otherwise, the event is ignored. The filter may be tuned by adjusting the time-out period of Timer 1. Because Timer 1 is free running, the debouncer must wait for two overflows to guarantee that the sampling delay is at least 1 time-out period. Therefore, after the initial edge event, the interrupt may occur between 1 and 2 time-out periods later. See Figure 19-1 on page 57.

By default the comparator is disabled during Idle mode. To allow the comparator to function during Idle, the CIDL bit is ACSR must be set. When CIDL is set, the comparator can be used to wake-up the CPU from Idle if the comparator interrupt is enabled. The comparator is always disabled during Power-down mode.

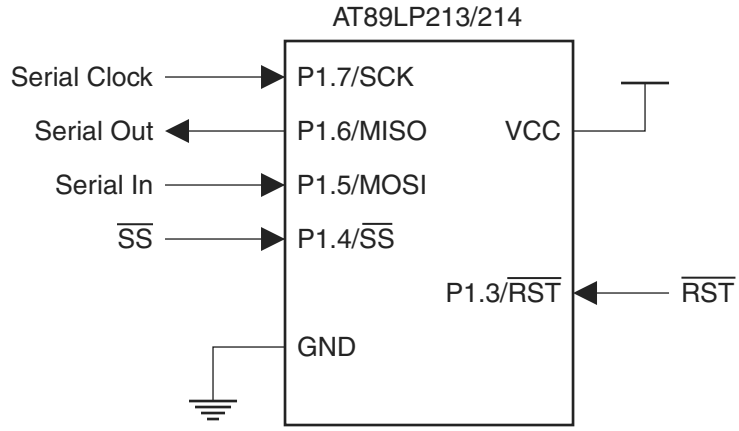
- Flexible Page Programming
- Row Erase Capability
- Page Write with Auto-Erase Commands
- Programming Status Register

For more detailed information on In-System Programming, refer to the Application Note entitled “AT89LP In-System Programming Specification”.

23.1 Physical Interface

In-System Programming utilizes the Serial Peripheral Interface (SPI) pins of an AT89LP213/214 microcontroller. The SPI is a full duplex synchronous serial interface consisting of four wires: Serial Clock (SCK), Master-In/Slave-out (MISO), Master-out/Slave-in (MOSI), and an active-low Slave Select ($\overline{SS}$). When programming an AT89LP213/214 device, the programmer always operates as the SPI master, and the target system always operates as the SPI slave. To enter or remain in In-System Programming mode the device’s reset line ($\overline{RST}$) must be held active (low). With the addition of VCC and GND, an AT89LP213/214 microcontroller can be programmed with a minimum of seven connections as shown in Figure 23-1.

Figure 23-1. In-System Programming Device Connections



The In-System Programming Interface is the only means of externally programming the AT89LP213/214 microcontroller. The ISP Interface can be used to program the device both in-system and in a stand-alone serial programmer. The ISP Interface does not require any clock other than SCK and is not limited by the system clock frequency. During In-System programming the system clock source of the target device can operate normally.

When designing a system where In-System Programming will be used, the following observations must be considered for correct operation:

- The ISP interface uses the SPI clock mode 0 (CPOL = 0,CPHA = 0) exclusively with a maximum frequency of 5 MHz.
- The AT89LP213/214 will enter programming mode only when its reset line ($\overline{RST}$) is active (low). To simplify this operation, it is recommended that the target reset can be controlled by the In-System programmer. To avoid problems, the In-System programmer should be able to keep the entire target system reset for the duration of the programming cycle. The target system should never attempt to drive the four SPI lines while reset is active.
- The $\overline{RST}$ input may be disabled to gain an extra I/O pin. In these cases the $\overline{RST}$ pin will always function as a reset during power up. To enter programming the $\overline{RST}$ pin must be

24.3.4 Quasi-Bidirectional Output

Figure 24-6. Quasi-Bidirectional Output I-V Characteristic at 5V

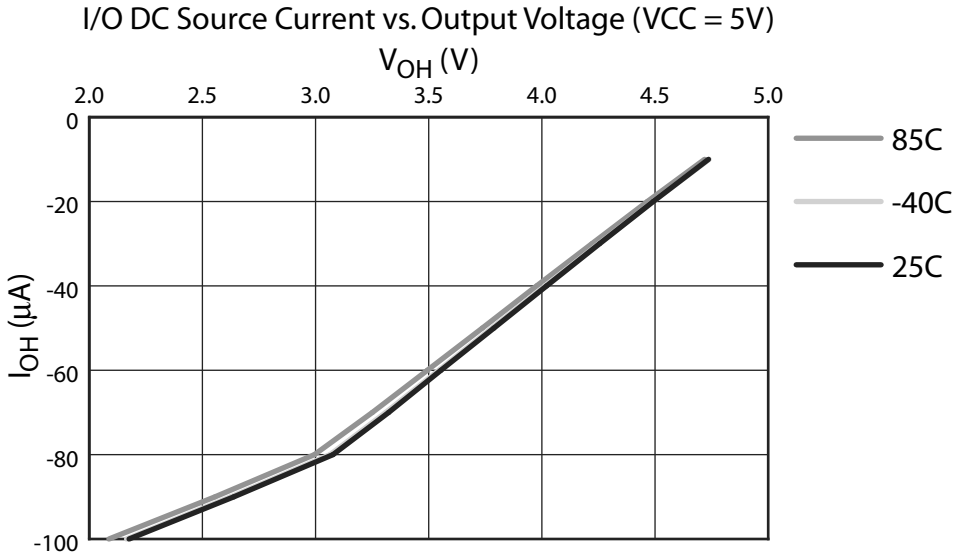


Figure 24-7. Quasi-Bidirectional Output I-V Characteristic at 3V

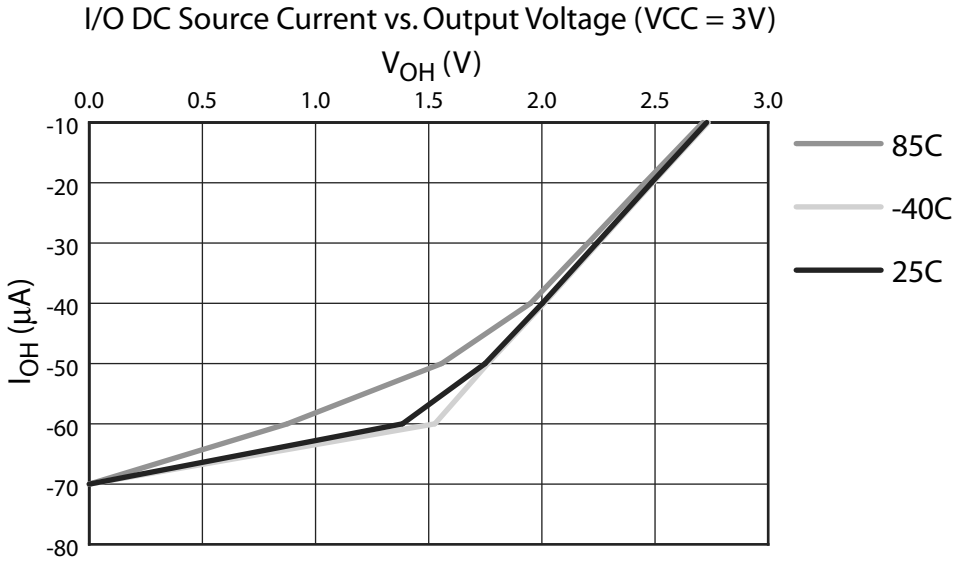


Figure 24-13. SPI Master Timing (CPHA = 0)

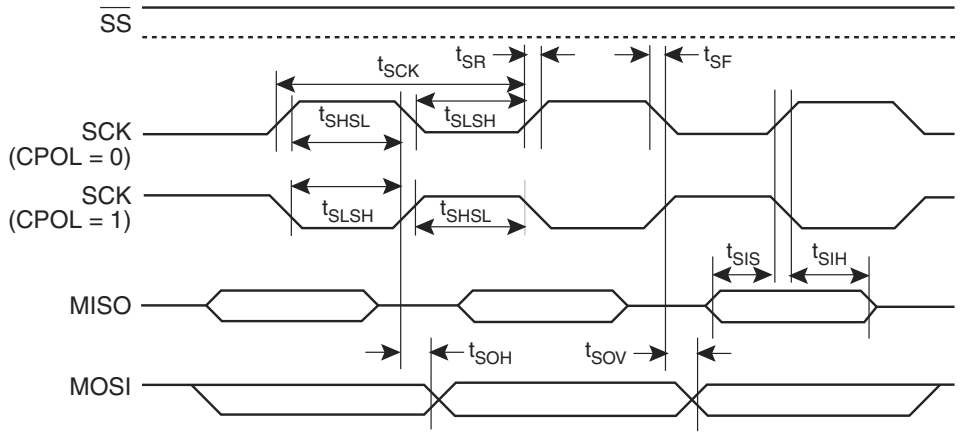


Figure 24-14. SPI Slave Timing (CPHA = 0)

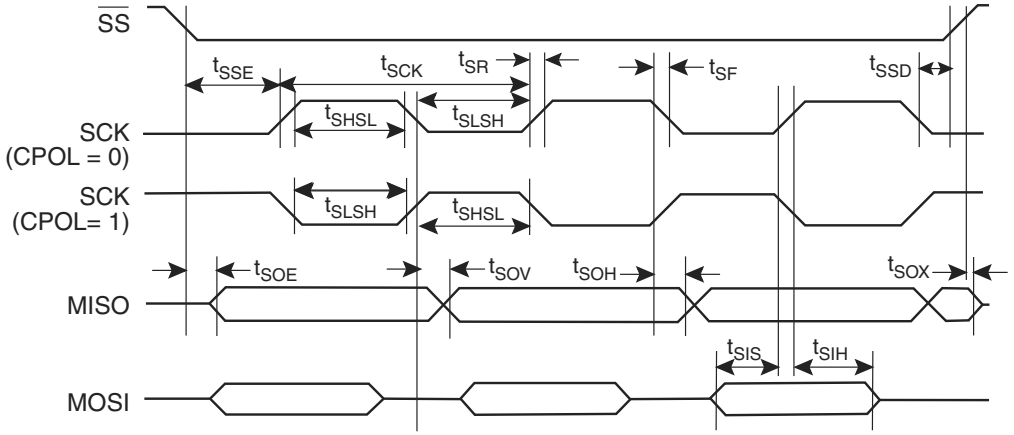
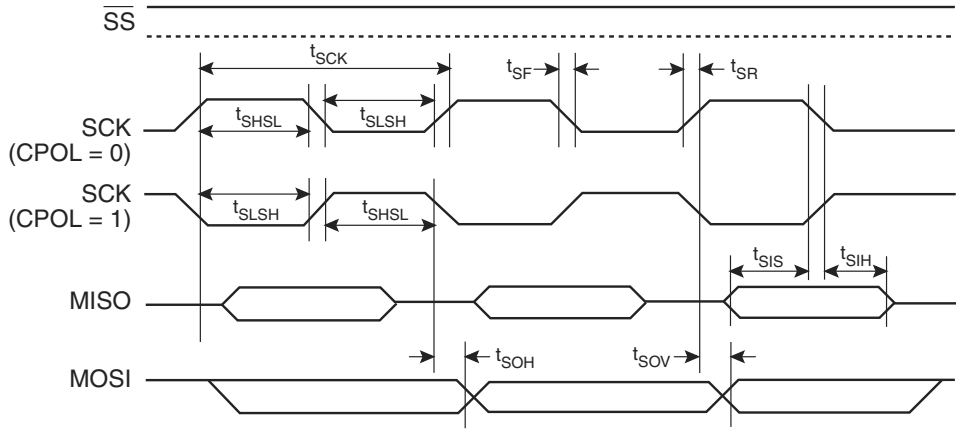
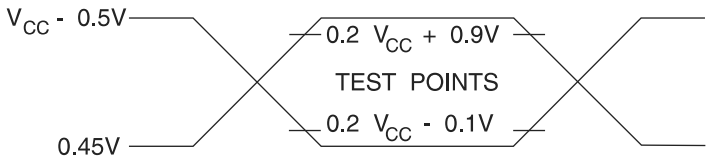


Figure 24-15. SPI Master Timing (CPHA = 1)



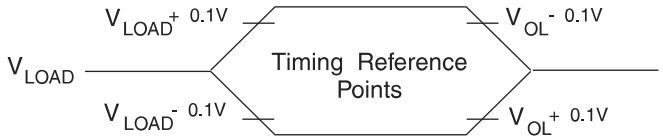
24.7 Test Conditions

24.7.1 AC Testing Input/Output Waveform[1]



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic “1” and 0.45V for a logic “0”. Timing measurements are made at V_{IH} min. for a logic “1” and V_{IL} max. for a logic “0”.

24.7.2 Float Waveform[1]



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

25. Ordering Information

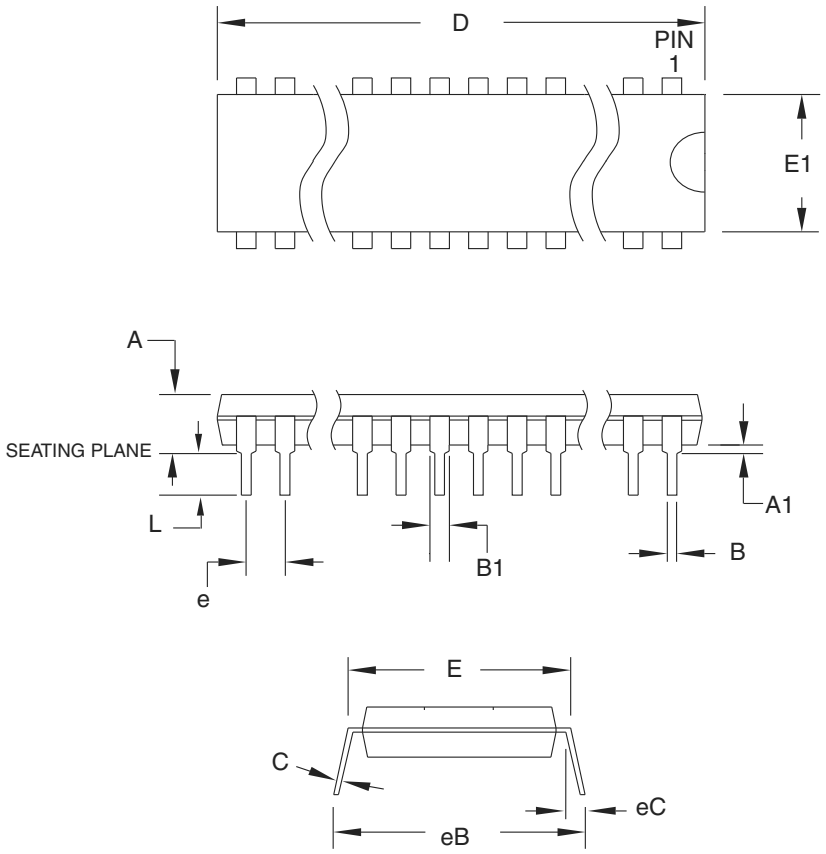
25.1 Green Package Option (Pb/Halide-free)

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
20	2.4V to 5.5V	AT89LP213-20PU AT89LP213-20XU	14P3 14X	Industrial (-40° C to 85° C)
		AT89LP214-20PU AT89LP214-20XU	14P3 14X	

Package Type	
14P3	14-lead, 0.300” Wide, Plastic Dual In-line Package (PDIP)
14X	14-lead, 0.173” Wide, Plastic Thin Shrink Small Outline Package (TSSOP)

26. Packaging Information

26.1 14P3 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	5.334	
A1	0.381	–	–	
D	18.669	–	19.685	Note 2
E	7.620	–	8.255	
E1	6.096	–	7.112	Note 2
B	0.356	–	0.559	
B1	1.143	–	1.778	
L	2.921	–	3.810	
C	0.203	–	0.356	
eB	–	–	10.922	
eC	0.000	–	1.524	
e	2.540 TYP			

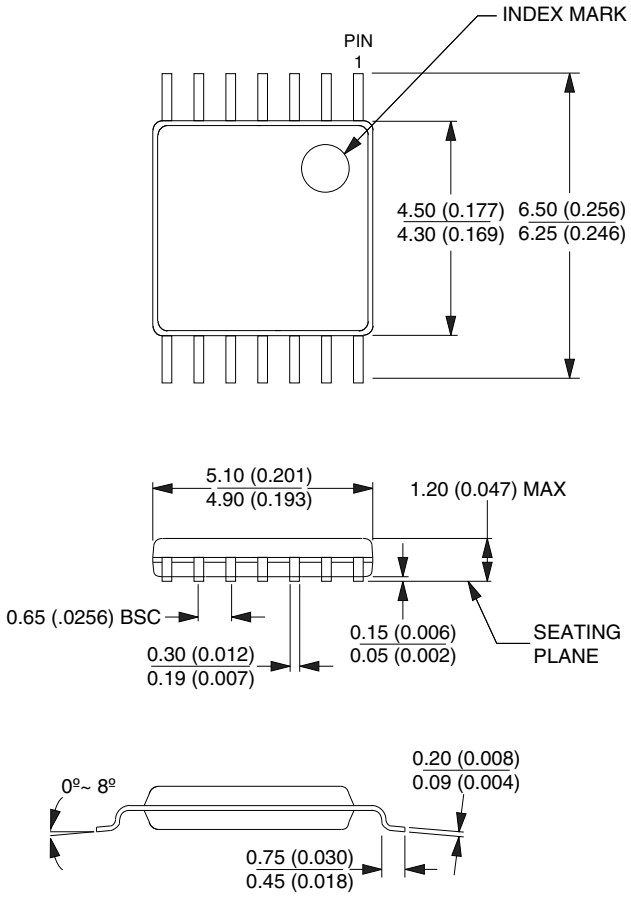
Notes: 1. This package conforms to JEDEC reference MS-001, Variation AA.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

11/02/05

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**14P3**, 14-lead (0.300"/7.62 mm Wide) Plastic Dual Inline Package (PDIP)	14P3	A

26.2 14X – TSSOP

Dimensions in Millimeters and (Inches).
Controlling dimension: Millimeters.
JEDEC Standard MO-153 AB-1.



05/16/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**14X (Formerly "14T")**, 14-lead (4.4 mm Body) Thin Shrink Small Outline Package (TSSOP)	14X	B

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