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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | Coldfire V1 |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | EBI/EMI, I²C, SPI, UART/USART, USB OTG |
| Peripherals | DMA, I²S, LVD, POR, PWM, WDT |
| Number of I/O | 48 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 17x12b; D/A 1x12b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51jf128vlh |

# Table of Contents

| Field | Description | Values |
|---|---|---|
| | | • 64 = 64 KB<br>• 128 = 128 KB |
| T | Temperature range, ambient (°C) | V = –40 to 105 |
| PP | Package identifier | • FM = 32 QFN (5 mm x 5 mm)<br>• HS = 44 Laminate QFN (5 mm x 5 mm)<br>• LF = 48 LQFP (7 mm x 7 mm)<br>• LH = 64 LQFP (10 mm x 10 mm) |

1. All parts also have FlexNVM, FlexRAM, and RAM.

## 2.4 Example

This is an example part number:

MCF51JF128VLH

# 3 Terminology and guidelines

## 3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

### 3.1.1 Example

This is an example of an operating requirement:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | 1.0 V core supply voltage | 0.9 | 1.1 | V |

## 3.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Digital supply voltage | –0.3 | 3.8 | V |
| $I_{DD}$ | Digital supply current | — | 120 | mA |
| $V_{DIO}$ | Digital input voltage (except $\overline{RESET}$, EXTAL, and XTAL) | –0.3 | $V_{DD}$ + 0.3 | V |
| $V_{AIO}$ | Analog, $\overline{RESET}$, EXTAL, and XTAL input voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| $I_D$ | Instantaneous maximum current single pin limit (applies to all port pins) | –25 | 25 | mA |
| $V_{DDA}$ | Analog supply voltage | $V_{DD}$ – 0.3 | $V_{DD}$ + 0.3 | V |
| $V_{USB\_DP}$ | USB_DP input voltage | –0.3 | 3.63 | V |
| $V_{USB\_DM}$ | USB_DM input voltage | –0.3 | 3.63 | V |
| VREGIN | USB Regulator input | –0.3 | 6.0 | V |

# 5 General

## 5.1 Typical Value Conditions

Typical values assume you meet the following conditions (or other conditions as specified):

| Symbol | Description | Value | Unit |
|---|---|---|---|
| $T_A$ | Ambient temperature | 25 | °C |
| $V_{DD}$ | 3.3 V supply voltage | 3.3 | V |

## 5.2 Nonswitching electrical specifications

### 5.2.1 Voltage and Current Operating Requirements

**Table 1. Voltage and current operating requirements**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | 3.6 | V | |
| $V_{DDA}$ | Analog supply voltage | 1.71 | 3.6 | V | |
| $V_{DD} – V_{DDA}$ | $V_{DD}$-to-$V_{DDA}$ differential voltage | –0.1 | 0.1 | V | |
| $V_{SS} – V_{SSA}$ | $V_{SS}$-to-$V_{SSA}$ differential voltage | –0.1 | 0.1 | V | |
| $V_{IH}$ | Input high voltage | 0.7 × $V_{DD}$ | — | V | 1 |
| | | 0.75 × $V_{DD}$ | — | V | |

*Table continues on the next page...*

**Table 2. LVD and POR operating requirements (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{LVDL}$ | Falling low-voltage detect threshold — low range (LVDV=00) | 1.54 | 1.60 | 1.66 | V | |
| $V_{LVW1L}$<br>$V_{LVW2L}$<br>$V_{LVW3L}$<br>$V_{LVW4L}$ | Low-voltage warning thresholds — low range<br>• Level 1 falling (LVWV=00)<br>• Level 2 falling (LVWV=01)<br>• Level 3 falling (LVWV=10)<br>• Level 4 falling (LVWV=11) | 1.74<br>1.84<br>1.94<br>2.04 | 1.80<br>1.90<br>2.00<br>2.10 | 1.86<br>1.96<br>2.06<br>2.16 | V<br>V<br>V<br>V | 1 |
| $V_{HYSL}$ | Low-voltage inhibit reset/recover hysteresis — low range | — | ±60 | — | mV | |
| $V_{BG}$ | Bandgap voltage reference | 0.97 | 1.00 | 1.03 | V | |
| $t_{LPO}$ | Internal low power oscillator period<br>factory trimmed | 900 | 1000 | 1100 | µs | |

1. Rising thresholds are falling threshold + hysteresis voltage

## 5.2.3 Voltage and current operating behaviors

**Table 3. Voltage and current operating behaviors**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{OH}$ | Output high voltage — high drive strength | | | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OH}$ = - 9 mA | $V_{DD}$ – 0.5 | — | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OH}$ = -3 mA | $V_{DD}$ – 0.5 | — | V | |
| | Output high voltage — low drive strength | | | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OH}$ = -2 mA | $V_{DD}$ – 0.5 | — | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OH}$ = -0.6 mA | $V_{DD}$ – 0.5 | — | V | |
| $I_{OHT}$ | Output high current total for all ports | — | 100 | mA | |
| $V_{OL}$ | Output low voltage — high drive strength | | | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL}$ = 9 mA | — | 0.5 | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OL}$ = 3 mA | — | 0.5 | V | |
| | Output low voltage — low drive strength | | | | |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL}$ = 2 mA | — | 0.5 | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OL}$ = 0.6 mA | — | 0.5 | V | |
| $I_{OLT}$ | Output low current total for all ports | — | 100 | mA | |
| $I_{IN}$ | Input leakage current (per pin) | | | | |
| | • @ full temperature range | — | 1.0 | µA | 1 |
| | • @ 25 °C | — | 0.1 | µA | |

*Table continues on the next page...*

**Table 3. Voltage and current operating behaviors (continued)**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $I_{OZ}$ | Hi-Z (off-state) leakage current (per pin) | — | 1 | μA | |
| $I_{OZ}$ | Total Hi-Z (off-state) leakage current (all input pins) | — | 4 | μA | |
| $R_{PU}$ | Internal pullup resistors | 22 | 50 | kΩ | 2 |
| $R_{PD}$ | Internal pulldown resistors | 22 | 50 | kΩ | 3 |

1. Tested by ganged leakage method
2. Measured at Vinput = $V_{SS}$
3. Measured at Vinput = $V_{DD}$

## 5.2.4 Power mode transition operating behaviors

All specifications except $t_{POR}$ and VLLSx-RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 50 MHz
- Bus clock (and flash and Mini-FlexBus clocks) = 25 MHz

**Table 4. Power mode transition operating behaviors**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $t_{POR}$ | After a POR event, amount of time from the point $V_{DD}$ reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.<br>• 1.71 V/($V_{DD}$ slew rate) ≤ 300 μs<br>• 1.71 V/($V_{DD}$ slew rate) > 300 μs | — | 300 1.71 V/($V_{DD}$ slew rate) | μs | 1 |
| | • VLLS1 → RUN | — | 132 | μs | 1, 2 |
| | • VLLS2 → RUN | — | 92 | μs | 1, 2 |
| | • VLLS3 → RUN | — | 92 | μs | 1, 2 |
| | • LLS → RUN | — | 7.5 | μs | 2 |
| | • VLPS → RUN | — | 5.5 | μs | 2 |
| | • STOP → RUN | — | 5.5 | μs | 2 |

1. Normal boot (FTFL_FOPT[LPBOOT] is 1)
2. The wakeup time includes the execution time for a small amount of firmware used to produce a GPIO clear event. Wakeup time is measured from the falling edge of the external wakeup event to the falling edge of a GPIO clear performed by software.

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions*, and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*.
2. $V_{DD}$ = 3 V, $T_A$ = 25 °C, $f_{OSC}$ = 32 kHz (crystal), $f_{BUS}$ = 24 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

### 5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for "EMC design."

### 5.2.8 Capacitance attributes

**Table 7. Capacitance attributes**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $C_{IN\_A}$ | Input capacitance: analog pins | — | 7 | pF |
| $C_{IN\_D}$ | Input capacitance: digital pins | — | 7 | pF |

## 5.3 Switching electrical specifications

**Table 8. Device clock specifications**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| Normal run mode | | | | | |
| $f_{SYS}$ | System and core clock | — | 50 | MHz | |
| $f_{SYS\_USB}$ | System and core clock when USB in operation | 20 | — | MHz | |
| $f_{BUS}$ | Bus clock | — | 25 | MHz | |
| FB_CLK | Mini-FlexBus clock | — | 25 | MHz | 1 |
| $f_{LPTMR}$ | LPTMR clock | — | 25 | MHz | |
| VLPR mode | | | | | |
| $f_{SYS}$ | System and core clock | — | 2 | MHz | |
| $f_{BUS}$ | Bus clock | — | 1 | MHz | |
| FB_CLK | Mini-FlexBus clock | — | 1 | MHz | 1 |
| $f_{LPTMR}$ | LPTMR clock[2] | — | 25 | MHz | |

**Table 13. MCG specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $J_{cyc\_pll}$ | PLL period jitter (RMS) | | | | | 8 |
| | • $f_{vco}$ = 48 MHz | — | 120 | — | ps | |
| | • $f_{vco}$ = 100 MHz | — | 50 | — | ps | |
| $J_{acc\_pll}$ | PLL accumulated jitter over 1µs (RMS) | | | | | 8 |
| | • $f_{vco}$ = 48 MHz | — | 1350 | — | ps | |
| | • $f_{vco}$ = 100 MHz | — | 600 | — | ps | |
| $D_{lock}$ | Lock entry frequency tolerance | ± 1.49 | — | ± 2.98 | % | |
| $D_{unl}$ | Lock exit frequency tolerance | ± 4.47 | — | ± 5.97 | % | |
| $t_{pll\_lock}$ | Lock detector detection time | — | — | $150 \times 10^{-6} + 1075(1/f_{pll\_ref})$ | s | 9 |

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation ($\Delta f_{dco\_t}$) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

## 6.3.2 Oscillator electrical specifications

### 6.3.2.1 Oscillator DC electrical specifications

**Table 14. Oscillator DC electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | — | 3.6 | V | |
| $I_{DDOSC}$ | Supply current — low-power mode (HGO=0) | | | | | 1 |
| | • 32 kHz | — | 500 | — | nA | |
| | • 1 MHz | — | 200 | — | µA | |
| | • 4 MHz | — | 200 | — | µA | |
| | • 8 MHz (RANGE=01) | — | 300 | — | µA | |
| | | — | 950 | — | µA | |

*Table continues on the next page...*

**Table 14. Oscillator DC electrical specifications (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1) | — | $V_{DD}$ | — | V | |

1. $V_{DD}$=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. $C_x$ and $C_y$ can be provided by using either integrated capacitors or external components.
4. When low-power mode is selected, $R_F$ is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

### 6.3.2.2 Oscillator frequency specifications

**Table 15. Oscillator frequency specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{osc\_lo}$ | Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00) | 32 | — | 40 | kHz | |
| $f_{osc\_hi\_1}$ | Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01) | 1 | — | 8 | MHz | |
| $f_{osc\_hi\_2}$ | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | 8 | — | 32 | MHz | |
| $f_{ec\_extal}$ | Input clock frequency (external clock mode) | — | — | 50 | MHz | 1, 2 |
| $t_{dc\_extal}$ | Input clock duty cycle (external clock mode) | 40 | 50 | 60 | % | |
| $t_{cst}$ | Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0) | — | 750 | — | ms | 3, 4 |
| | Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1) | — | 250 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0) | — | 0.6 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1) | — | 1 | — | ms | |

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

### 6.4.1.3 Flash high voltage current behaviors

**Table 18. Flash high voltage current behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{DD\_PGM}$ | Average current adder during high voltage flash programming operation | — | 2.5 | 6.0 | mA |
| $I_{DD\_ERS}$ | Average current adder during high voltage flash erase operation | — | 1.5 | 4.0 | mA |

### 6.4.1.4 Reliability specifications

**Table 19. NVM reliability specifications**

| Symbol | Description | Min. | Typ.[1] | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Program Flash | | | | | | |
| $t_{nvmretp10k}$ | Data retention after up to 10 K cycles | 5 | 50 | — | years | 2 |
| $t_{nvmretp1k}$ | Data retention after up to 1 K cycles | 20 | 100 | — | years | 2 |
| $t_{nvmretp100}$ | Data retention after up to 100 cycles | 15 | 100 | — | years | 2 |
| $n_{nvmcycp}$ | Cycling endurance | 10 K | 50 K | — | cycles | 3 |
| Data Flash | | | | | | |
| $t_{nvmretd10k}$ | Data retention after up to 10 K cycles | 5 | 50 | — | years | 2 |
| $t_{nvmretd1k}$ | Data retention after up to 1 K cycles | 20 | 100 | — | years | 2 |
| $t_{nvmretd100}$ | Data retention after up to 100 cycles | 15 | 100 | — | years | 2 |
| $n_{nvmcycd}$ | Cycling endurance | 10 K | 50 K | — | cycles | 3 |
| FlexRAM as EEPROM | | | | | | |
| $t_{nvmretee100}$ | Data retention up to 100% of write endurance | 5 | 50 | — | years | 2 |
| $t_{nvmretee10}$ | Data retention up to 10% of write endurance | 20 | 100 | — | years | 2 |
| $t_{nvmretee1}$ | Data retention up to 1% of write endurance | 15 | 100 | — | years | 2 |
| $n_{nvmwree16}$<br>$n_{nvmwree128}$<br>$n_{nvmwree512}$<br>$n_{nvmwree4k}$<br>$n_{nvmwree8k}$ | Write endurance<br>• EEPROM backup to FlexRAM ratio = 16<br>• EEPROM backup to FlexRAM ratio = 128<br>• EEPROM backup to FlexRAM ratio = 512<br>• EEPROM backup to FlexRAM ratio = 4096<br>• EEPROM backup to FlexRAM ratio = 8192 | <br>35 K<br>315 K<br>1.27 M<br>10 M<br>20 M | <br>175 K<br>1.6 M<br>6.4 M<br>50 M<br>100 M | <br>—<br>—<br>—<br>—<br>— | <br>writes<br>writes<br>writes<br>writes<br>writes | 4 |

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology.
3. Cycling endurance represents number of program/erase cycles at –40 °C ≤ $T_j$ ≤ 125 °C.
4. Write endurance represents the number of writes to each FlexRAM location at –40 °C ≤Tj ≤ 125 °C influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup. Minimum and typical values assume all byte-writes to FlexRAM.

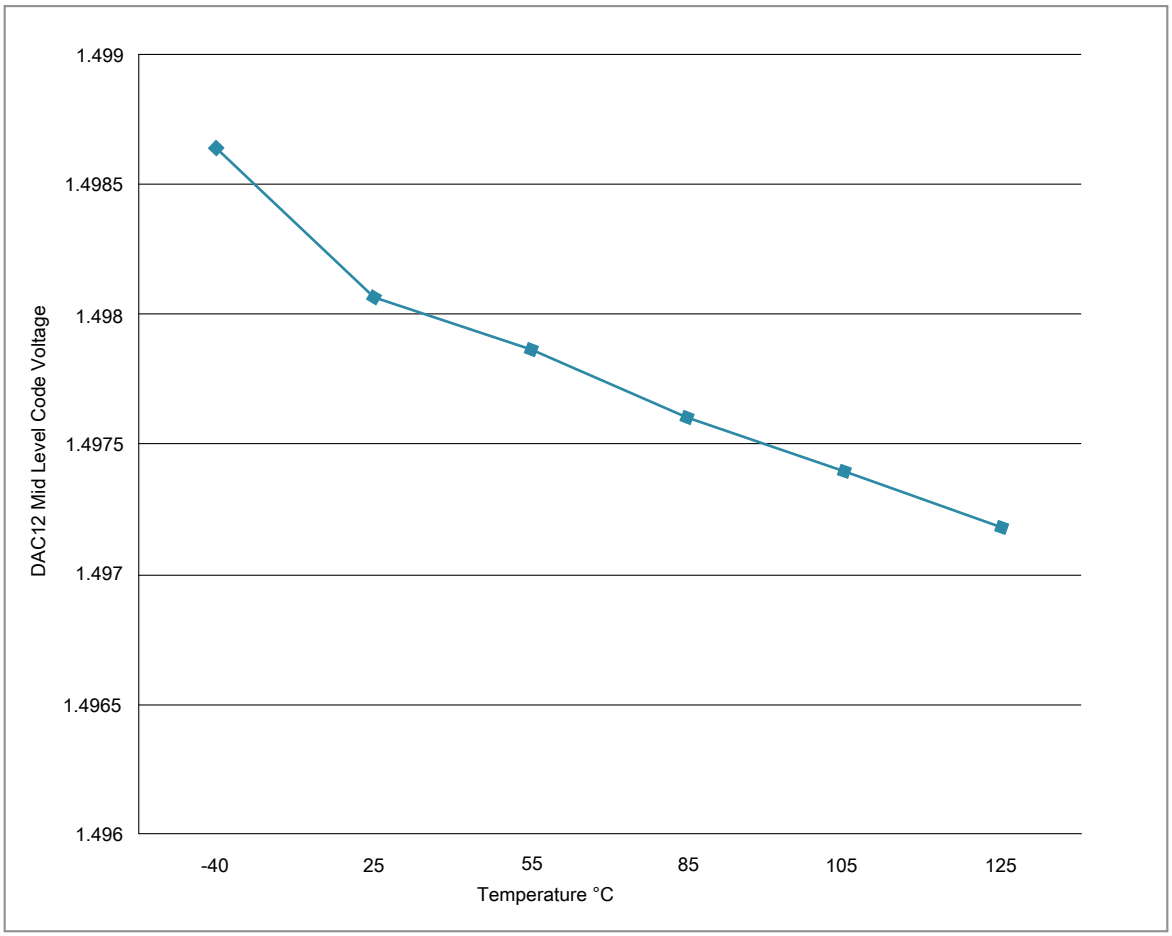


**Figure 13. Offset at half scale vs. temperature**

## 6.6.4 Voltage reference electrical specifications

**Table 27. VREF full-range operating requirements**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | 1.71 | 3.6 | V | — |
| $C_L$ | Output load capacitance | 100 | | nF | 1 |

1. $C_L$ must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.

**Table 28. VREF full-range operating behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{out}$ | Voltage reference output with factory trim at nominal $V_{DDA}$ and temperature=25C | 1.1965 | 1.2 | 1.2027 | V | |
| $V_{out}$ | Voltage reference output — factory trim | 1.144 | — | 1.266 | V | |

*Table continues on the next page...*

### 6.8.4 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to 20% $V_{DD}$ and 70% $V_{DD}$, unless noted, as well as input signal transitions of 3 ns and a 50 pF maximum load on all SPI pins. All timing assumes slew rate control is disabled and high drive strength is enabled for SPI output pins.

**Table 33. SPI master mode timing**

| Num. | Symbol | Description | Min. | Max. | Unit | Comment |
|---|---|---|---|---|---|---|
| 1 | $f_{op}$ | Frequency of operation | $f_{BUS}/2048$ | $f_{BUS}/2$ | Hz | $f_{BUS}$ is the bus clock as defined in Table 8. |
| 2 | $t_{SPSCK}$ | SPSCK period | 2 x $t_{BUS}$ | 2048 x $t_{BUS}$ | ns | $t_{BUS}$ = 1/ $f_{BUS}$ |
| 3 | $t_{Lead}$ | Enable lead time | 1/2 | — | $t_{SPSCK}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1/2 | — | $t_{SPSCK}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{BUS}$ - 30 | 1024 x $t_{BUS}$ | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 21 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 0 | — | ns | — |
| 8 | $t_{v}$ | Data valid (after SPSCK edge) | — | 25 | ns | — |
| 9 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |
| 10 | $t_{RI}$ | Rise time input | — | $t_{BUS}$ - 25 | ns | — |
| | $t_{FI}$ | Fall time input | | | | |
| 11 | $t_{RO}$ | Rise time output | — | 25 | ns | — |
| | $t_{FO}$ | Fall time output | | | | |

## Table 34. SPI slave mode timing (continued)

| Num. | Symbol | Description | Min. | Max. | Unit | Comment |
|---|---|---|---|---|---|---|
| 3 | $t_{Lead}$ | Enable lead time | 1 | — | $t_{BUS}$ | — |
| 4 | $t_{Lag}$ | Enable lag time | 1 | — | $t_{BUS}$ | — |
| 5 | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{BUS}$ - 30 | — | ns | — |
| 6 | $t_{SU}$ | Data setup time (inputs) | 19.5 | — | ns | — |
| 7 | $t_{HI}$ | Data hold time (inputs) | 0 | — | ns | — |
| 8 | $t_a$ | Slave access time | — | $t_{BUS}$ | ns | Time to data active from high-impedance state |
| 9 | $t_{dis}$ | Slave MISO disable time | — | $t_{BUS}$ | ns | Hold time to high-impedance state |
| 10 | $t_v$ | Data valid (after SPSCK edge) | — | 27 | ns | — |
| 11 | $t_{HO}$ | Data hold time (outputs) | 0 | — | ns | — |
| 12 | $t_{RI}$ | Rise time input | — | $t_{BUS}$ - 25 | ns | — |
| | $t_{FI}$ | Fall time input | | | | |
| 13 | $t_{RO}$ | Rise time output | — | 25 | ns | — |
| | $t_{FO}$ | Fall time output | | | | |

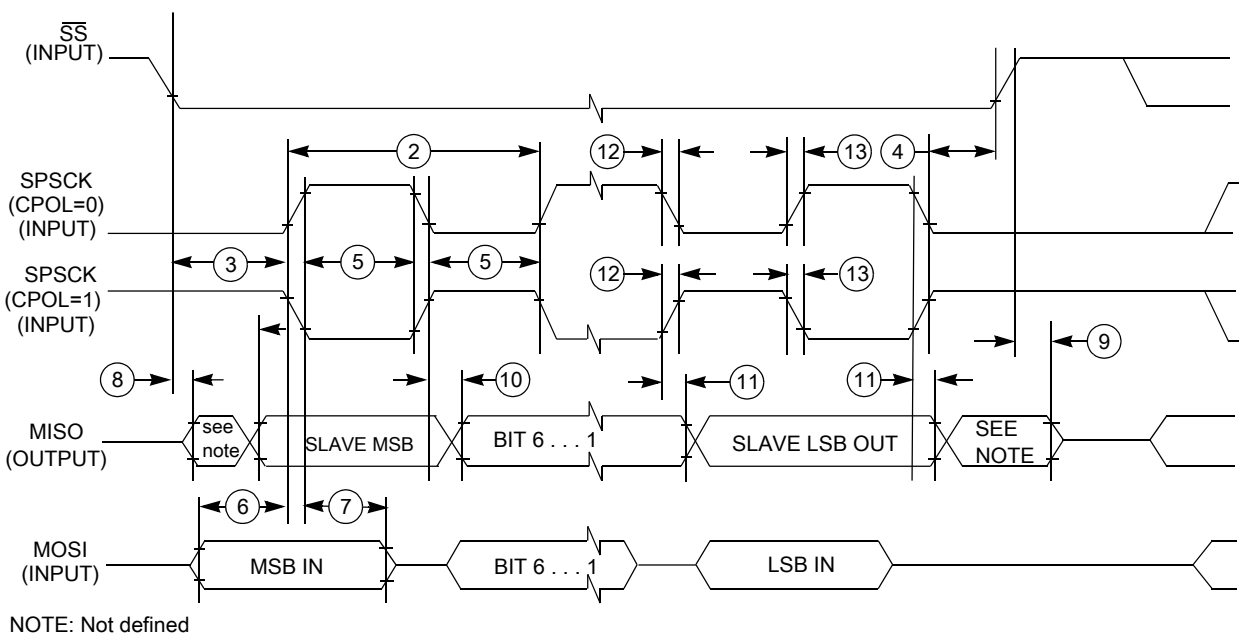


**Figure 16. SPI slave mode timing (CPHA=0)**

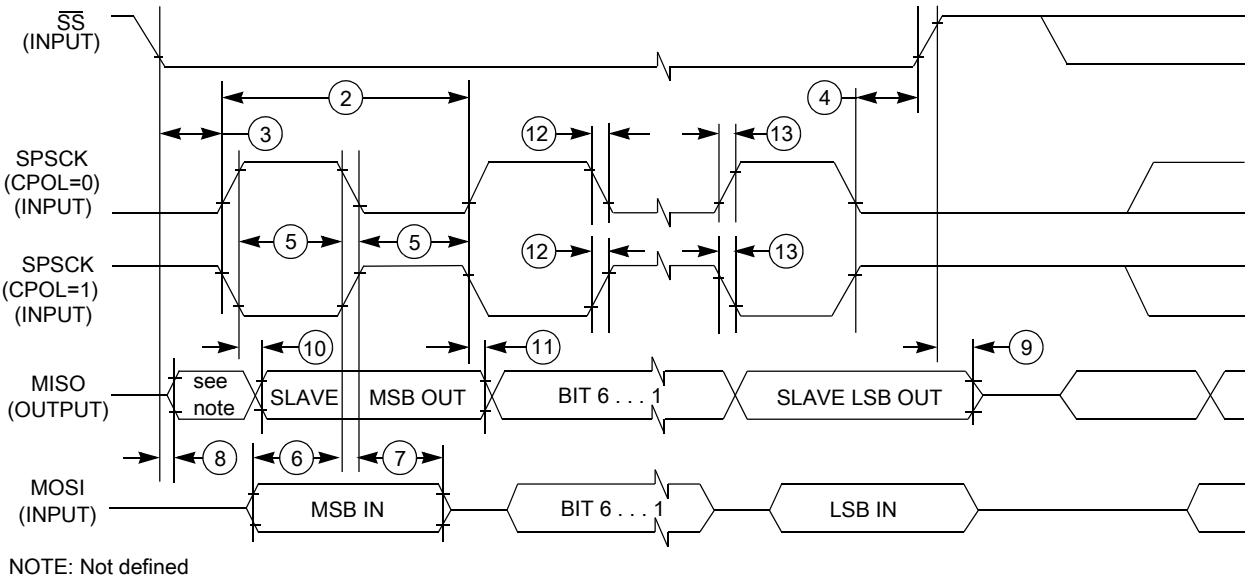


**Figure 17. SPI slave mode timing (CPHA=1)**

## 6.8.5 I2S/SAI Switching Specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures. All timing shown is also with respect to input signal transitions of 3 ns and a 50 pF maximum load.

**Table 35. I2S/SAI master mode timing**

| Num. | Characteristic | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| S1 | I2S_MCLK cycle time[1] | 40 | — | ns |
| S2 | I2S_MCLK (as an input) pulse width high/low | 45% | 55% | MCLK period |
| S3 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (output) | 80 | — | ns |
| S4 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low | 45% | 55% | BCLK period |
| S5 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid | — | 15 | ns |
| S6 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid | 0 | — | ns |
| S7 | I2S_TX_BCLK to I2S_TXD valid | — | 15 | ns |
| S8 | I2S_TX_BCLK to I2S_TXD invalid | 0 | — | ns |
| S9 | I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK | 25 | — | ns |

*Table continues on the next page...*

## NOTE

- On PTB0, EZP_MS_b is active only during reset. Refer to the detailed boot description.
- PTC1 is open drain.

| 64-pin | 48-pin | 44-pin | 32-pin | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| — | — | — | EP | Exposed Pads | Exposed die attach pad. Connection to VSS is recommended. | | | | | | | | |
| — | — | EP | — | VSS | Exposed die attach pads are connected internally to VSS. External connection to VSS is recommended. | | | | | | | | |
| 1 | — | — | — | VDD | VDD | | | | | | | | |
| 2 | — | — | — | VSS | VSS | | | | | | | | |
| 3 | — | — | — | Disabled | Disabled | PTC6 | UART0_TX | I2C0_SCL | RGPIO6 | SPI1_MOSI | FBa_AD11 | | |
| 4 | — | — | — | Disabled | Disabled | PTC7 | UART0_RX | I2C0_SDA | RGPIO7 | SPI1_MISO | FBa_AD12 | | |
| 5 | 1 | — | — | Disabled | Disabled | PTD0 | UART0_CTS_b | I2C1_SDA | RGPIO8 | SPI1_SCLK | FBa_AD13 | I2S0_MCLK/ I2S0_CLKIN | |
| 6 | 2 | — | — | Disabled | Disabled | PTD1 | UART0_RTS_b | I2C1_SCL | RGPIO9 | SPI1_SS | FBa_AD14 | I2S0_RX_BCLK | |
| 7 | 3 | 1 | 1 | Disabled | Disabled | PTA0 | | I2C2_SCL | FTM1_CH0 | SPI0_SS | FBa_AD15 | I2S0_RX_FS | |
| 8 | 4 | 2 | 2 | Disabled | Disabled | PTA1 | | I2C2_SDA | FTM1_CH1 | | FBa_AD16 | I2S0_RXD | |
| 9 | 5 | 3 | 3 | Disabled | Disabled | PTA2 | UART1_TX | | FTM1_CH2 | SPI1_SS | | | |
| 10 | 6 | 4 | 4 | Disabled | Disabled | PTA3 | UART1_RX | | FTM1_CH3 | SPI1_SCLK | | I2S0_TX_BCLK | EZP_CLK |
| 11 | 7 | 5 | 5 | ADC0_SE2 | ADC0_SE2 | PTA4 | UART1_CTS_b | I2C2_SCL | FTM1_CH4 | SPI1_MISO | | I2S0_TX_FS | EZP_DI |
| 12 | 8 | 6 | 6 | ADC0_SE3 | ADC0_SE3 | PTA5 | UART1_RTS_b | I2C2_SDA | FTM1_CH5 | SPI1_MOSI | CLKOUT | I2S0_TXD | EZP_DO |
| 13 | 9 | 7 | 7 | VDDA | VDDA | | | | | | | | |
| 14 | 10 | 8 | — | VREFH | VREFH | | | | | | | | |
| 15 | 11 | 9 | — | VREF_OUT | VREF_OUT | | | | | | | | |
| 16 | 12 | 10 | — | VREFL | VREFL | | | | | | | | |
| 17 | 13 | 11 | 8 | VSSA | VSSA | | | | | | | | |
| 18 | 14 | 12 | 9 | DAC0_OUT | DAC0_OUT | | | | | | | | |
| 19 | 15 | 13 | 10 | VREGIN | VREGIN | | | | | | | | |
| 20 | 16 | 14 | 11 | VOUT33 | VOUT33 | | | | | | | | |
| 21 | 17 | 15 | 12 | USB0_DM | USB0_DM | | | | | | | | |

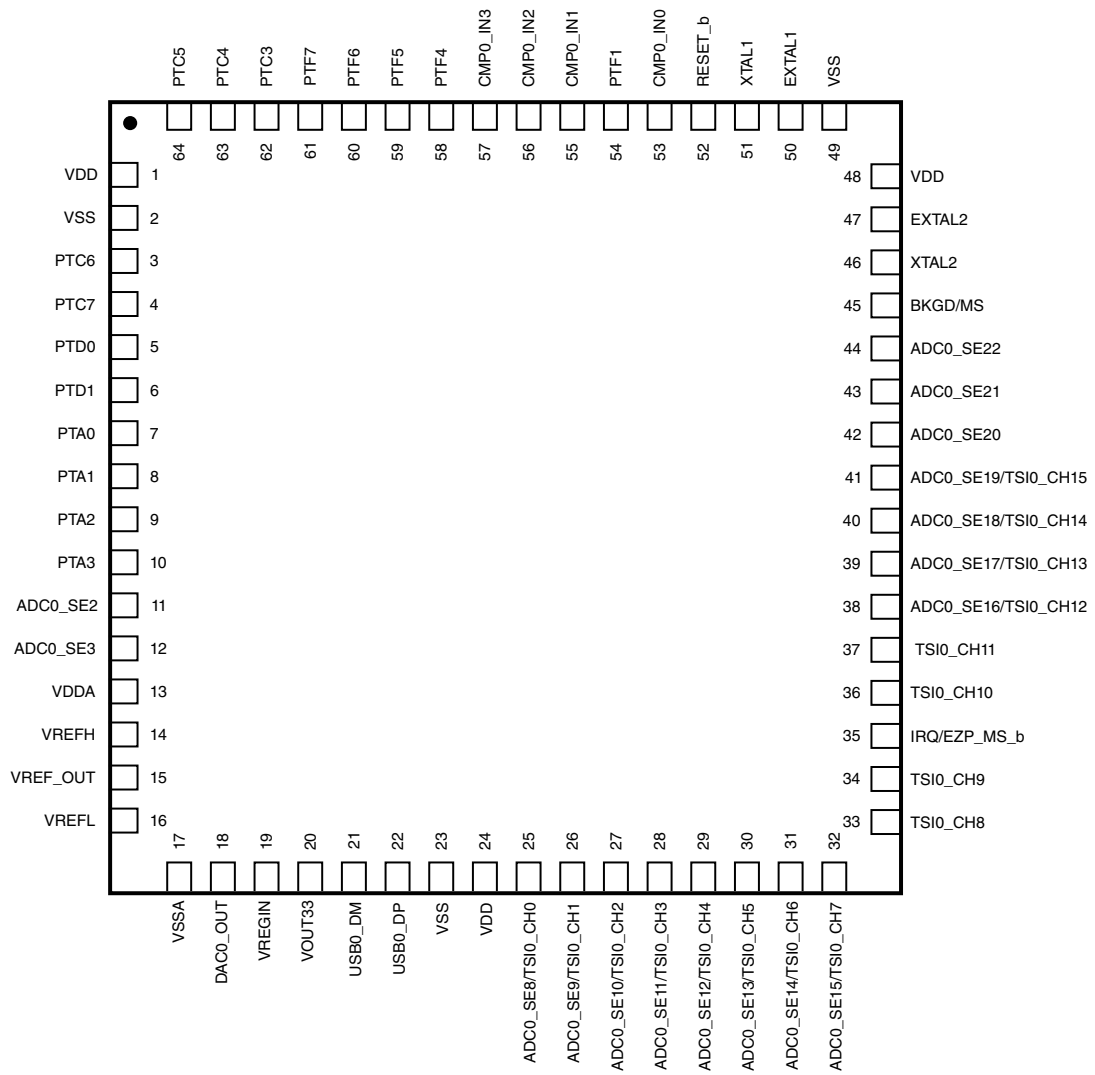


**Figure 20. 64-pin LQFP**

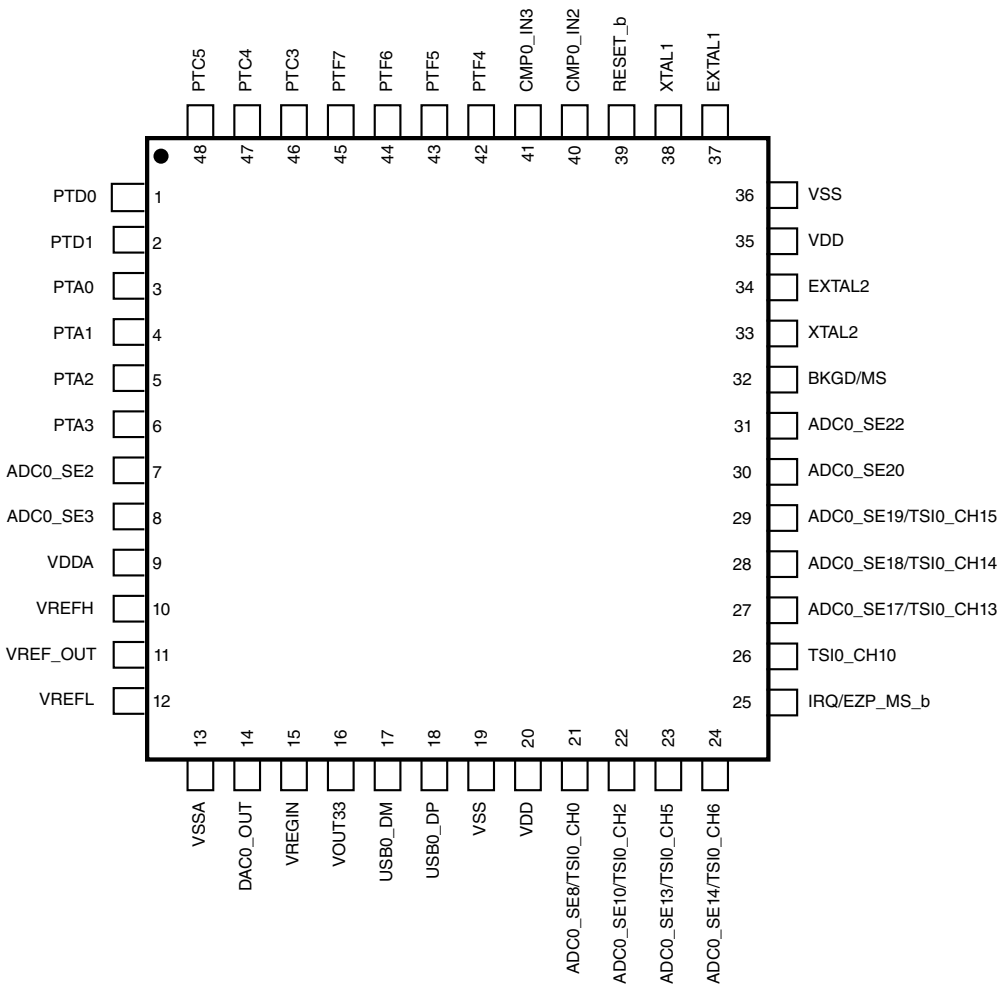


**Figure 21. 48-pin LQFP**

## Table 38. Module signals by GPIO port and pin (continued)

| 64-pin | 48-pin | 44-pin | 32-pin | Port | Module signal(s) |
|---|---|---|---|---|---|
| 48 | 35 | 31 | 24 | | VDD |
| 2 | | | | | VSS |
| 23 | 19 | 17 | 14 | | VSS |
| 49 | 36 | 32 | 25 | | VSS |
| System | | | | | |
| 45 | 32 | 28 | 21 | PTB4 | BKGD/MS |
| 12 | 8 | 6 | 6 | PTA5 | CLKOUT |
| 62 | 46 | 42 | 30 | PTC3 | CLKOUT |
| 10 | 6 | 4 | 4 | PTA3 | EZP_CLK |
| 11 | 7 | 5 | 5 | PTA4 | EZP_DI |
| 12 | 8 | 6 | 6 | PTA5 | EZP_DO |
| 35 | 25 | 23 | 17 | PTB0 | IRQ/EZP_MS_b, EZP_CS_b |
| 52 | 39 | 35 | 28 | PTC1 | RESET_b |
| OSC | | | | | |
| 50 | 37 | 33 | 26 | PTB7 | EXTAL1 |
| 47 | 34 | 30 | 23 | PTB6 | EXTAL2 |
| 51 | 38 | 34 | 27 | PTC0 | XTAL1 |
| 46 | 33 | 29 | 22 | PTB5 | XTAL2 |
| LLWU | | | | | |
| 4 | | | | PTC7 | LLWU_P0 |
| 6 | 2 | | | PTD1 | LLWU_P1 |
| 12 | 8 | 6 | 6 | PTA5 | LLWU_P2 |
| 30 | 23 | 21 | 16 | PTA7 | LLWU_P3 |
| 32 | | | | PTD7 | LLWU_P4 |
| 35 | 25 | 23 | 17 | PTB0 | LLWU_P5 |
| 36 | 26 | 24 | 18 | PTB1 | LLWU_P6 |
| 39 | 27 | 25 | 19 | PTB2 | LLWU_P7 |
| 44 | 31 | 27 | | PTE7 | LLWU_P8 |
| 45 | 32 | 28 | 21 | PTB4 | LLWU_P9 |
| 55 | | | | PTF2 | LLWU_P10 |
| 56 | 40 | 36 | | PTF3 | LLWU_P11 |
| 57 | 41 | 37 | 29 | PTC2 | LLWU_P12 |
| 59 | 43 | 39 | | PTF5 | LLWU_P13 |
| 62 | 46 | 42 | 30 | PTC3 | LLWU_P14 |
| 63 | 47 | 43 | 31 | PTC4 | LLWU_P15 |
| RGPIO | | | | | |
| 51 | 38 | 34 | 27 | PTC0 | RGPIO0 |
| 56 | 40 | 36 | | PTF3 | RGPIO1 |
| 57 | 41 | 37 | 29 | PTC2 | RGPIO2 |

*Table continues on the next page...*

## Table 38. Module signals by GPIO port and pin (continued)

| 64-pin | 48-pin | 44-pin | 32-pin | Port | Module signal(s) |
|---|---|---|---|---|---|
| 61 | 45 | 41 | | PTF7 | PTF7 |
| 5 V VREG | | | | | |
| 20 | 16 | 14 | 11 | | VOUT33 |
| 19 | 15 | 13 | 10 | | VREGIN |
| USB0 | | | | | |
| 63 | 47 | 43 | 31 | PTC4 | USB_SOF_PULSE |
| 62 | 46 | 42 | 30 | PTC3 | USB_CLKIN |
| 21 | 17 | 15 | 12 | | USB0_DM |
| 22 | 18 | 16 | 13 | | USB0_DP |
| 20 | 16 | 14 | 11 | | VOUT33 |
| 19 | 15 | 13 | 10 | | VREGIN |
| ADC0 | | | | | |
| 11 | 7 | 5 | 5 | PTA4 | ADC0_SE2 |
| 12 | 8 | 6 | 6 | PTA5 | ADC0_SE3 |
| 25 | 21 | 19 | 15 | PTA6 | ADC0_SE8 |
| 26 | | | | PTD2 | ADC0_SE9 |
| 27 | 22 | 20 | | PTD3 | ADC0_SE10 |
| 28 | | | | PTD4 | ADC0_SE11 |
| 29 | | | | PTD5 | ADC0_SE12 |
| 30 | 23 | 21 | 16 | PTA7 | ADC0_SE13 |
| 31 | 24 | 22 | | PTD6 | ADC0_SE14 |
| 32 | | | | PTD7 | ADC0_SE15 |
| 38 | | | | PTE3 | ADC0_SE16 |
| 39 | 27 | 25 | 19 | PTB2 | ADC0_SE17 |
| 40 | 28 | 26 | 20 | PTB3 | ADC0_SE18 |
| 41 | 29 | | | PTE4 | ADC0_SE19 |
| 42 | 30 | | | PTE5 | ADC0_SE20 |
| 43 | | | | PTE6 | ADC0_SE21 |
| 44 | 31 | 27 | | PTE7 | ADC0_SE22 |
| 13 | 9 | 7 | 7 | | VDDA |
| 14 | 10 | 8 | | | VREFH |
| 16 | 12 | 10 | | | VREFL |
| 17 | 13 | 11 | 8 | | VSSA |
| DAC0 | | | | | |
| 18 | 14 | 12 | 9 | | DAC0_OUT |
| VREF | | | | | |
| 15 | 11 | 9 | | | VREF_OUT |
| CMP0 | | | | | |
| 53 | | | | PTF0 | CMP0_IN0 |

*Table continues on the next page...*

## Table 38. Module signals by GPIO port and pin (continued)

| 64-pin | 48-pin | 44-pin | 32-pin | Port | Module signal(s) |
|---|---|---|---|---|---|
| 56 | 40 | 36 | | PTF3 | FBa_AD8 |
| 60 | 44 | 40 | | PTF6 | FBa_AD9 |
| 61 | 45 | 41 | | PTF7 | FBa_AD10 |
| 3 | | | | PTC6 | FBa_AD11 |
| 4 | | | | PTC7 | FBa_AD12 |
| 5 | 1 | | | PTD0 | FBa_AD13 |
| 6 | 2 | | | PTD1 | FBa_AD14 |
| 7 | 3 | 1 | 1 | PTA0 | FBa_AD15 |
| 8 | 4 | 2 | 2 | PTA1 | FBa_AD16 |
| 25 | 21 | 19 | 15 | PTA6 | FBa_AD17 |
| 57 | 41 | 37 | 29 | PTC2 | FBa_AD18 |
| 58 | 42 | 38 | | PTF4 | FBa_AD19 |
| 40 | 28 | 26 | 20 | PTB3 | FBa_ALE |
| 39 | 27 | 25 | 19 | PTB2 | FBa_CS0_b |
| 37 | | | | PTE2 | FBa_D0 |
| 34 | | | | PTE1 | FBa_D1 |
| 33 | | | | PTE0 | FBa_D2 |
| 32 | | | | PTD7 | FBa_D3 |
| 31 | 24 | 22 | | PTD6 | FBa_D4 |
| 30 | 23 | 21 | 16 | PTA7 | FBa_D5 |
| 29 | | | | PTD5 | FBa_D6 |
| 28 | | | | PTD4 | FBa_D7 |
| 38 | | | | PTE3 | FBa_OE_b |
| 59 | 43 | 39 | | PTF5 | FBa_RW_b |
| DATA_BUS | | | | | |
| 8 | 4 | 2 | 2 | PTA1 | FBa_AD16 |
| 39 | 27 | 25 | 19 | PTB2 | FBa_CS0_b |
| 61 | 45 | 41 | | PTF7 | FBa_D0 |
| 60 | 44 | 40 | | PTF6 | FBa_D1 |
| 59 | 43 | 39 | | PTF5 | FBa_D2 |
| 58 | 42 | 38 | | PTF4 | FBa_D3 |
| 31 | 24 | 22 | | PTD6 | FBa_D4 |
| 30 | 23 | 21 | 16 | PTA7 | FBa_D5 |
| 27 | 22 | 20 | | PTD3 | FBa_D6 |
| 25 | 21 | 19 | 15 | PTA6 | FBa_D7 |
| 44 | 31 | 27 | | PTE7 | FBa_RW_b |
| I2C0 and I2C1 | | | | | |
| 3 | | | | PTC6 | I2C0_SCL |
| 35 | 25 | 23 | 17 | PTB0 | I2C0_SCL |

*Table continues on the next page...*

## Table 38. Module signals by GPIO port and pin (continued)

| 64-pin | 48-pin | 44-pin | 32-pin | Port | Module signal(s) |
|---|---|---|---|---|---|
| 44 | 31 | 27 | | PTE7 | SPI1_MOSI |
| 60 | 44 | 40 | | PTF6 | SPI1_MOSI |
| 5 | 1 | | | PTD0 | SPI1_SCLK |
| 10 | 6 | 4 | 4 | PTA3 | SPI1_SCLK |
| 42 | 30 | | | PTE5 | SPI1_SCLK |
| 58 | 42 | 38 | | PTF4 | SPI1_SCLK |
| 6 | 2 | | | PTD1 | SPI1_SS |
| 9 | 5 | 3 | 3 | PTA2 | SPI1_SS |
| 41 | 29 | | | PTE4 | SPI1_SS |
| 57 | 41 | 37 | 29 | PTC2 | SPI1_SS |
| UART0 | | | | | |
| 5 | 1 | | | PTD0 | UART0_CTS_b |
| 32 | | | | PTD7 | UART0_CTS_b |
| 42 | 30 | | | PTE5 | UART0_CTS_b |
| 62 | 46 | 42 | 30 | PTC3 | UART0_CTS_b |
| 6 | 2 | | | PTD1 | UART0_RTS_b |
| 33 | | | | PTE0 | UART0_RTS_b |
| 41 | 29 | | | PTE4 | UART0_RTS_b |
| 61 | 45 | 41 | | PTF7 | UART0_RTS_b |
| 4 | | | | PTC7 | UART0_RX |
| 31 | 24 | 22 | | PTD6 | UART0_RX |
| 43 | | | | PTE6 | UART0_RX |
| 63 | 47 | 43 | 31 | PTC4 | UART0_RX |
| 3 | | | | PTC6 | UART0_TX |
| 30 | 23 | 21 | 16 | PTA7 | UART0_TX |
| 44 | 31 | 27 | | PTE7 | UART0_TX |
| 64 | 48 | 44 | 32 | PTC5 | UART0_TX |
| UART1 | | | | | |
| 11 | 7 | 5 | 5 | PTA4 | UART1_CTS_b |
| 58 | 42 | 38 | | PTF4 | UART1_CTS_b |
| 12 | 8 | 6 | 6 | PTA5 | UART1_RTS_b |
| 57 | 41 | 37 | 29 | PTC2 | UART1_RTS_b |
| 10 | 6 | 4 | 4 | PTA3 | UART1_RX |
| 59 | 43 | 39 | | PTF5 | UART1_RX |
| 9 | 5 | 3 | 3 | PTA2 | UART1_TX |
| 60 | 44 | 40 | | PTF6 | UART1_TX |