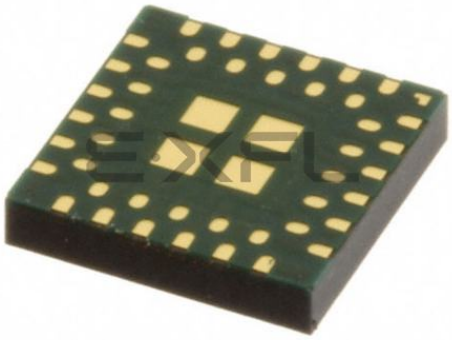

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 9x12b; D/A 1x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFLGA Exposed Pad
Supplier Device Package	44-MAPLGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51jf32vhs

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device:

1. Go to www.freescale.com.
2. Perform a part number search for the following partial device numbers: PCF51JF and MCF51JF.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q CCCC DD MMM T PP

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
CCCC	Core code	CF51 = ColdFire V1
DD	Device number	JF, JU, QF, QH, QM, QU
MMM	Memory size (program flash memory)[1]	• 32 = 32 KB

Table continues on the next page...

3.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

3.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

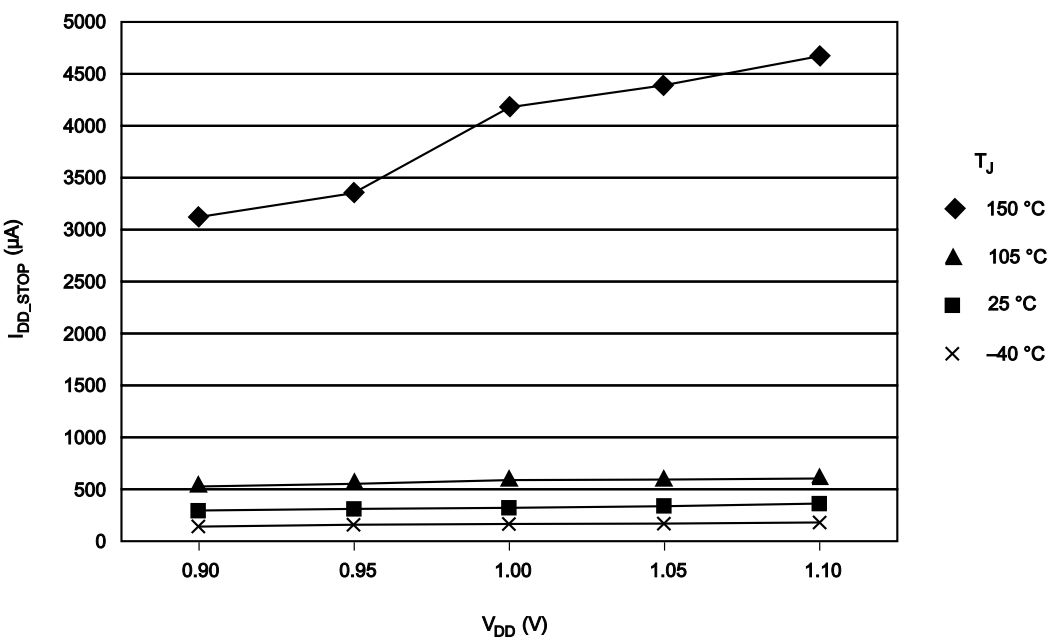
3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



5.2.5 Power consumption operating behaviors

Table 5. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from RAM • @ 1.8 V • @ 3.0 V	— —	13 13	— 16	mA mA	2
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash memory with page buffering disabled • @ 1.8 V • @ 3.0 V	— —	14.3 14.5	— 17.9	mA mA	2
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from RAM, exercising flash memory • @ 1.8 V • @ 3.0 V	— —	20 20	23.5 25	mA mA	3
I_{DD_WAIT}	Wait mode current at 3.0 V — all peripheral clocks disabled	—	5.8	6.8	mA	4
I_{DD_STOP}	Stop mode current at 3.0 V • @ –40 to 25 °C • @ 105 °C	— —	0.34 0.90	0.41 1.8	mA mA	
I_{DD_VLPR}	Very low-power run mode current at 3.0 V — all peripheral clocks disabled	—	0.63	1.32	mA	5
I_{DD_VLPR}	Very low-power run mode current at 3.0 V — all peripheral clocks enabled	—	0.78	1.46	mA	6
I_{DD_VLPW}	Very low-power wait mode current at 3.0 V	—	0.15	0.62	mA	7
I_{DD_VLPS}	Very low-power stop mode current at 3.0 V • @ –40 to 25 °C • @ 105 °C	— —	19 145	45 312	µA	8
I_{DD_LLS}	Low leakage stop mode current at 3.0 V • @ –40 to 25 °C • @ 105 °C	— —	3.0 53.3	4.8 157	µA µA	8,9,10
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V • @ –40 to 25 °C • @ 105 °C	— —	1.8 39.2	3.3 115	µA µA	8,9,10
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V	— —	1.6 22.2	2.8 65	µA µA	8,9

Table continues on the next page...

Table 5. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• @ –40 to 25 °C • @ 105 °C					
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V • @ –40 to 25 °C • @ 105 °C	— —	1.4 17.6	2.6 50	µA µA	8,9
I_{DD_RTC}	Average current adder for real-time clock function • @ –40 to 25 °C	—	0.7	—	µA	11

1. The analog supply current is the sum of the active current for each of the analog modules on the device. See each module's specification for its supply current.
2. 50 MHz core and system clocks, and 25 MHz bus clock. MCG configured for FEI mode. All peripheral clocks disabled.
3. 50 MHz core and system clocks, and 25 MHz bus clock. MCG configured for FEI mode. All peripheral clocks enabled, but peripherals are not in active operation.
4. 50 MHz core and system clocks, and 25 MHz bus clock. MCG configured for FEI mode.
5. 2 MHz core and system clocks, and 1 MHz bus clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash memory.
6. 2 MHz core and system clocks, and 1 MHz bus clock. MCG configured for BLPE mode. All peripheral clocks enabled, but peripherals are not in active operation. Code executing from flash memory.
7. 2 MHz core and system clocks, and 1 MHz bus clock. MCG configured for BLPE mode. All peripheral clocks disabled.
8. OSC clocks disabled.
9. All pads disabled.
10. Data reflects devices with 32 KB of RAM. For devices with 16 KB of RAM, power consumption is reduced by 500 nA. For devices with 8 KB of RAM, power consumption is reduced by 750 nA.
11. RTC function current includes LPTMR with OSC enabled with 32.768 kHz crystal at 3.0 V

5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode, except for 50 MHz core (FEI mode)
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL
- For the ALLON curve, all peripheral clocks are enabled, but peripherals are not in active operation
- USB Voltage Regulator disabled
- No GPIOs toggled
- Code execution from flash memory with cache enabled

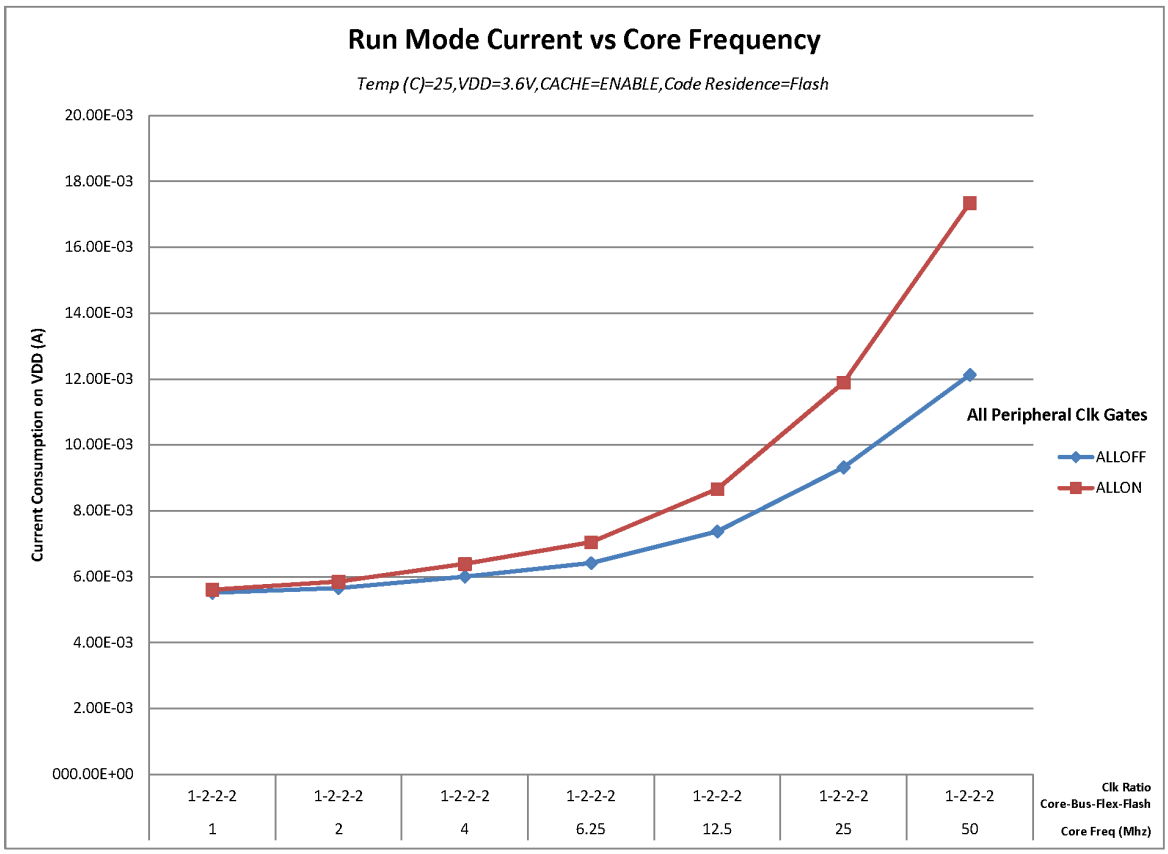


Figure 1. Run mode supply current vs. core frequency

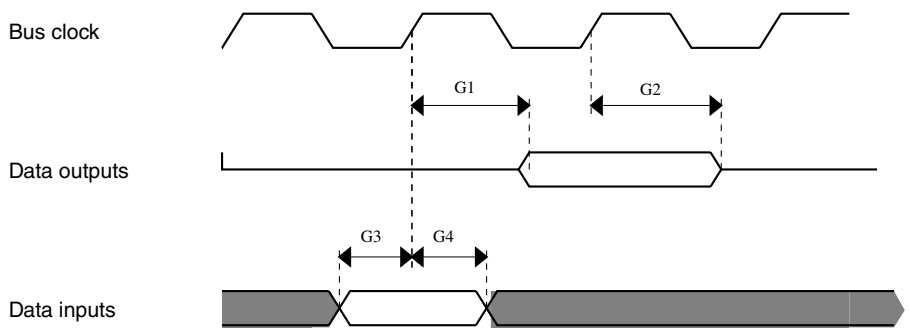


Figure 3. EGPIO timing diagram

The following general purpose specifications apply to all signals configured for RGPIO, FTM, and UART. The conditions are 25 pf load, V_{DD} = 3.6 V to 1.71 V, and full temperature range. The GPIO are set for high drive, no slew rate control, and no input filter, digital or analog, unless otherwise specified.

Table 10. RGPIO General Control Timing

Symbol	Description	Min.	Max.	Unit
R1	CPUCLK from CLK_OUT pin high to GPIO output valid	—	16	ns
R2	CPUCLK from CLK_OUT pin high to GPIO output invalid (output hold)	1	—	ns
R3	GPIO input valid to bus clock high	17	—	ns
R4	CPUCLK from CLK_OUT pin high to GPIO input invalid	—	2	ns

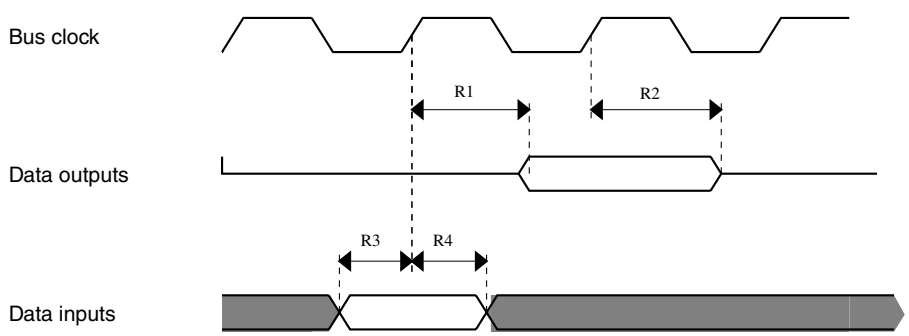


Figure 4. RGPIO timing diagram

Table 14. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• 16 MHz	—	1.2	—	mA	
	• 24 MHz	—	1.5	—	mA	
	• 32 MHz					
I_{DDOSC}	Supply current — high-gain mode (HGO=1)					1
	• 32 kHz	—	25	—	µA	
	• 1 MHz	—	300	—	µA	
	• 4 MHz	—	400	—	µA	
	• 8 MHz (RANGE=01)	—	500	—	µA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)					
	• 1 MHz resonator	—	6.6	—	kΩ	
	• 2 MHz resonator	—	3.3	—	kΩ	
	• 4 MHz resonator	—	0	—	kΩ	
	• 8 MHz resonator	—	0	—	kΩ	
	• 16 MHz resonator	—	0	—	kΩ	
	• 20 MHz resonator	—	0	—	kΩ	
	• 32 MHz resonator	—	0	—	kΩ	
V_{pp}[5]	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	

Table continues on the next page...

6.4 Memories and memory interfaces

6.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 16. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversblk32k}$	Erase Block high-voltage time for 32 KB	—	52	452	ms	1
$t_{hversblk128k}$	Erase Block high-voltage time for 128 KB	—	208	1808	ms	1

1. Maximum time based on expectations at cycling end-of-life.

6.4.1.2 Flash timing specifications — commands

Table 17. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Read 1s Block execution time					1
$t_{rd1blk32k}$	• 32 KB data flash	—	—	0.5	ms	
$t_{rd1blk128k}$	• 128 KB program flash	—	—	1.7	ms	
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	—
	Erase Flash Block execution time					2
$t_{ersblk32k}$	• 32 KB data flash	—	55	465	ms	
$t_{ersblk128k}$	• 128 KB program flash	—	220	1850	ms	
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
	Program Section execution time					—
$t_{pgmsec512}$	• 512 bytes flash	—	4.7	—	ms	
$t_{pgmsec1k}$	• 1 KB flash	—	9.3	—	ms	

Table continues on the next page...

6.4.2 EzPort Switching Specifications

All timing is shown with respect to a maximum pin load of 50 pF and input signal transitions of 3 ns.

Table 20. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	$f_{SYS}/2$	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	$f_{SYS}/8$	MHz
EP2	$\overline{\text{EZP\_CS}}$ negation to next $\overline{\text{EZP\_CS}}$ assertion	2 x t_{EZP_CK}	—	ns
EP3	$\overline{\text{EZP\_CS}}$ input valid to EZP_CK high (setup)	15	—	ns
EP4	EZP_CK high to $\overline{\text{EZP\_CS}}$ input invalid (hold)	0.0	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	15	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	0.0	—	ns
EP7	EZP_CK low to EZP_Q output valid (setup)	—	25	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0.0	—	ns
EP9	$\overline{\text{EZP\_CS}}$ negation to EZP_Q tri-state	—	12	ns

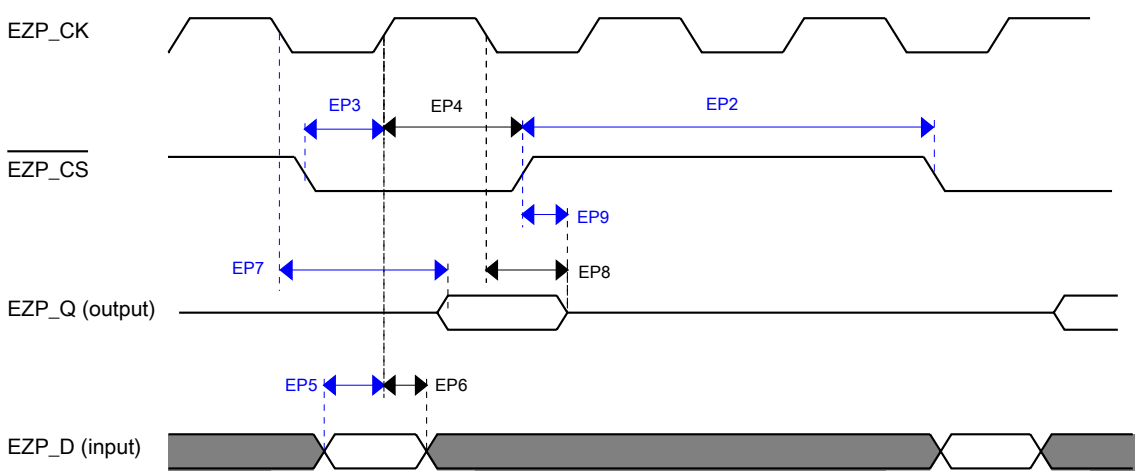


Figure 5. EzPort Timing Diagram

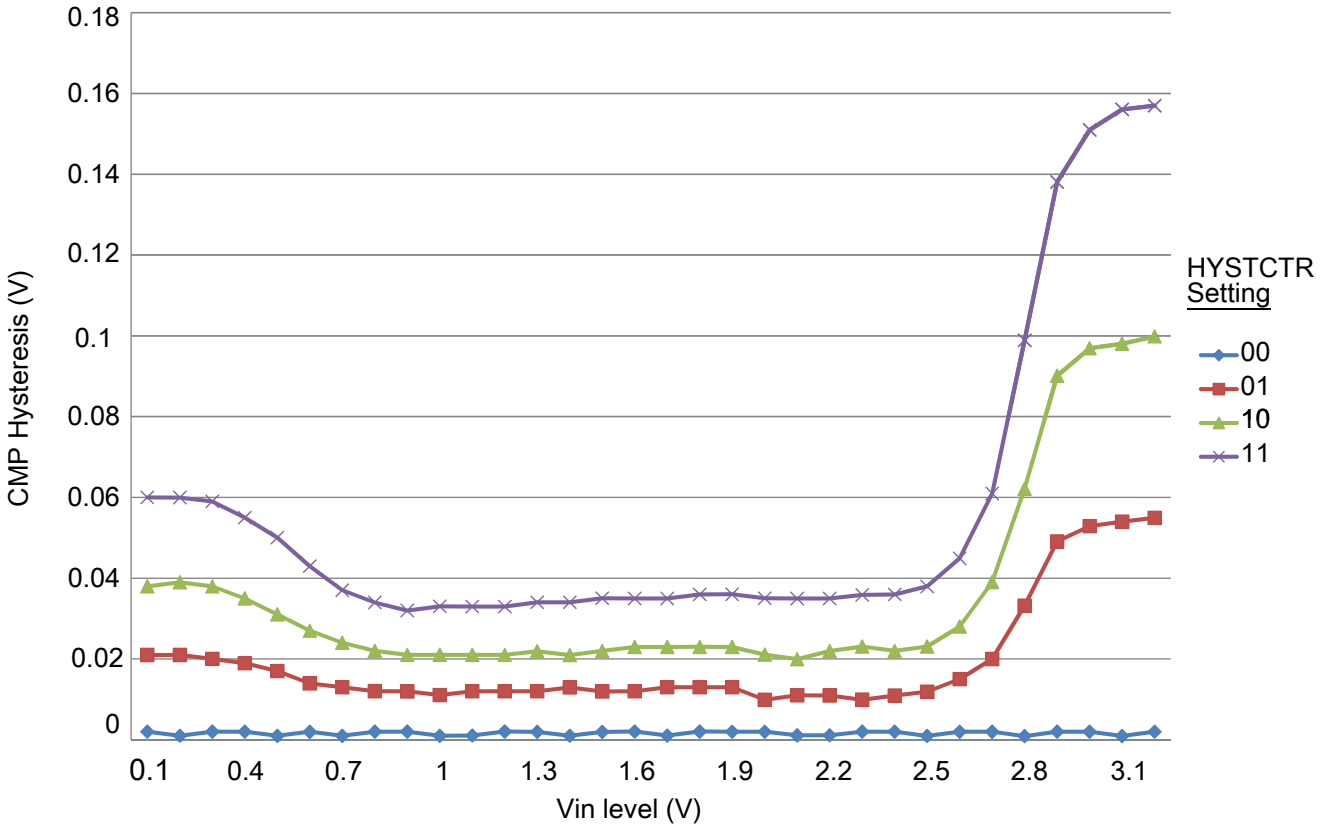


Figure 11. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

6.6.3 12-bit DAC electrical characteristics

6.6.3.1 12-bit DAC operating requirements

Table 25. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or V_{REFH}.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

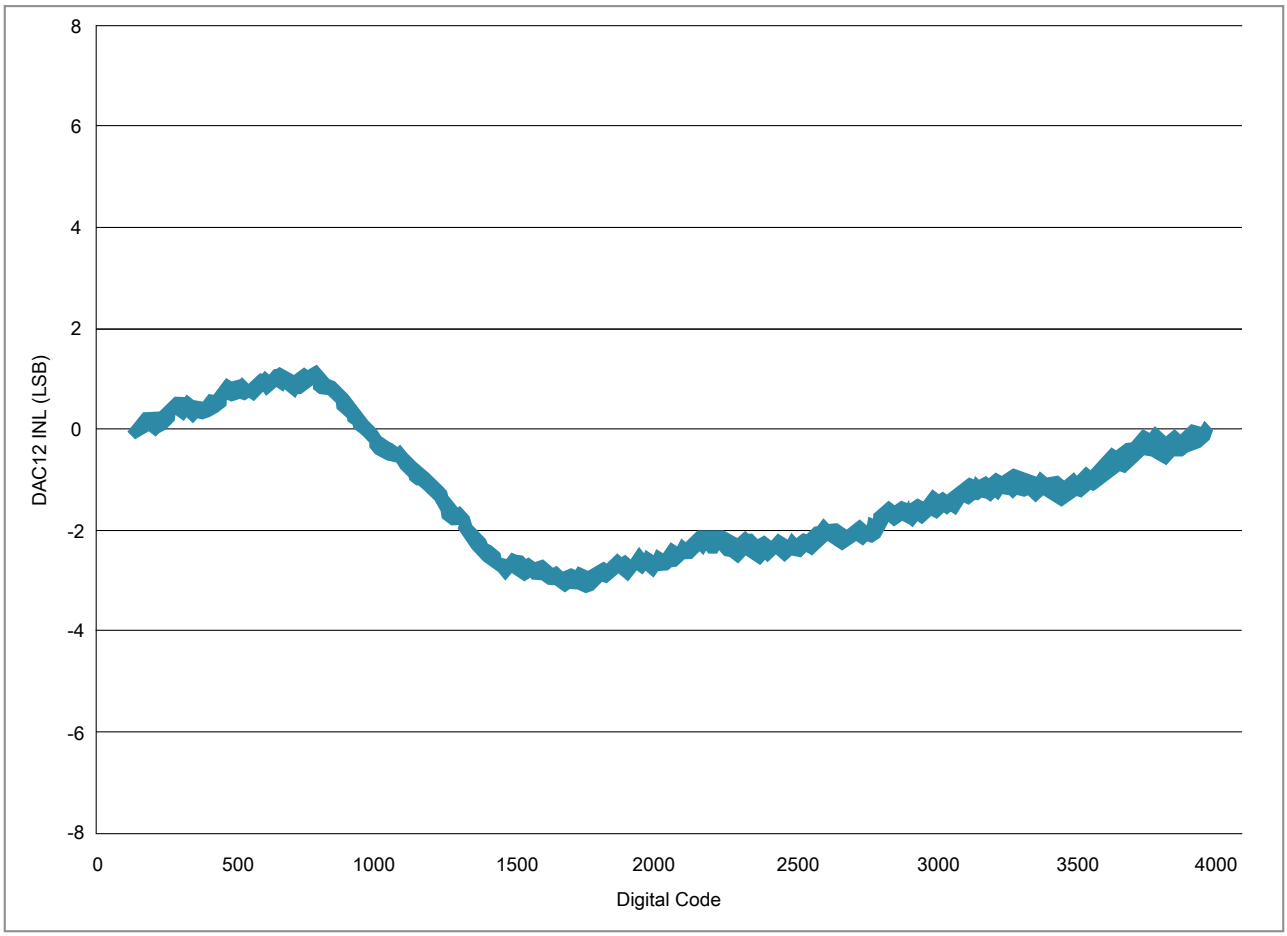


Figure 12. Typical INL error vs. digital code

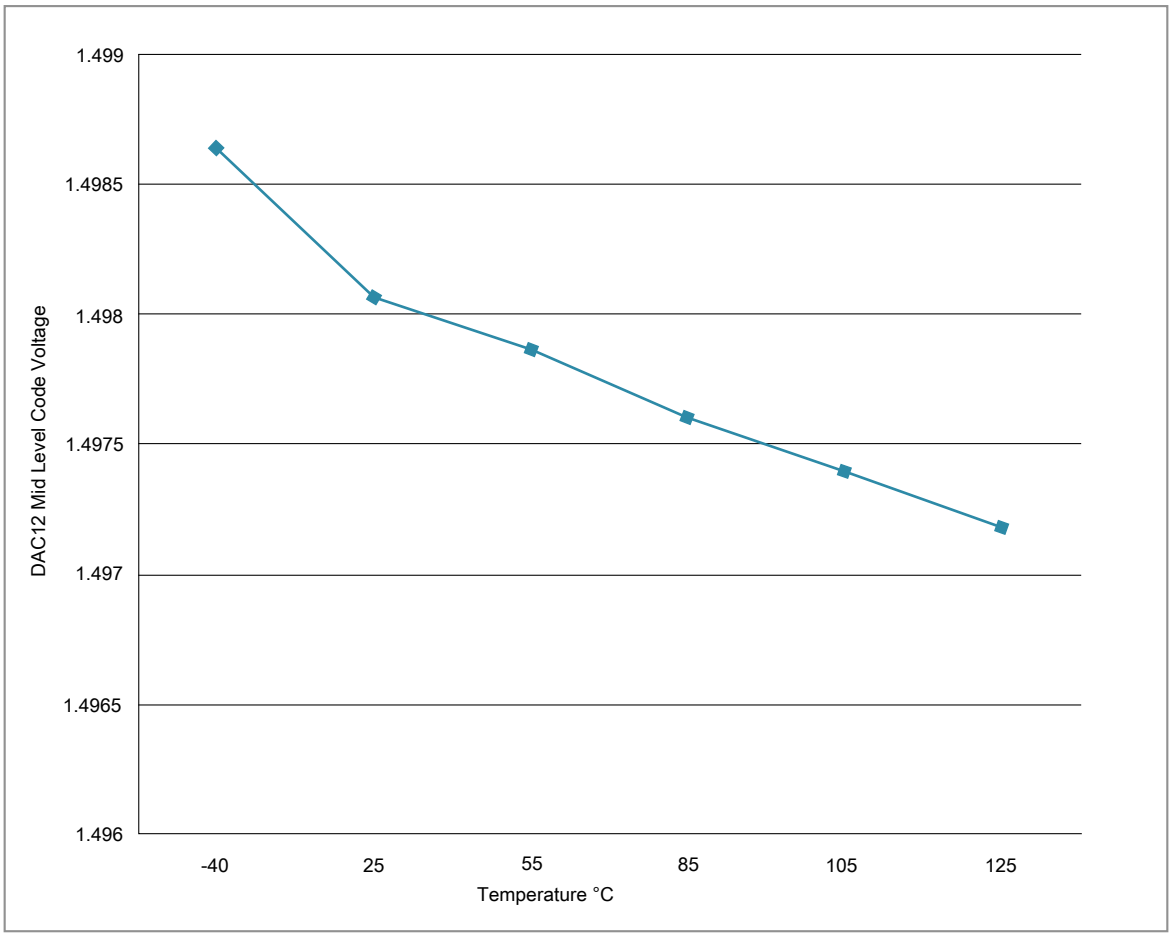


Figure 13. Offset at half scale vs. temperature

6.6.4 Voltage reference electrical specifications

Table 27. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	—
C_L	Output load capacitance	100		nF	1

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.

Table 28. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25C	1.1965	1.2	1.2027	V	
V_{out}	Voltage reference output — factory trim	1.144	—	1.266	V	

Table continues on the next page...

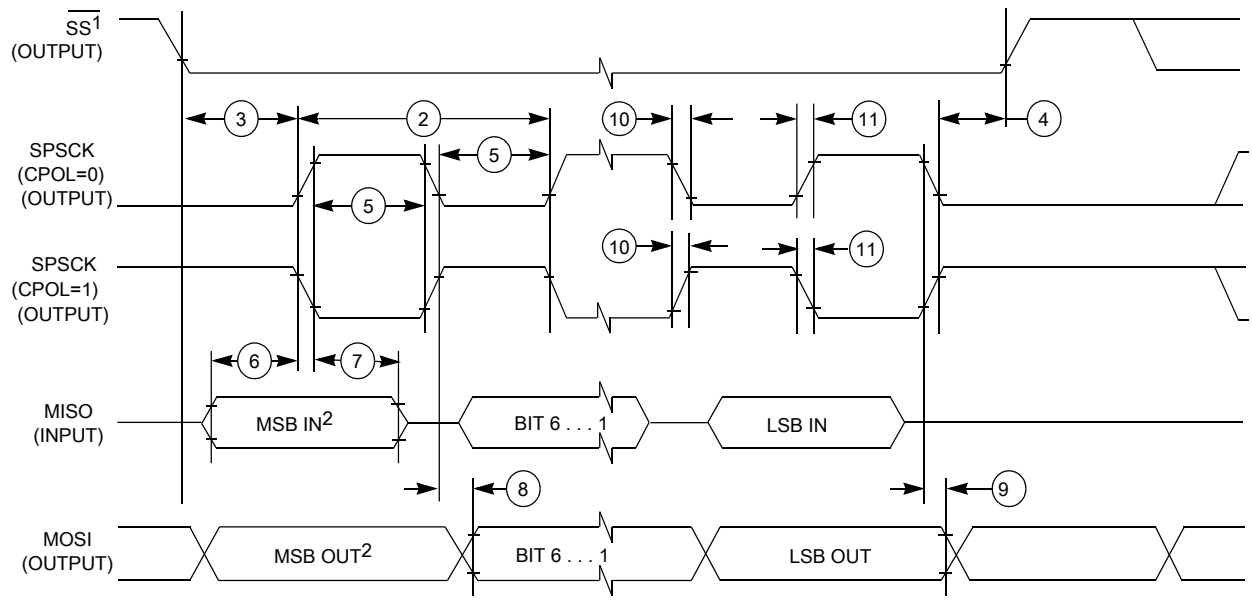
6.8.4 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless noted, as well as input signal transitions of 3 ns and a 50 pF maximum load on all SPI pins. All timing assumes slew rate control is disabled and high drive strength is enabled for SPI output pins.

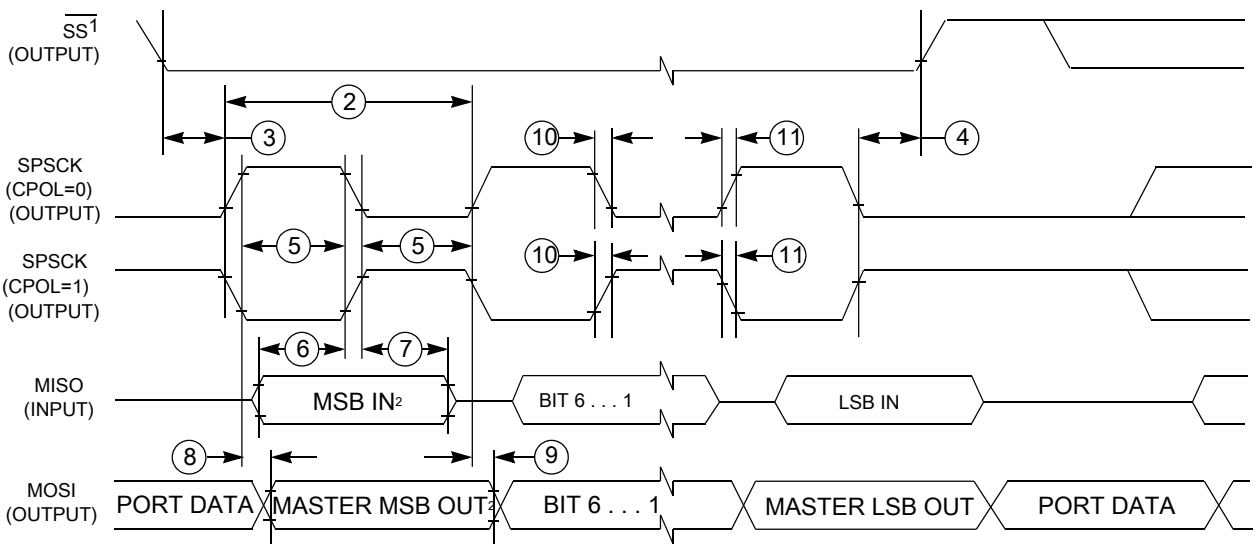
Table 33. SPI master mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	$f_{BUS}/2048$	$f_{BUS}/2$	Hz	f_{BUS} is the bus clock as defined in Table 8.
2	t_{SPSCK}	SPSCK period	2 x t_{BUS}	2048 x t_{BUS}	ns	t_{BUS} = 1/ f_{BUS}
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{BUS} - 30	1024 x t_{BUS}	ns	—
6	t_{SU}	Data setup time (inputs)	21	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_{v}	Data valid (after SPSCK edge)	—	25	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{BUS} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 14. SPI master mode timing (CPHA=0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 15. SPI master mode timing (CPHA=1)

Table 34. SPI slave mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	0	$f_{BUS}/4$	Hz	f_{BUS} is the bus clock as defined in Table 8.
2	t_{SPSCK}	SPSCK period	4 x t_{BUS}	—	ns	t_{BUS} = 1/ f_{BUS}

Table continues on the next page...

Table 34. SPI slave mode timing (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Comment
3	t_{Lead}	Enable lead time	1	—	t_{BUS}	—
4	t_{Lag}	Enable lag time	1	—	t_{BUS}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{BUS} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	19.5	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_a	Slave access time	—	t_{BUS}	ns	Time to data active from high-impedance state
9	t_{dis}	Slave MISO disable time	—	t_{BUS}	ns	Hold time to high-impedance state
10	t_v	Data valid (after SPSCK edge)	—	27	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{BUS} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

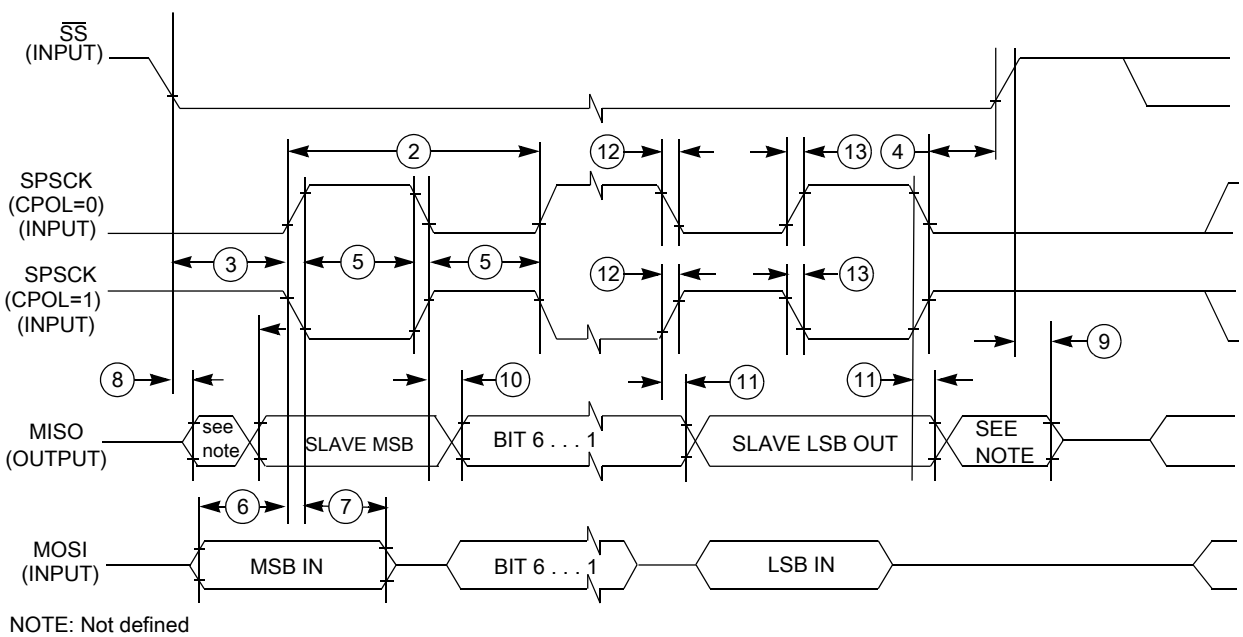


Figure 16. SPI slave mode timing (CPHA=0)

Table 35. I2S/SAI master mode timing (continued)

Num.	Characteristic	Min.	Max.	Unit
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns
S11	I2S_TX_FS input assertion to I2S_TXD output valid [2]	—	21	ns

1. This parameter is limited in VLPx modes.
2. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

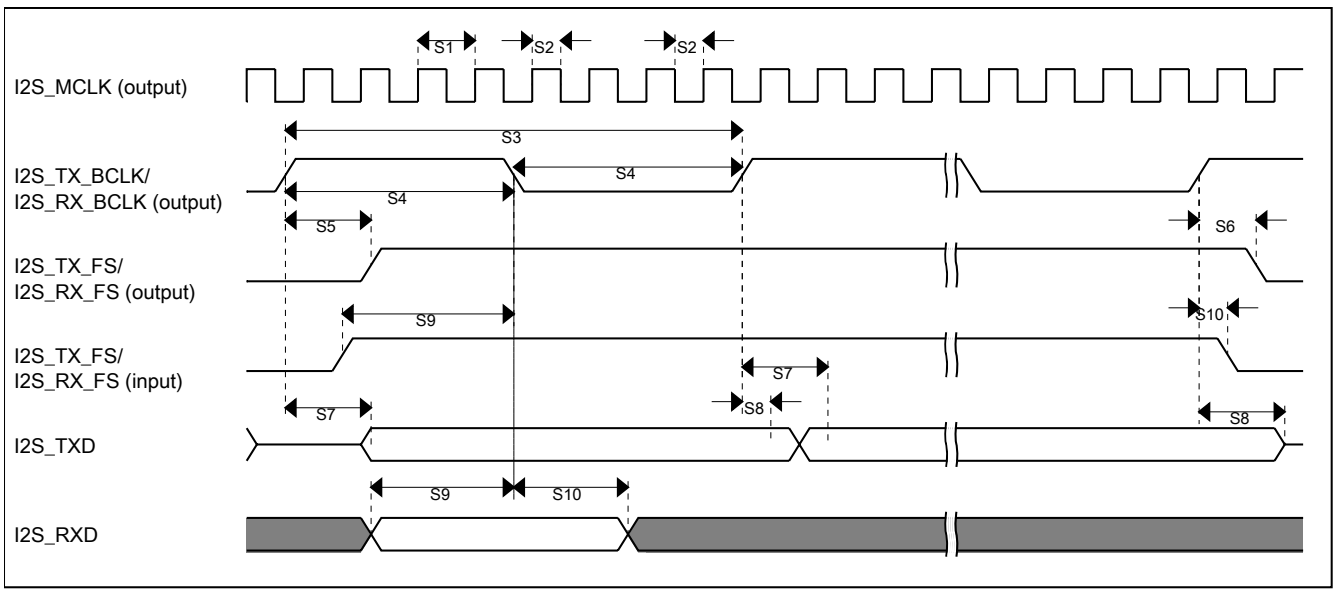


Figure 18. I2S/SAI timing — master modes

Table 36. I2S/SAI slave mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input) I2S_TX_BCLK cycle time (input)	80 160	— —	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	10	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	29	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	21	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

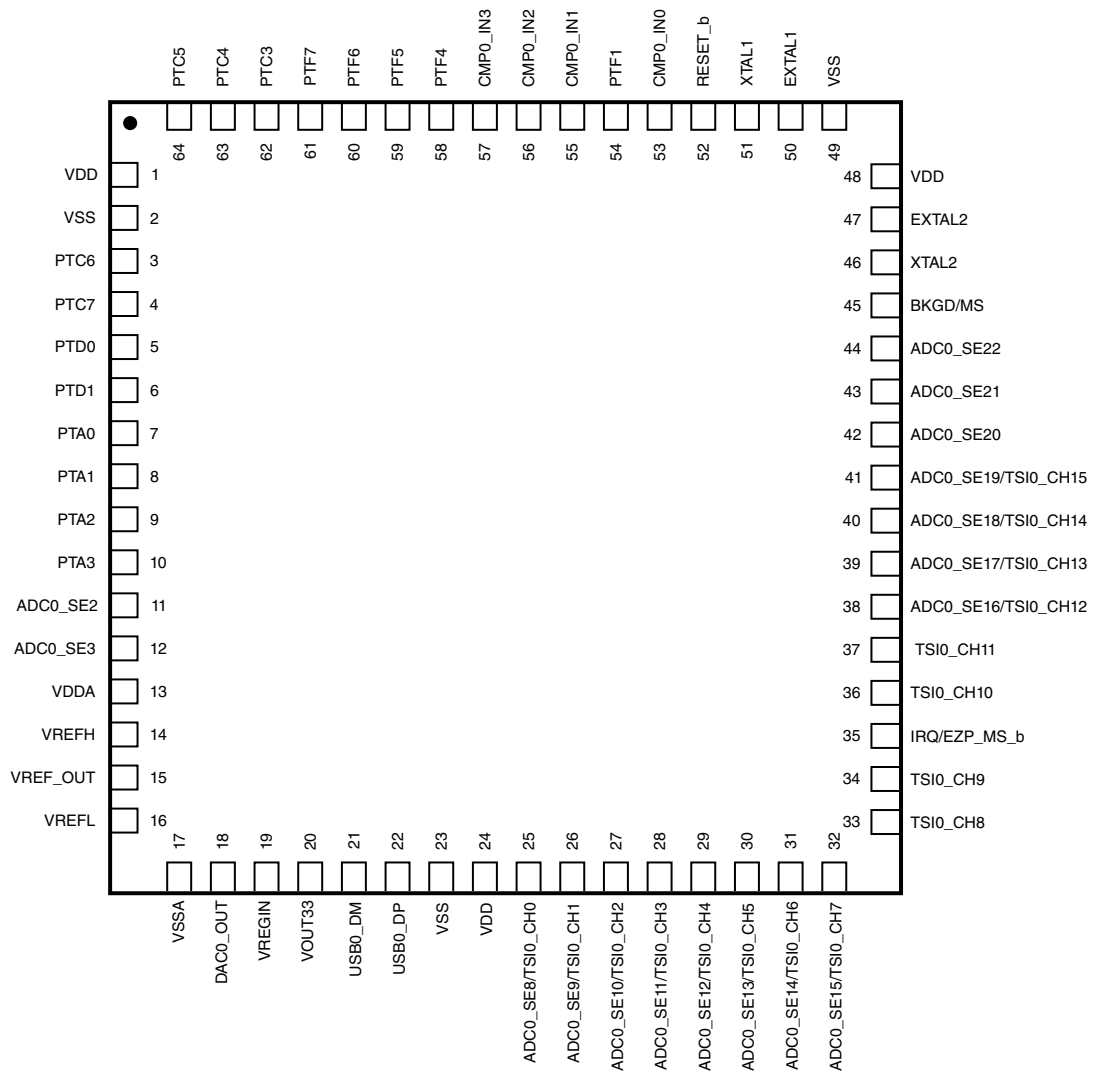


Figure 20. 64-pin LQFP

Table 38. Module signals by GPIO port and pin (continued)

64-pin	48-pin	44-pin	32-pin	Port	Module signal(s)
48	35	31	24		VDD
2					VSS
23	19	17	14		VSS
49	36	32	25		VSS
System					
45	32	28	21	PTB4	BKGD/MS
12	8	6	6	PTA5	CLKOUT
62	46	42	30	PTC3	CLKOUT
10	6	4	4	PTA3	EZP_CLK
11	7	5	5	PTA4	EZP_DI
12	8	6	6	PTA5	EZP_DO
35	25	23	17	PTB0	IRQ/EZP_MS_b, EZP_CS_b
52	39	35	28	PTC1	RESET_b
OSC					
50	37	33	26	PTB7	EXTAL1
47	34	30	23	PTB6	EXTAL2
51	38	34	27	PTC0	XTAL1
46	33	29	22	PTB5	XTAL2
LLWU					
4				PTC7	LLWU_P0
6	2			PTD1	LLWU_P1
12	8	6	6	PTA5	LLWU_P2
30	23	21	16	PTA7	LLWU_P3
32				PTD7	LLWU_P4
35	25	23	17	PTB0	LLWU_P5
36	26	24	18	PTB1	LLWU_P6
39	27	25	19	PTB2	LLWU_P7
44	31	27		PTE7	LLWU_P8
45	32	28	21	PTB4	LLWU_P9
55				PTF2	LLWU_P10
56	40	36		PTF3	LLWU_P11
57	41	37	29	PTC2	LLWU_P12
59	43	39		PTF5	LLWU_P13
62	46	42	30	PTC3	LLWU_P14
63	47	43	31	PTC4	LLWU_P15
RGPIO					
51	38	34	27	PTC0	RGPIO0
56	40	36		PTF3	RGPIO1
57	41	37	29	PTC2	RGPIO2

Table continues on the next page...

Table 38. Module signals by GPIO port and pin (continued)

64-pin	48-pin	44-pin	32-pin	Port	Module signal(s)
4				PTC7	I2C0_SDA
36	26	24	18	PTB1	I2C0_SDA
6	2			PTD1	I2C1_SCL
42	30			PTE5	I2C1_SCL
51	38	34	27	PTC0	I2C1_SCL
5	1			PTD0	I2C1_SDA
43				PTE6	I2C1_SDA
50	37	33	26	PTB7	I2C1_SDA
I2C2 and I2C3					
7	3	1	1	PTA0	I2C2_SCL
11	7	5	5	PTA4	I2C2_SCL
8	4	2	2	PTA1	I2C2_SDA
12	8	6	6	PTA5	I2C2_SDA
32				PTD7	I2C3_SCL
37				PTE2	I2C3_SCL
33				PTE0	I2C3_SDA
38				PTE3	I2C3_SDA
SPI0					
39	27	25	19	PTB2	SPI0_MISO
55				PTF2	SPI0_MISO
63	47	43	31	PTC4	SPI0_MISO
38				PTE3	SPI0_MOSI
40	28	26	20	PTB3	SPI0_MOSI
56	40	36		PTF3	SPI0_MOSI
64	48	44	32	PTC5	SPI0_MOSI
36	26	24	18	PTB1	SPI0_SCLK
54				PTF1	SPI0_SCLK
62	46	42	30	PTC3	SPI0_SCLK
7	3	1	1	PTA0	SPI0_SS
34				PTE1	SPI0_SS
53				PTF0	SPI0_SS
61	45	41		PTF7	SPI0_SS
SPI1					
4				PTC7	SPI1_MISO
11	7	5	5	PTA4	SPI1_MISO
43				PTE6	SPI1_MISO
59	43	39		PTF5	SPI1_MISO
3				PTC6	SPI1_MOSI
12	8	6	6	PTA5	SPI1_MOSI

Table continues on the next page...