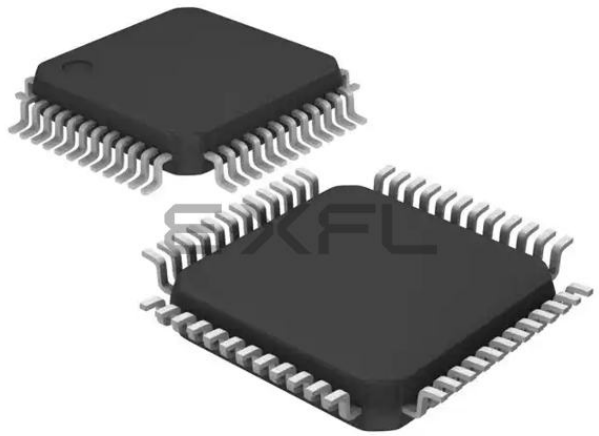

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 9x12b; D/A 1x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51jf64vhs

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device:

1. Go to www.freescale.com.
2. Perform a part number search for the following partial device numbers: PCF51JF and MCF51JF.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q CCCC DD MMM T PP

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
CCCC	Core code	CF51 = ColdFire V1
DD	Device number	JF, JU, QF, QH, QM, QU
MMM	Memory size (program flash memory)[1]	• 32 = 32 KB

Table continues on the next page...

Field	Description	Values
		• 64 = 64 KB • 128 = 128 KB
T	Temperature range, ambient (°C)	V = –40 to 105
PP	Package identifier	• FM = 32 QFN (5 mm x 5 mm) • HS = 44 Laminate QFN (5 mm x 5 mm) • LF = 48 LQFP (7 mm x 7 mm) • LH = 64 LQFP (10 mm x 10 mm)

1. All parts also have FlexNVM, FlexRAM, and RAM.

2.4 Example

This is an example part number:

MCF51JF128VLH

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

3.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

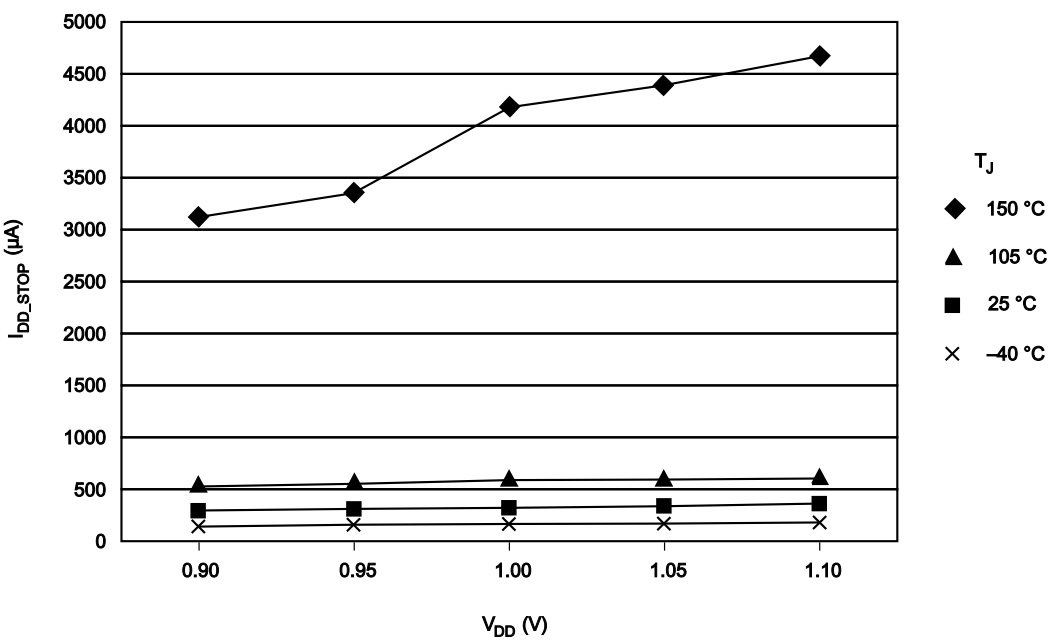
3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



5.2.5 Power consumption operating behaviors

Table 5. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from RAM • @ 1.8 V • @ 3.0 V	— —	13 13	— 16	mA mA	2
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash memory with page buffering disabled • @ 1.8 V • @ 3.0 V	— —	14.3 14.5	— 17.9	mA mA	2
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from RAM, exercising flash memory • @ 1.8 V • @ 3.0 V	— —	20 20	23.5 25	mA mA	3
I_{DD_WAIT}	Wait mode current at 3.0 V — all peripheral clocks disabled	—	5.8	6.8	mA	4
I_{DD_STOP}	Stop mode current at 3.0 V • @ –40 to 25 °C • @ 105 °C	— —	0.34 0.90	0.41 1.8	mA mA	
I_{DD_VLPR}	Very low-power run mode current at 3.0 V — all peripheral clocks disabled	—	0.63	1.32	mA	5
I_{DD_VLPR}	Very low-power run mode current at 3.0 V — all peripheral clocks enabled	—	0.78	1.46	mA	6
I_{DD_VLPW}	Very low-power wait mode current at 3.0 V	—	0.15	0.62	mA	7
I_{DD_VLPS}	Very low-power stop mode current at 3.0 V • @ –40 to 25 °C • @ 105 °C	— —	19 145	45 312	µA	8
I_{DD_LLS}	Low leakage stop mode current at 3.0 V • @ –40 to 25 °C • @ 105 °C	— —	3.0 53.3	4.8 157	µA µA	8,9,10
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V • @ –40 to 25 °C • @ 105 °C	— —	1.8 39.2	3.3 115	µA µA	8,9,10
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V	— —	1.6 22.2	2.8 65	µA µA	8,9

Table continues on the next page...

Table 5. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• @ –40 to 25 °C • @ 105 °C					
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V • @ –40 to 25 °C • @ 105 °C	— —	1.4 17.6	2.6 50	µA µA	8,9
I_{DD_RTC}	Average current adder for real-time clock function • @ –40 to 25 °C	—	0.7	—	µA	11

1. The analog supply current is the sum of the active current for each of the analog modules on the device. See each module's specification for its supply current.
2. 50 MHz core and system clocks, and 25 MHz bus clock. MCG configured for FEI mode. All peripheral clocks disabled.
3. 50 MHz core and system clocks, and 25 MHz bus clock. MCG configured for FEI mode. All peripheral clocks enabled, but peripherals are not in active operation.
4. 50 MHz core and system clocks, and 25 MHz bus clock. MCG configured for FEI mode.
5. 2 MHz core and system clocks, and 1 MHz bus clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash memory.
6. 2 MHz core and system clocks, and 1 MHz bus clock. MCG configured for BLPE mode. All peripheral clocks enabled, but peripherals are not in active operation. Code executing from flash memory.
7. 2 MHz core and system clocks, and 1 MHz bus clock. MCG configured for BLPE mode. All peripheral clocks disabled.
8. OSC clocks disabled.
9. All pads disabled.
10. Data reflects devices with 32 KB of RAM. For devices with 16 KB of RAM, power consumption is reduced by 500 nA. For devices with 8 KB of RAM, power consumption is reduced by 750 nA.
11. RTC function current includes LPTMR with OSC enabled with 32.768 kHz crystal at 3.0 V

5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode, except for 50 MHz core (FEI mode)
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL
- For the ALLON curve, all peripheral clocks are enabled, but peripherals are not in active operation
- USB Voltage Regulator disabled
- No GPIOs toggled
- Code execution from flash memory with cache enabled

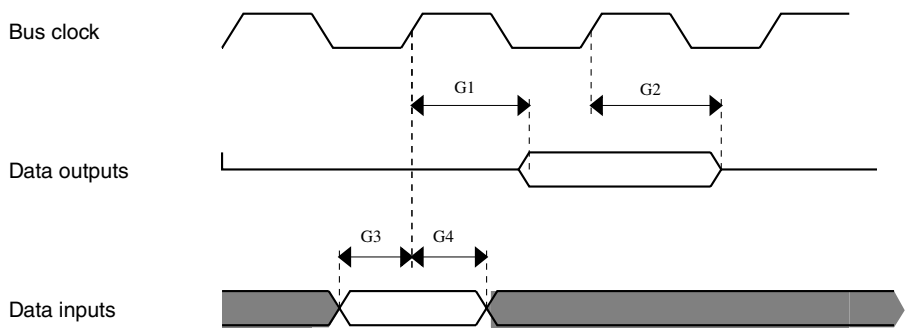


Figure 3. EGPIO timing diagram

The following general purpose specifications apply to all signals configured for RGPIO, FTM, and UART. The conditions are 25 pf load, V_{DD} = 3.6 V to 1.71 V, and full temperature range. The GPIO are set for high drive, no slew rate control, and no input filter, digital or analog, unless otherwise specified.

Table 10. RGPIO General Control Timing

Symbol	Description	Min.	Max.	Unit
R1	CPUCLK from CLK_OUT pin high to GPIO output valid	—	16	ns
R2	CPUCLK from CLK_OUT pin high to GPIO output invalid (output hold)	1	—	ns
R3	GPIO input valid to bus clock high	17	—	ns
R4	CPUCLK from CLK_OUT pin high to GPIO input invalid	—	2	ns

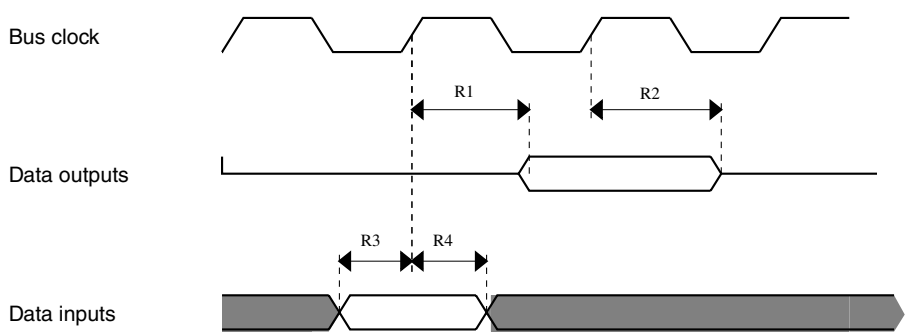


Figure 4. RGPIO timing diagram

5.4 Thermal specifications

5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	115	°C
T_A	Ambient temperature	–40	105	°C

5.4.2 Thermal attributes

Board type	Symbol	Description	64 LQFP	48 LQFP	44 Laminate QFN	32 QFN	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	73	79	108	98	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	54	55	69	33	°C/W	1
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	61	66	91	81	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	48	48	63	28	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	37	34	44	13	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	20	20	31	2.2	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	5.0	4.0	6.0	6.0	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions —Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions —Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions —Natural Convection (Still Air)*.

Table 13. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
J_{cyc_pll}	PLL period jitter (RMS)					8
	• f_{vco} = 48 MHz	—	120	—	ps	
	• f_{vco} = 100 MHz	—	50	—	ps	
J_{acc_pll}	PLL accumulated jitter over 1µs (RMS)					8
	• f_{vco} = 48 MHz	—	1350	—	ps	
	• f_{vco} = 100 MHz	—	600	—	ps	
D_{lock}	Lock entry frequency tolerance	± 1.49	—	± 2.98	%	
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll\_ref})$	s	9

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

6.3.2 Oscillator electrical specifications

6.3.2.1 Oscillator DC electrical specifications

Table 14. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 1 MHz	—	200	—	µA	
	• 4 MHz	—	200	—	µA	
	• 8 MHz (RANGE=01)	—	300	—	µA	
		—	950	—	µA	

Table continues on the next page...

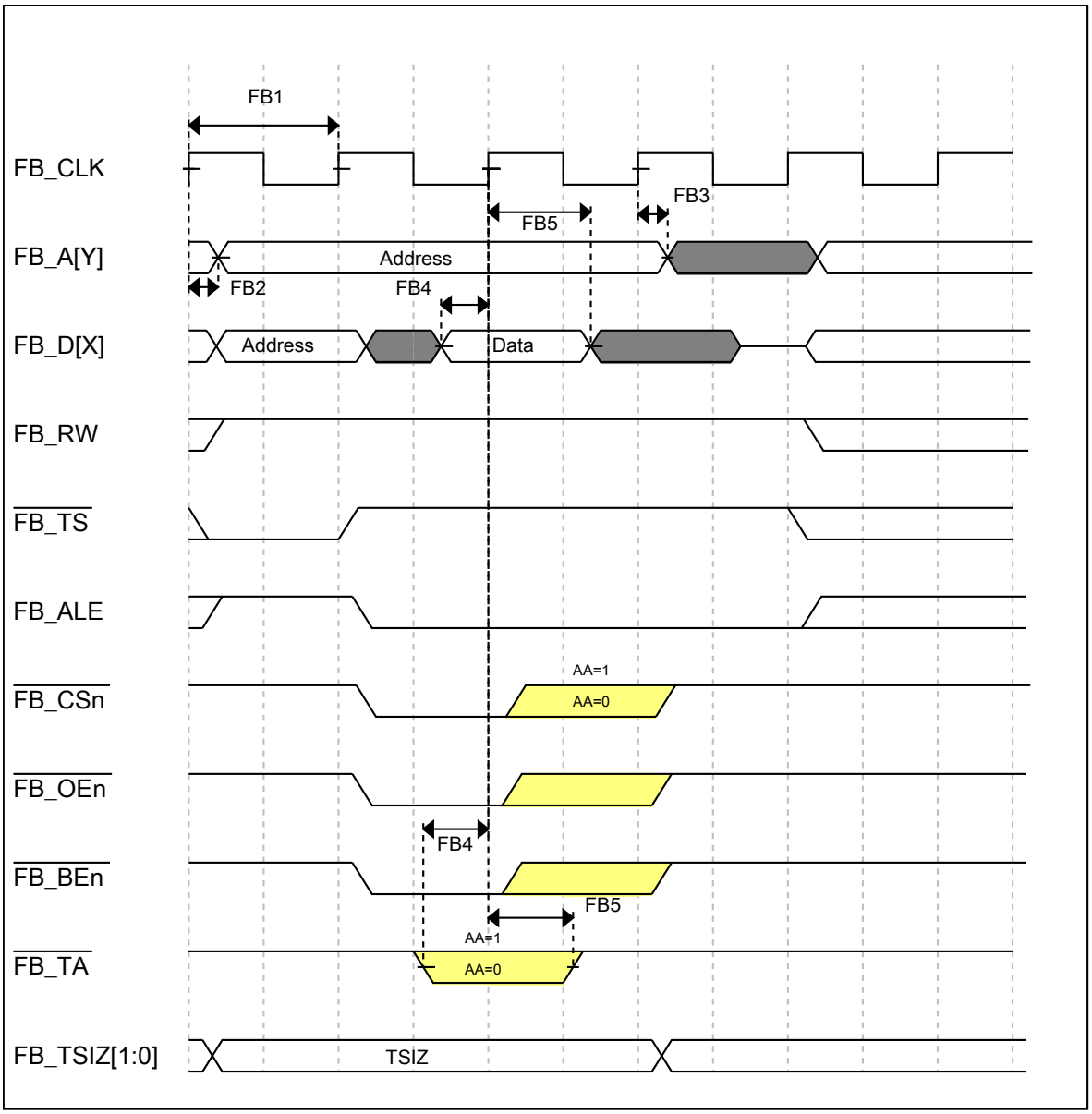


Figure 6. Mini-FlexBus read timing diagram

6.6.2 CMP and 6-bit DAC electrical specifications

Table 24. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}–0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

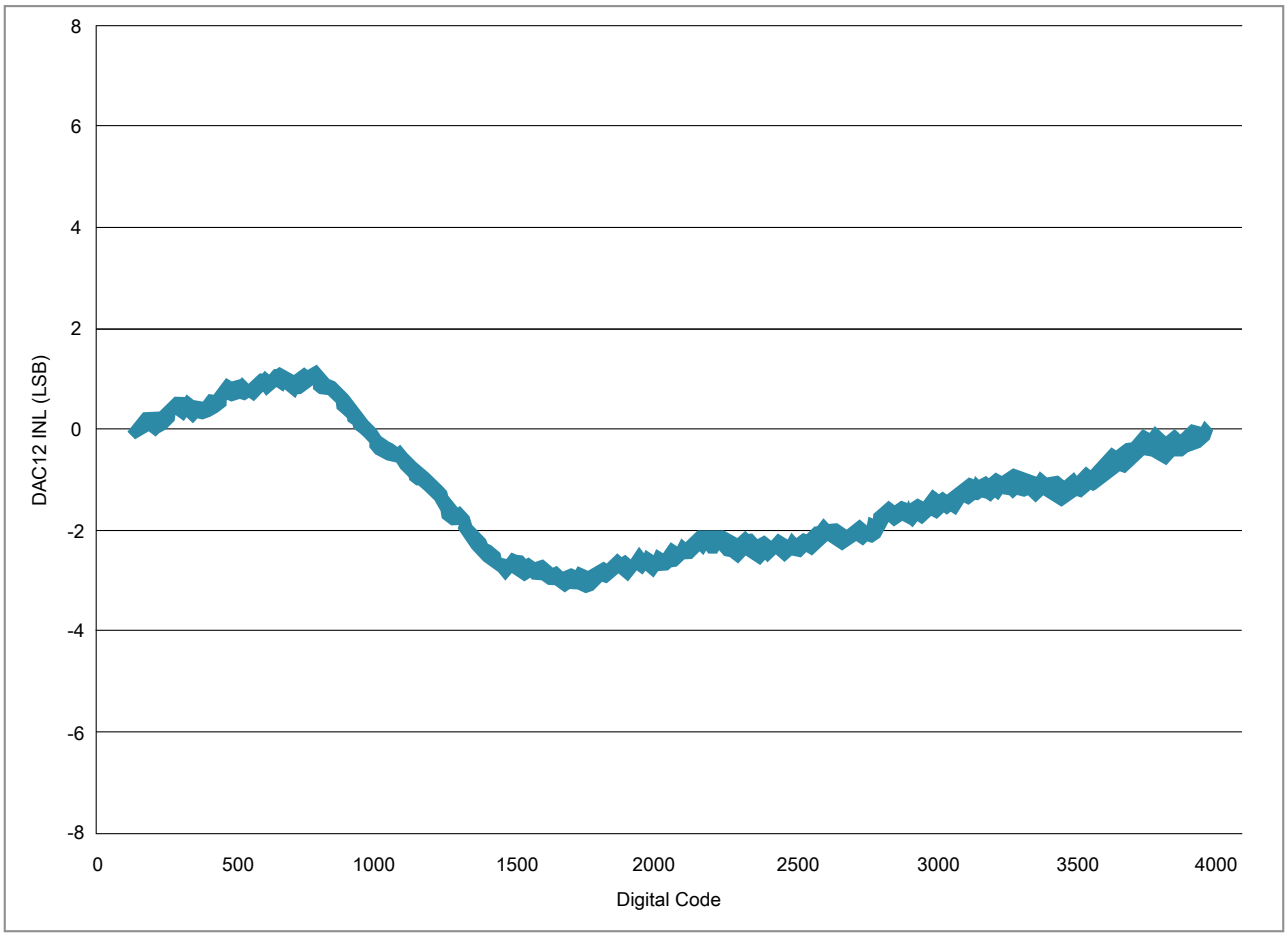


Figure 12. Typical INL error vs. digital code

NOTE

6.8.2 USB DCD electrical specifications

Table 31. USB0 DCD electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DP_SRC}	USB_DP source voltage (up to 250 µA)	0.5	—	0.7	V
V_{LGC}	Threshold voltage for logic high	0.8	—	2.0	V
I_{DP_SRC}	USB_DP source current	7	10	13	µA
I_{DM_SINK}	USB_DM sink current	50	100	150	µA
R_{DM_DWN}	D- pulldown resistance for data pin contact detect	14.25	—	24.8	kΩ
V_{DAT_REF}	Data detect voltage	0.25	0.33	0.4	V

6.8.3 USB VREG electrical specifications

Table 32. USB VREG electrical specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
VREGIN	Input supply voltage	2.7	—	5.5	V	
I_{DDon}	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	—	120	186	µA	
I_{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.1	10	µA	
I_{DDoff}	Quiescent current — Shutdown mode • VREGIN = 5.0 V and temperature=25 °C • Across operating voltage and temperature	— —	650 —	— 4	nA µA	
$I_{LOADrun}$	Maximum load current — Run mode	—	—	120	mA	
$I_{LOADstby}$	Maximum load current — Standby mode	—	—	1	mA	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) > 3.6 V • Run mode • Standby mode	 3 2.1	 3.3 2.8	 3.6 3.6	 V V	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode	2.1	—	3.6	V	2
C_{OUT}	External output capacitor	1.76	2.2	8.16	µF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I_{LIM}	Short circuit current	—	290	—	mA	

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.
2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I_{Load}.

6.8.4 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless noted, as well as input signal transitions of 3 ns and a 50 pF maximum load on all SPI pins. All timing assumes slew rate control is disabled and high drive strength is enabled for SPI output pins.

Table 33. SPI master mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	$f_{BUS}/2048$	$f_{BUS}/2$	Hz	f_{BUS} is the bus clock as defined in Table 8.
2	t_{SPSCK}	SPSCK period	2 x t_{BUS}	2048 x t_{BUS}	ns	t_{BUS} = 1/ f_{BUS}
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{BUS} - 30	1024 x t_{BUS}	ns	—
6	t_{SU}	Data setup time (inputs)	21	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_{v}	Data valid (after SPSCK edge)	—	25	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{BUS} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

Table 34. SPI slave mode timing (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Comment
3	t_{Lead}	Enable lead time	1	—	t_{BUS}	—
4	t_{Lag}	Enable lag time	1	—	t_{BUS}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{BUS} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	19.5	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_a	Slave access time	—	t_{BUS}	ns	Time to data active from high-impedance state
9	t_{dis}	Slave MISO disable time	—	t_{BUS}	ns	Hold time to high-impedance state
10	t_v	Data valid (after SPSCK edge)	—	27	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{BUS} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

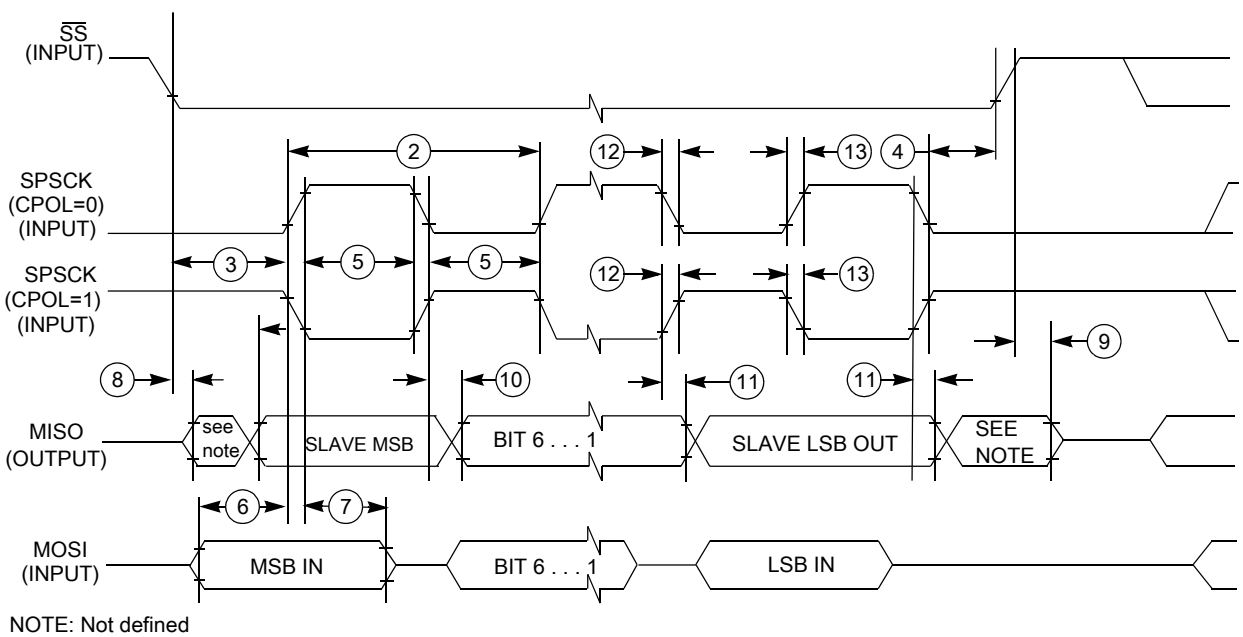


Figure 16. SPI slave mode timing (CPHA=0)

Table 35. I2S/SAI master mode timing (continued)

Num.	Characteristic	Min.	Max.	Unit
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns
S11	I2S_TX_FS input assertion to I2S_TXD output valid [2]	—	21	ns

1. This parameter is limited in VLPx modes.
2. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

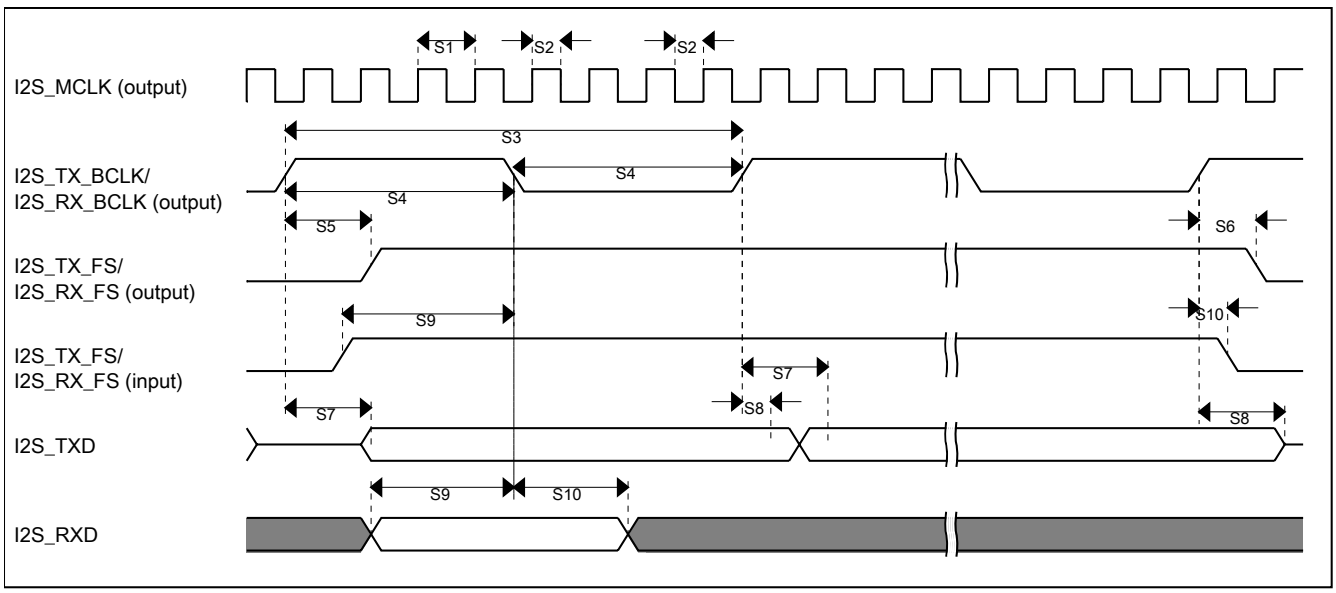


Figure 18. I2S/SAI timing — master modes

Table 36. I2S/SAI slave mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input) I2S_TX_BCLK cycle time (input)	80 160	— —	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	10	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	29	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	21	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

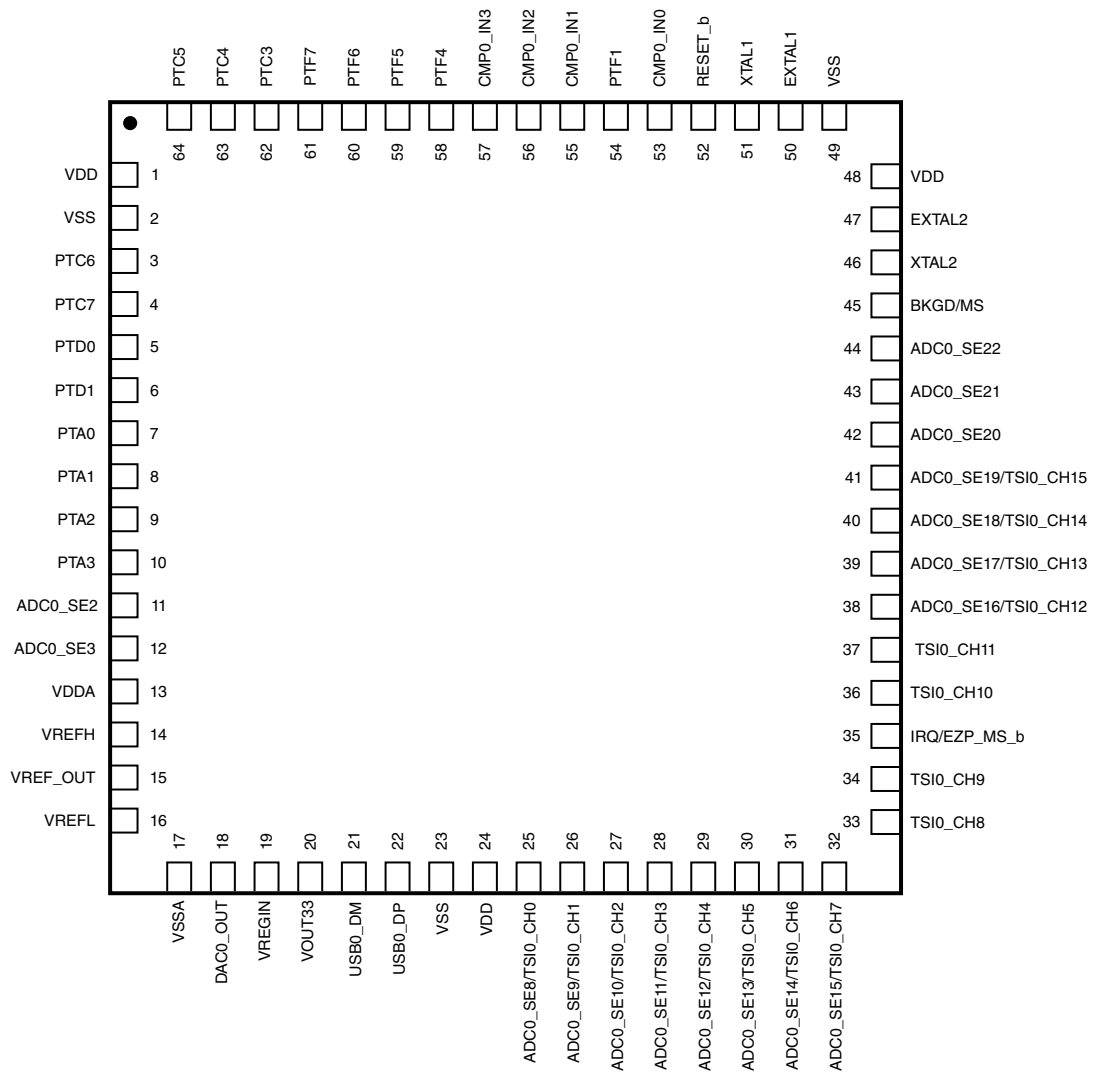


Figure 20. 64-pin LQFP

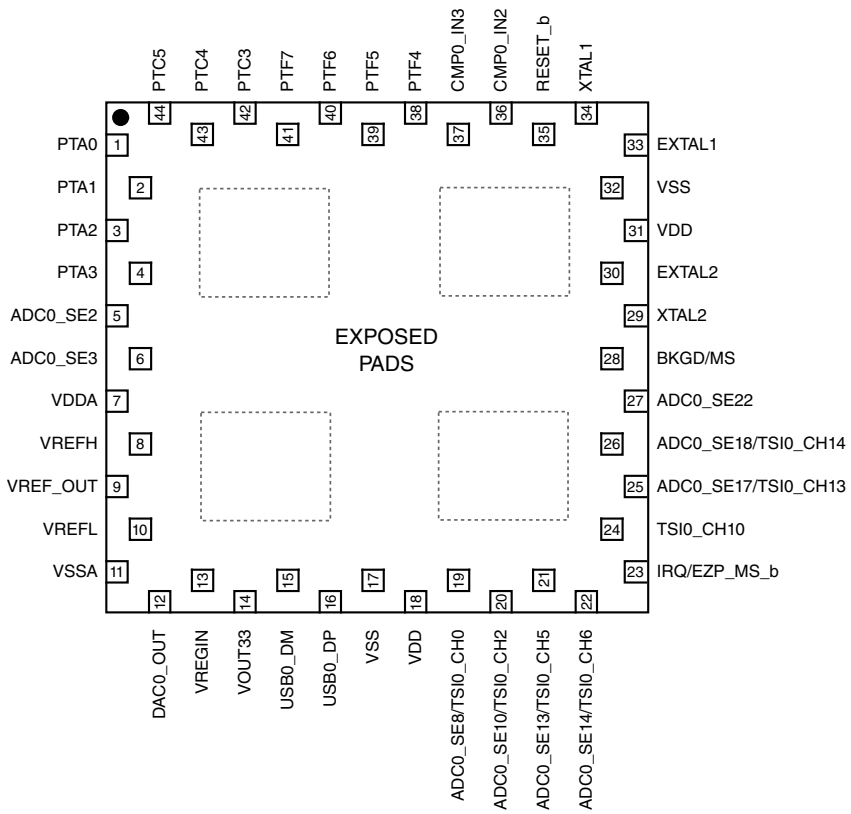


Figure 22. 44-pin Laminate QFN

Table 38. Module signals by GPIO port and pin (continued)

64-pin	48-pin	44-pin	32-pin	Port	Module signal(s)
PDB0					
44	31	27		PTE7	PDB0_EXTRG
63	47	43	31	PTC4	PDB0_EXTRG
FTM0					
34				PTE1	FTM_FLT0
25	21	19	15	PTA6	FTM_FLT1
36	26	24	18	PTB1	FTM_FLT2 / FTM0_QD_PHB
26				PTD2	FTM0_CH0/ FTM0_QD_PHA
27	22	20		PTD3	FTM0_CH1 / FTM0_QD_PHB
30	23	21	16	PTA7	FTM0_QD_PHA
51	38	34	27	PTC0	TMR_CLKIN0
50	37	33	26	PTB7	TMR_CLKIN1
FTM1					
34				PTE1	FTM_FLT0
25	21	19	15	PTA6	FTM_FLT1
36	26	24	18	PTB1	FTM_FLT2
7	3	1	1	PTA0	FTM1_CH0
8	4	2	2	PTA1	FTM1_CH1
9	5	3	3	PTA2	FTM1_CH2
10	6	4	4	PTA3	FTM1_CH3
11	7	5	5	PTA4	FTM1_CH4
12	8	6	6	PTA5	FTM1_CH5
51	38	34	27	PTC0	TMR_CLKIN0
50	37	33	26	PTB7	TMR_CLKIN1
MTIM					
51	38	34	27	PTC0	TMR_CLKIN0
50	37	33	26	PTB7	TMR_CLKIN1
Mini-FlexBus					
36	26	24	18	PTB1	FB_CLKOUT
27	22	20		PTD3	FBa_AD0
41	29			PTE4	FBa_AD1
42	30			PTE5	FBa_AD2
43				PTE6	FBa_AD3
44	31	27		PTE7	FBa_AD4
53				PTF0	FBa_AD5
54				PTF1	FBa_AD6
55				PTF2	FBa_AD7

Table continues on the next page...

9 Revision History

The following table summarizes content changes since the previous release of this document.

Table 39. Revision History

Rev. No.	Date	Substantial Changes
7	03/2015	• Updated the value and description in Power mode transition operating behaviors • Updated the maximum value of f_{fll_ref} in MCG specs • 12-bit ADC characteristics: Updated the values of temperature sensor slope for -40°C to 25°C and 25°C to 105°C • Updated the minimum and typical values of V_{out} in VREF full-range operating behaviors • Updated the maximum internal reference frequency and maximum FLL reference frequency range in MCG specifications • Updated the values of Temperature sensor voltage in 12-bit ADC characteristics • Removed the temperature parameter from VREF full-range operating requirements table • Removed Write endurance to FlexRAM for EEPROM section • Removed ADC calculator tool footnote from ADC operating conditions