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Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Automotive
Core Processor	S12
Program Memory Type	FLASH (32KB)
Controller Series	HCS12
RAM Size	2K x 8
Interface	LIN, SCI
Number of I/O	9
Voltage - Supply	2.25V ~ 5.5V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	48-LQFP Exposed Pad
Supplier Device Package	48-HLQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm912f634dv1aer2

3.5 Static Electrical Characteristics

Static electrical characteristics noted under conditions 5.5V ≤ VSUP ≤ 18 V, -40 °C ≤ T_A ≤ 105 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions unless otherwise noted.

3.5.1 Static Electrical Characteristics Analog Die

Table 10. Static Electrical Characteristics - Power Supply

Ratings	Symbol	Min	Typ	Max	Unit
Power-On Reset (POR) Threshold (measured on VS1)	V_{POR}	1.5	-	3.5	V
Low Voltage Warning (LVI) Threshold (measured on VS1, falling edge) Hysteresis (measured on VS1)	 V_{LVI} V_{LVI_H}	 5.55 -	 6.0 1.0	 6.6 -	V
High Voltage Warning (HVI) Threshold (measured on VS2, rising edge) Hysteresis (measured on VS2)	 V_{HVI} V_{HVI_H}	 18 -	 19.25 1.0	 20.5 -	V
Low Battery Warning (LBI) Threshold (measured on VSENSE, falling edge) Hysteresis (measured on VSENSE)	 V_{LBI} V_{LBI_H}	 5.55 -	 6.0 1.0	 6.6 -	V
J2602 Under-voltage threshold	$V_{J2602UV}$	5.5	5.7	6.2	V
Low VDDX Voltage (LVRX) Threshold	V_{LVRX}	2.7	3.0	3.3	V
Low VDD Voltage Reset (LVR) Threshold Normal Mode	V_{LVR}	2.30	2.35	2.4	V
Low VDD Voltage Reset (LVR) Threshold Stop Mode [16]	V_{LVRS}	1.6	1.85	2.1	V
VDD Over-voltage Threshold (VROV)	V_{VDDOV}	2.575	2.7875	3.0	V
VDDX Over-voltage Threshold (VROVX)	V_{VDDXOV}	5.25	5.675	6.1	V

Note:
16. See MM912F634ER, MM912F634, Silicon Analog Mask (M91W) / Digital Mask (M33G) Errata

Table 11. Static Electrical Characteristics - Resets

Ratings	Symbol	Min	Typ	Max	Unit
Low-state Output Voltage I_{OUT} = 2.0 mA	V_{OL}	-	-	0.8	V
Pull-up Resistor	R_{RPU}	25	-	50	kOhm
Low-state Input Voltage	V_{IL}	-	-	$0.3V_{DDX}$	V
High-state Input Voltage	V_{IH}	$0.7V_{DDX}$	-	-	V
Reset Release Voltage (VDDX)	V_{RSTRV}	-	1.5	-	V
RESET_A pin Current Limitation		5.0	7.5	10	mA

Table 12. Static Electrical Characteristics - Window Watchdog

Ratings	Symbol	Min	Typ	Max	Unit
Watchdog Disable Voltage (fixed voltage)	V_{TST}	7.0	-	10	V
Watchdog Enable Voltage (fixed voltage)	V_{TSTEN}	-	-	5.5	V

Table 13. Static Electrical Characteristics - Voltage Regulator 5V (VDDX)

Ratings	Symbol	Min	Typ	Max	Unit
Normal Mode Output Voltage 1.0 mA < I_{VDDX} + $I_{VDDXINTERNAL}$ < 80 mA; 5.5 V < V_{SUP} < 27 V [17]	V_{DDXRUN}	4.75	5.00	5.25	V
Normal Mode Output Current Limitation (I_{VDDX})	$I_{VDDXLIMRUN}$	80	130	200	mA

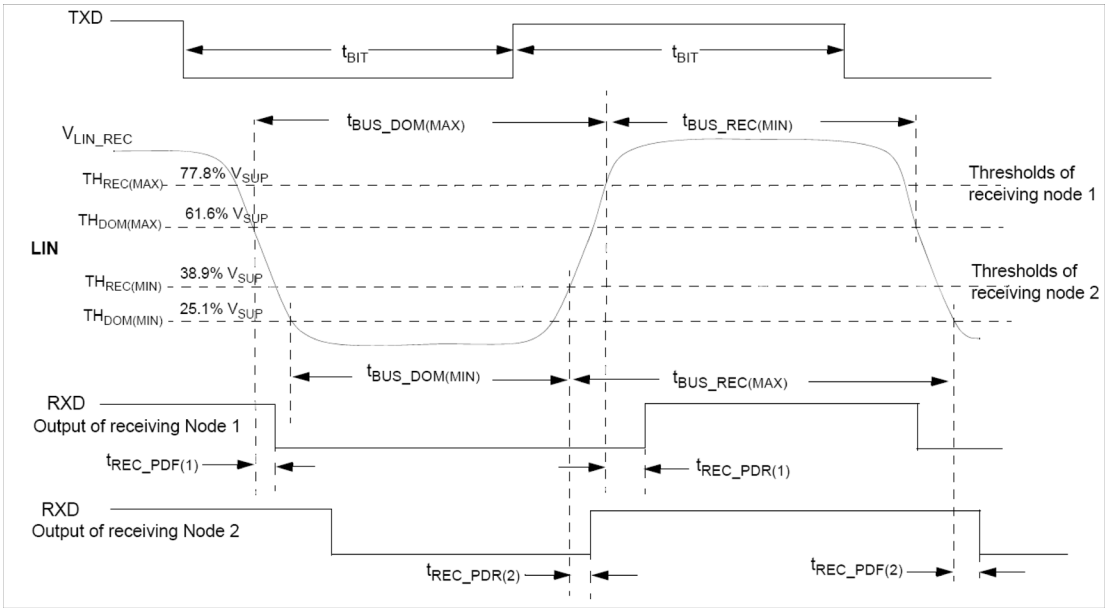


Figure 7. LIN Timing Measurements for Slow Baud Rate

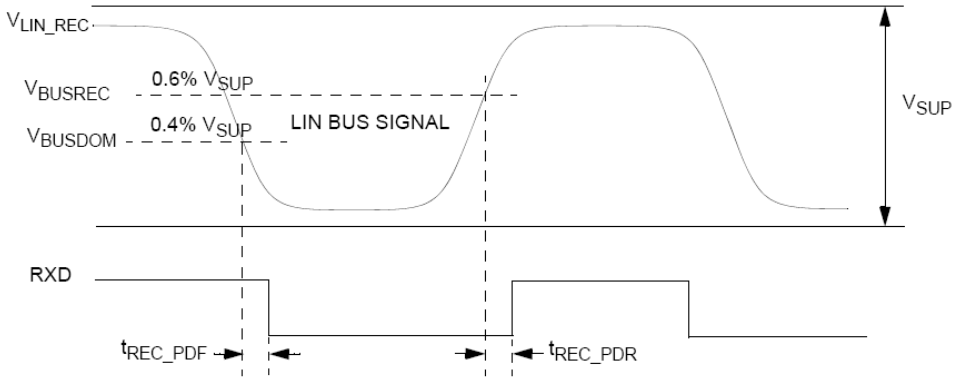


Figure 8. LIN Receiver Timing

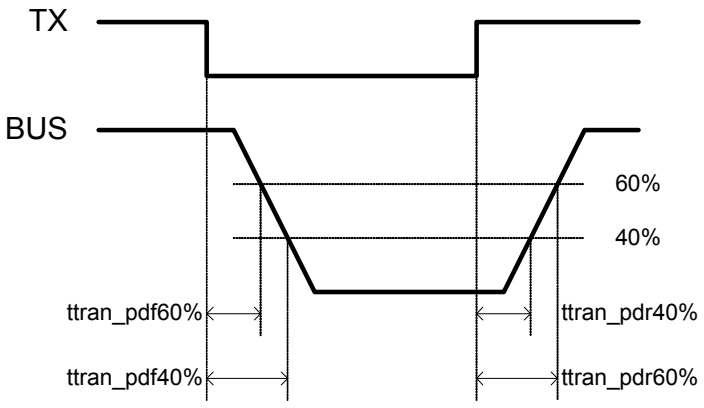


Figure 9. LIN Transmitter Timing

3.6.2.1.5 Blank Check

The time it takes to perform a blank check on the Flash is dependant on the location of the first non-blank word, starting at relative address zero. It takes one bus cycle per word to verify plus a setup of the command.

$$t_{check} \text{ a location } \text{Þ } t_{cyc} + 10 \text{ Þ } t_{cyc}$$

Table 37. NVM Timing Characteristics

Rating	Symbol	Min	Typ	Max	Unit
Bus frequency for programming or erase operations	f_{NVMBUS}	1.0	-	-	MHz
Operating frequency	f_{NVMOP}	150	-	200	kHz
Single word programming time	t_{SWPGM}	46(36)	-	74.5(36)	µs
Flash burst programming consecutive word	t_{BWPGM}	20.4(36)	-	31(37)	µs
Flash burst programming time for 64 words(39)	t_{BRPGM}	1331.2(36)	-	2027.5(37)	µs
Sector erase time(37)	t_{ERA}	20(38)	-	26.7(37)	ms
Mass erase time	t_{MASS}	100(40)	-	133(37)	ms
Blank check time Flash per block	t_{CHECK}	11(39)	-	65546(40)	t_{CYC}

Note:
36. Minimum programming times are achieved under maximum NVM operating frequency f_{NVMOP} and maximum bus frequency f_{BUS}.
37. The sector erase cycle is divided into 16 individual erase pulses to achieve faster system response during the erase flow. The given erase time (t_{ERA}) specifies the time considering consecutive pulses.
38. Minimum erase times are achieved under maximum NVM operating frequency, f_{NVMOP}.
39. Minimum time, if first word in the array is not blank.
40. Maximum time to complete check on an erased block.

Table 65. Analog die Registers[60] - 0x0200–0x02FF D2D Blocking Access (D2DI) 2 of 3/ 0x0300–0x03FF D2D Non Blocking Access (D2DI) 3 of 3 (continued)

Offset	Name		7	6	5	4	3	2	1	0
0x97	ADR8 (lo)	R	adr8 1	adr8 0	0	0	0	0	0	0
	ADC Data Result Register 8	W								
0x98	ADR9 (hi)	R	adr9 9	adr9 8	adr9 7	adr9 6	adr9 5	adr9 4	adr9 3	adr9 2
	ADC Data Result Register 9	W								
0x99	ADR9 (lo)	R	adr9 1	adr9 0	0	0	0	0	0	0
	ADC Data Result Register 9	W								
0x9A	ADR10 (hi)	R	adr10 9	adr10 8	adr10 7	adr10 6	adr10 5	adr10 4	adr10 3	adr10 2
	ADC Data Result Reg 10	W								
0x9B	ADR10 (lo)	R	adr10 1	adr10 0	0	0	0	0	0	0
	ADC Data Result Reg 10	W								
0x9C	ADR11 (hi)	R	adr11 9	adr11 8	adr11 7	adr11 6	adr11 5	adr11 4	adr11 3	adr11 2
	ADC Data Result Reg 11	W								
0x9D	ADR11 (lo)	R	adr11 1	adr11 0	0	0	0	0	0	0
	ADC Data Result Reg 11	W								
0x9E	ADR12 (hi)	R	adr12 9	adr12 8	adr12 7	adr12 6	adr12 5	adr12 4	adr12 3	adr12 2
	ADC Data Result Reg 12	W								
0x9F	ADR12 (lo)	R	adr12 1	adr12 0	0	0	0	0	0	0
	ADC Data Result Reg 12	W								
0xA2	ADR14 (hi)	R	adr14 9	adr14 8	adr14 7	adr14 6	adr14 5	adr14 4	adr14 3	adr14 2
	ADC Data Result Reg 14	W								
0xA3	ADR14 (lo)	R	adr14 1	adr14 0	0	0	0	0	0	0
	ADC Data Result Reg 14	W								
0xA4	ADR15 (hi)	R	adr15 9	adr15 8	adr15 7	adr15 6	adr15 5	adr15 4	adr15 3	adr15 2
	ADC Data Result Reg 15	W								
0xA5	ADR15 (lo)	R	adr15 1	adr15 0	0	0	0	0	0	0
	ADC Data Result Reg 15	W								
0xC0	TIOS	R	0	0	0	0	IOS3	IOS2	IOS1	IOS0
	TIM InCap/OutComp Select	W								
0xC1	CFORC	R	0	0	0	0	0	0	0	0
	Timer Compare Force Reg	W					FOC3	FOC2	FOC1	FOC0
0xC2	OC3M	R	0	0	0	0	OC3M3	OC3M2	OC3M1	OC3M0
	Output Comp 3 Mask Reg	W								
0xC3	OC3D	R	0	0	0	0	OC3D3	OC3D2	OC3D1	OC3D0
	Output Comp 3 Data Reg	W								
0xC4	TCNT (hi)	R	tcnt 15	tcnt 14	tcnt 13	tcnt 12	tcnt 11	tcnt 10	tcnt 9	tcnt 8
	Timer Count Register	W								
0xC5	TCNT (lo)	R	tcnt 7	tcnt 6	tcnt 5	tcnt 4	tcnt 3	tcnt 2	tcnt 1	tcnt 0
	Timer Count Register	W								
0xC6	TSCR1	R	TEN	0	0	TFFCA	0	0	0	0
	Timer System Control Reg 1	W								
0xC7	TTOV	R	0	0	0	0	TOV3	TOV2	TOV1	TOV0
	Timer Toggle Overflow Reg	W								

The Conversion Complete Register for the not available Lx analog input (3.8) must be ignored.

0x84	ACCSR (hi)	R	CC15	CC14	0	CC12	CC11	CC10	CC9	CC8
	ADC Conv Complete Reg	W								
0x85	ACCSR (lo)	R	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0
	ADC Conv Complete Reg	W								

The ADC Data Result Register for the not available Lx analog input (3.8) must be ignored.

0x8C-0 x97	ADRx (hi)	R	adrx 9	adrx 8	adrx 7	adrx 6	adrx 5	adrx 4	adrx 3	adrx 2
	ADC Data Result Register x	W								
	ADRx (lo)	R	adrx 1	adrx 0	0	0	0	0	0	0
	ADC Data Result Register x	W								

4.2.3.2.3 Functional Considerations

For the not available Lx inputs, the following functions are limited:

- No Wake-up feature / Cyclic Sense
- No Digital Input
- No Analog Input and conversion via ADC

4.5 Die to Die Interface - Target

The D2D Interface is the bus interface to the Microcontroller. Access to the MM912F634 analog die is controlled by the D2D Interface module. This section describes the functionality of the die-to-die target block (D2D).

4.5.1 Overview

The D2D is the target for a data transfer from the target to the initiator (MCU). The initiator provides a set of configuration registers and two memory mapped 256 Byte address windows. When writing to a window, a transaction is initiated sending a write command, followed by an 8-bit address, and the data byte or word is received from the initiator. When reading from a window, a transaction is received with the read command, followed by an 8-bit address. The target then responds with the data. The basic idea is that a peripheral located on the MM912F634 analog die, can be addressed like an on-chip peripheral.

Features:

- software transparent register access to peripherals on the MM912F634 analog die
- 256 Byte address window
- supports blocking read or write, as well as non-blocking write transactions
- 4 bit physical bus width
- automatic synchronization of the target when initiator starts driving the interface clock
- generates transaction and error status as well as EOT acknowledge
- providing single interrupt interface to D2D Initiator

4.5.2 Low Power Mode Operation

The D2D module is disabled in SLEEP mode. In Stop mode, the D2DINT signal is used to wake-up a powered down MCU. As the MCU could wake up without the MM912F634 analog die, a special command will be recognized as a wake-up event during Stop mode. See Section 4.3, “Modes of Operation".

4.5.2.1 Normal Mode / Stop Mode

NOTE

The maximum allowed clock speed of the interface is limited to f_{D2D}.

While in Normal or Stop mode, D2DCLK acts as input only with pull present. D2D[3:0] operates as an input/output with pull-down always present. D2DINT acts as output only.

4.5.2.2 Sleep Mode

While in Sleep mode, all Interface data pins are pulled down to DGND to reduce power consumption.

Figure 32 shows the receiver portion of the SCI.

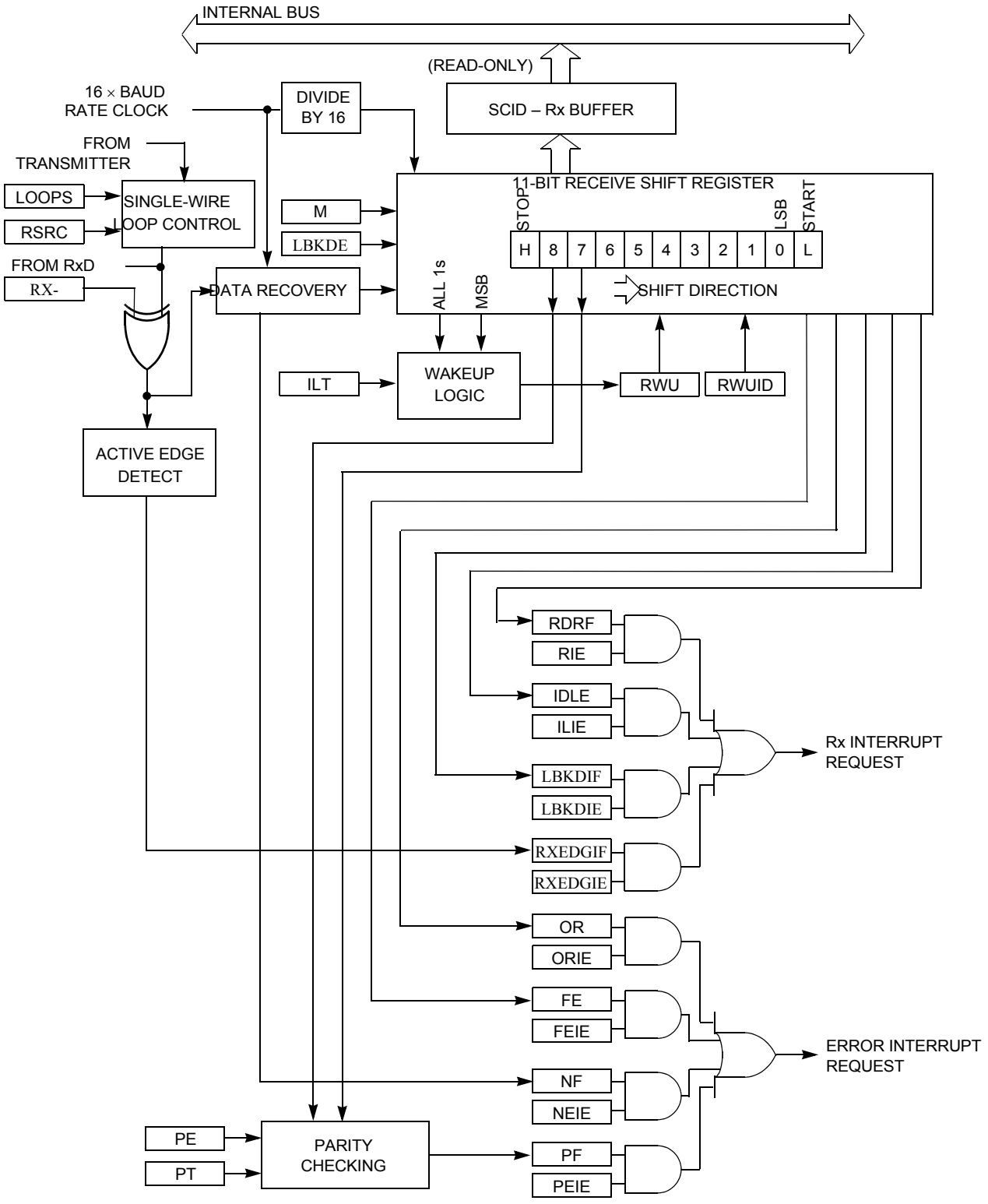


Figure 32. SCI Receiver Block Diagram

4.18.3.3.8 Timer Control Register 1 (TCTL1)

NOTE

These four pairs of control bits are encoded to specify the output action to be taken as a result of a successful Output Compare on “n” channel. When either OMn or OLn, the pin associated with the corresponding channel becomes an output tied to its IOC. To enable output action by the OMn and OLn bits on a timer port, the corresponding bit in OC3M should be cleared.

Table 166. Timer Control Register 1 (TCTL1)

Offset[122] 0xC8 Access: User read/write

	7	6	5	4	3	2	1	0
R W	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
Reset	0	0	0	0	0	0	0	0

Note:
122. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 167. TCTL1 - Register Field Descriptions

Field	Description
7,5,3,1 OMn	Output Mode bit
6,4,2,0 OLn	Output Level bit

Table 168. Compare Result Output Action

OMn	OLn	Action
0	0	Timer disconnected from output pin logic
0	1	Toggle OCn output line
1	0	Clear OCn output line to zero
1	1	Set OCn output line to one

4.18.3.3.9 Timer Control Register 2 (TCTL2)

Table 169. Timer Control Register 2 (TCTL2)

Offset 0xC9 Access: User read/write

	7	6	5	4	3	2	1	0
R W	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
Reset	0	0	0	0	0	0	0	0

Note:
123. [123]Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 170. TCTL2 - Register Field Descriptions

Field	Description
EDGnB,EDGnA	Input Capture Edge Control

These four pairs of control bits configure the input capture edge detector circuits.

Table 188. Analog Digital Converter Module - Memory Map (continued)

Register / Offset[132]		Bit 7	6	5	4	3	2	1	Bit 0
0x8D ADR3 (lo)	R	ADR3[1:0]							
	W								
0x8E ADR4 (hi)	R	ADR4[9:2]							
	W								
0x8F ADR4 (lo)	R	ADR4[1:0]							
	W								
0x90 ADR5 (hi)	R	ADR5[9:2]							
	W								
0x91 ADR5 (lo)	R	ADR5[1:0]							
	W								
0x92 ADR6 (hi)	R	ADR6[9:2]							
	W								
0x93 ADR6 (lo)	R	ADR6[1:0]							
	W								
0x94 ADR7 (hi)	R	ADR7[9:2]							
	W								
0x95 ADR7 (lo)	R	ADR7[1:0]							
	W								
0x96 ADR8 (hi)	R	ADR8[9:2]							
	W								
0x97 ADR8 (lo)	R	ADR8[1:0]							
	W								
0x98 ADR9 (hi)	R	ADR9[9:2]							
	W								
0x99 ADR9 (lo)	R	ADR9[1:0]							
	W								
0x9A ADR10 (hi)	R	ADR10[9:2]							
	W								
0x9B ADR10 (lo)	R	ADR10[1:0]							
	W								
0x9C ADR11 (hi)	R	ADR11[9:2]							
	W								
0x9D ADR11 (lo)	R	ADR11[1:0]							
	W								
0x9E ADR12 (hi)	R	ADR12[9:2]							
	W								
0x9F ADR12 (lo)	R	ADR12[1:0]							
	W								
0xA0 Reserved	R								
	W								
0xA1 Reserved	R								
	W								

The hardware handshake protocol is enabled by the ACK_ENABLE and disabled by the ACK_DISABLE BDM commands. This provides backwards compatibility with the existing POD devices which are not able to execute the hardware handshake protocol. It also allows for new POD devices, that support the hardware handshake protocol, to freely communicate with the target device. If desired, without the need for waiting for the ACK pulse.

The commands are described as follows:

- ACK_ENABLE — enables the hardware handshake protocol. The target will issue the ACK pulse when a CPU command is executed by the CPU. The ACK_ENABLE command itself also has the ACK pulse as a response.
- ACK_DISABLE — disables the ACK pulse protocol. In this case, the host needs to use the worst case delay time at the appropriate places in the protocol.

The default state of the BDM after reset is hardware handshake protocol disabled.

All the read commands will ACK (if enabled) when the data bus cycle has completed, and the data is then ready for reading out by the BKGD serial pin. All the write commands will ACK (if enabled) after the data has been received by the BDM through the BKGD serial pin, and when the data bus cycle is complete. See Section 4.30.4.3, “BDM Hardware Commands"” and Section 4.30.4.4, “Standard BDM Firmware Commands"” for more information on the BDM commands.

The ACK_ENABLE sends an ACK pulse when the command has been completed. This feature could be used by the host to evaluate if the target supports the hardware handshake protocol. If an ACK pulse is issued in response to this command, the host knows that the target supports the hardware handshake protocol. If the target does not support the hardware handshake protocol the ACK pulse is not issued. In this case, the ACK_ENABLE command is ignored by the target since it is not recognized as a valid command.

The BACKGROUND command will issue an ACK pulse when the CPU changes from normal to background mode. The ACK pulse related to this command could be aborted using the SYNC command.

The GO command will issue an ACK pulse when the CPU exits from background mode. The ACK pulse related to this command could be aborted using the SYNC command.

The GO_UNTIL[(169)] command is equivalent to a GO command with exception that the ACK pulse, in this case, is issued when the CPU enters into background mode. This command is an alternative to the GO command and should be used when the host wants to trace if a breakpoint match occurs, and causes the CPU to enter active background mode. Note that the ACK is issued whenever the CPU enters BDM, which could be caused by a breakpoint match or by a BGND instruction being executed. The ACK pulse related to this command could be aborted using the SYNC command.

The TRACE1 command has the related ACK pulse issued when the CPU enters background active mode after one instruction of the application program is executed. The ACK pulse related to this command could be aborted using the SYNC command.

4.30.4.9 SYNC — Request Timed Reference Pulse

The SYNC command is unlike other BDM commands, because the host does not necessarily know the correct communication speed to use for BDM communications until after it has analyzed the response to the SYNC command. To issue a SYNC command, the host should perform the following steps:

1. Drive the BKGD pin low for at least 128 cycles at the lowest possible BDM serial communication frequency (the lowest serial communication frequency is determined by either DCO clock or external crystal oscillator depending on the configuration chosen in the CRG.)
2. Drive BKGD high for a brief speedup pulse to get a fast rise time (this speedup pulse is typically one cycle of the host clock.)
3. Remove all drive to the BKGD pin so it reverts to high-impedance.
4. Listen to the BKGD pin for the sync response pulse.

Table 280. State1 Sequencer Next State Selection

SC[2:0]	Description
000	Any match to Final State
001	Match1 to State3
010	Match2 to State2
011	Match1 to State2
100	Match0 to State2..... Match1 to State3
101	Match1 to State3..... Match0 Final State
110	Match0 to State2..... Match2 to State3
111	Either Match0 or Match1 to State2..... Match2 has no effect

The priorities described in Table 311 dictate that in the case of simultaneous matches, the match on the lower channel number (0,1,2) has priority. The SC[2:0] encoding ensures that a match leading to final state has priority over all other matches.

4.31.3.2.7.2 Debug State Control Register 2 (DBGSCR2)

Table 281. Debug State Control Register 2 (DBGSCR2)

Address: 0x0027

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	SC2	SC1	SC0
W								
Reset	0	0	0	0	0	0	0	0

Read: If COMRV[1:0] = 01

Write: If COMRV[1:0] = 01 and DBG is not armed.

This register is visible at 0x0027 only with COMRV[1:0] = 01. The state control register 2 selects the targeted next state whilst in State2. The matches refer to the match channels of the comparator match control logic as depicted in Figure 69 and described in Section 4.31.3.2.8.1, “Debug Comparator Control Register (DBGXCTL)””. Comparators must be enabled by setting the comparator enable bit in the associated DBGXCTL control register.

Table 282. DBGSCR2 Field Descriptions

Field	Description
2–0 SC[2:0]	These bits select the targeted next state whilst in State2, based upon the match event.

Table 283. State2 —Sequencer Next State Selection

SC[2:0]	Description
000	Match0 to State1..... Match2 to State3.
001	Match1 to State3
010	Match2 to State3
011	Match1 to State3..... Match0 Final State
100	Match1 to State1..... Match2 to State3
101	Match2 Final State
110	Match2 to State1..... Match0 to Final State
111	Match2 has no affect, all other matches (M0,M1) to Final State

The priorities described in Table 311 dictate that in the case of simultaneous matches, the match on the lower channel number (0,1,2) has priority. The SC[2:0] encoding ensures that a match leading to final state has priority over all other matches

Table 292. DBGXCTL Field Descriptions (continued)

Field	Description
5 TAG	**Tag Select**— This bit controls whether the comparator match has immediate effect, causing an immediate state sequencer transition or tag the opcode at the matched address. Tagged opcodes trigger only if they reach the execution stage of the instruction queue. 0 Allow state sequencer transition immediately on match 1 On match, tag the opcode. If the opcode is about to be executed allow a state sequencer transition
4 BRK	**Break**— This bit controls whether a comparator match terminates a debug session immediately, independent of state sequencer state. To generate an immediate breakpoint the module breakpoints must be enabled using the DBGC1 bit DBGBRK. 0 The debug session termination is dependent upon the state sequencer and trigger conditions. 1 A match on this channel terminates the debug session immediately; breakpoints if active are generated, tracing, if active, is terminated and the module disarmed.
3 RW	**Read/Write Comparator Value Bit** — The RW bit controls whether read or write is used in compare for the associated comparator. The RW bit is not used if RWE = 0. This bit is ignored if the TAG bit in the same register is set. 0 Write cycle will be matched 1 Read cycle will be matched
2 RWE	**Read/Write Enable Bit** — The RWE bit controls whether read or write comparison is enabled for the associated comparator.This bit is ignored if the TAG bit in the same register is set 0 Read/Write is not used in comparison 1 Read/Write is used in comparison
0 COMPE	Determines if comparator is enabled 0 The comparator is not enabled 1 The comparator is enabled

Table 293 shows the effect for RWE and RW on the comparison conditions. These bits are ignored if the corresponding TAG bit is set since the match occurs based on the tagged opcode reaching the execution stage of the instruction queue.

Table 293. Read or Write Comparison Logic Table

RWE Bit	RW Bit	RW Signal	Comment
0	x	0	RW not used in comparison
0	x	1	RW not used in comparison
1	0	0	Write data bus
1	0	1	No match
1	1	0	No match
1	1	1	Read data bus

4.31.3.2.8.2 Debug Comparator Address High Register (DBGXAH)

Table 294. Debug Comparator Address High Register (DBGXAH)

Address: 0x0029

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	Bit 17	Bit 16
W								
Reset	0	0	0	0	0	0	0	0

The DBGC1_COMRV bits determine which comparator address registers are visible in the 8-byte window from 0x0028 to 0x002F.

Table 295. Comparator Address Register Visibility

COMRV	Visible Comparator
00	DBGAAH, DBGAAM, DBGAAL

Table 295. Comparator Address Register Visibility (continued)

COMRV	Visible Comparator
01	DBGBAH, DBGBAM, DBGBAL
10	DBGCAH, DBGCAM, DBGCAL
11	None

Read: Anytime. See Table 296 for visible register encoding.

Write: If DBG not armed. See Table 296 for visible register encoding.

Table 296. DBGXAH Field Descriptions

Field	Description
1–0 Bit[17:16]	**Comparator Address High Compare Bits** — The Comparator address high compare bits control whether the selected comparator will compare the address bus bits [17:16] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one

4.31.3.2.8.3 Debug Comparator Address Mid Register (DBGXAM)

Address: 0x002A

	7	6	5	4	3	2	1	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset	0	0	0	0	0	0	0	0

Table 297. Debug Comparator Address Mid Register (DBGXAM)

Read: Anytime. See Table 297 for visible register encoding.

Write: If DBG not armed. See Table 297 for visible register encoding.

Table 298. DBGXAM Field Descriptions

Field	Description
7–0 Bit[15:8]	**Comparator Address Mid Compare Bits** — The Comparator address mid compare bits control whether the selected comparator will compare the address bus bits [15:8] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one

4.31.4.2.3 Range Comparisons

Using the AB comparator pair for a range comparison, the data bus can also be used for qualification by using the comparator A data registers. Furthermore the DBGACTL RW and RWE bits can be used to qualify the range comparison on either a read or a write access. The corresponding DBGBCTL bits are ignored. The SZE and SZ control bits are ignored in range mode. The comparator A TAG bit is used to tag range comparisons. The comparator B TAG bit is ignored in range modes. In order for a range comparison using comparators A and B, both COMPEA and COMPEB must be set; to disable range comparisons both must be cleared. The comparator A BRK bit is used to for the AB range, the comparator B BRK bit is ignored in range mode.

When configured for range comparisons and tagging, the ranges are accurate only to word boundaries.

4.31.4.2.3.1 Inside Range (CompA_Addr $\leq$ address $\leq$ CompB_Addr)

In the Inside Range comparator mode, comparator pair A and B can be configured for range comparisons. This configuration depends upon the control register (DBGC2). The match condition requires that a valid match for both comparators happens on the same bus cycle. A match condition on only one comparator is not valid. An aligned word access which straddles the range boundary is valid only if the aligned address is inside the range.

4.31.4.2.3.2 Outside Range (address < CompA_Addr or address > CompB_Addr)

In the outside range comparator mode, comparator pair A and B can be configured for range comparisons. A single match condition on either of the comparators is recognized as valid. An aligned word access which straddles the range boundary is valid only if the aligned address is outside the range.

Outside range mode in combination with tagging can be used to detect if the opcode fetches are from an unexpected range. In forced match mode the outside range match would typically be activated at any interrupt vector fetch or register access. This can be avoided by setting the upper range limit to $3FFFF or lower range limit to $00000 respectively.

4.31.4.3 Match Modes (Forced or Tagged)

Match modes are used as qualifiers for a state sequencer change of state. The Comparator control register TAG bits select the match mode. The modes are described in the following sections.

4.31.4.3.1 Forced Match

When configured for forced matching, a comparator channel match can immediately initiate a transition to the next state sequencer state whereby the corresponding flags in DBGSR are set. The state control register for the current state determines the next state. Forced matches are typically generated 2-3 bus cycles after the final matching address bus cycle, independent of comparator RWE/RW settings. Furthermore since opcode fetches occur several cycles before the opcode execution a forced match of an opcode address typically precedes a tagged match at the same address.

4.31.4.3.2 Tagged Match

If a CPU taghit occurs a transition to another state, sequencer state is initiated, and the corresponding DBGSR flags are set. For a comparator related taghit to occur, the DBG must first attach tags to instructions as they are fetched from memory. When the tagged instruction reaches the execution stage of the instruction queue a taghit is generated by the CPU. This can initiate a state sequencer transition.

4.31.4.3.3 Immediate Trigger

Independent of comparator matches it is possible to initiate a tracing session and/or breakpoint, by writing to the TRIG bit in DBGC1. This forces the state sequencer into the Final State and issues a forced breakpoint request to the CPU.

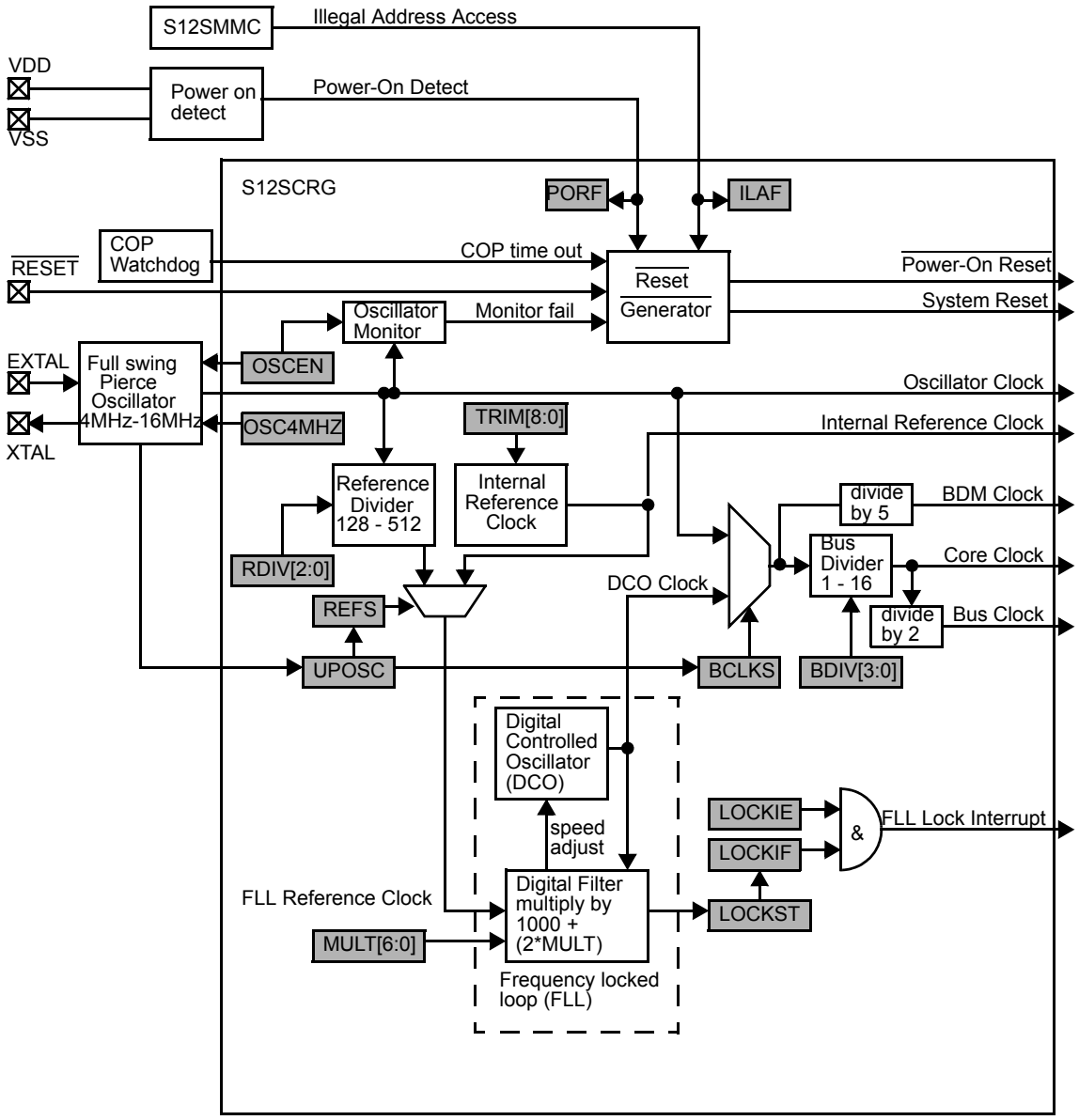


Figure 72. Block diagram of 9S12I32PIMV1

4.32.2 Signal Description

This section lists and describes the signals that connect off chip.

4.32.2.1 RESET

$\overline{\text{RESET}}$ is an active low bidirectional reset pin. As an input it initializes the MCU asynchronously to a known start-up state. As an open-drain output it indicates that a System Reset or Power-on Reset (internal to MCU) has been triggered.

4.32.3 Memory Map and Registers

This section provides a detailed description of all registers accessible in the 9S12I32PIMV1.

4.32.3.1 Module Memory Map

Table 319 gives an overview on all 9S12I32PIMV1 registers.

Table 319. 9S12I32PIMV1 Register Summary

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0034	CRGCTL0	R	OSCEN	RDIV[2:0]			BCLKS	REFS	OSC4MHZ	0
		W								
0x0035	CRGCTL1	R	BDIV[3:0]				0	0	LOCKIE	0
		W								
0x0036	CRGMULT	R	0	MULT[6:0]						
		W								
0x0037	CRGFLG	R	0	PORF	0	LOCKIF	LOCKST	ILAF	UPOSC	0
		W								
0x0038	CRGTRIMH	R	0	0	0	0	0	0	0	TRIM[8]
		W								
0x0039	CRGTRIML	R	TRIM[7:0]							
		W								
0x003A	CRGTEST0 (Reserved)	R	0	0	0	0	0	0	0	0
		W								
0x003B	CRGTEST1 (Reserved)	R	U	U	U	U	U	U	U	U
		W								

4.32.3.2 Register Descriptions

This section describes in address order all the 9S12I32PIMV1 registers and their individual bits.

Table 343. COPCTL Field Descriptions (continued)

Field	Description
3 COPRSTP	**COP Runs in Stop Mode Bit** Normal modes: Write once Special modes: Write anytime 0 COP stops in Stop mode 1 COP continues in Stop mode **Note:** If the COPRSTP bit is cleared the COP counter will go static while in Stop mode. The COP counter will not initialize like in Wait mode with COPSWAI bit set.
2–0 CR[2:0]	**COP Watchdog Timer Rate Select Bits** — These bits select the COP timeout rate (see Table 344). Writing a non-zero value to CR[2:0] enables the COP counter and starts the timeout period. A COP counter timeout causes a system reset. This can be avoided by periodically (before timeout) re-initialize the COP counter via the ARMCOP register. While all of the following four conditions are true the CR[2:0], WCOP bits are ignored and the COP operates at highest timeout period (2^{16} cycles) in normal COP mode (Window COP mode disabled): 1) COP is enabled (CR[2:0] is not 000) 2) BDM mode active 3) RSBCK = 0 4) Operation in special mode

Table 344. COP Watchdog Rates(187)

CR2	CR1	CR0	Input_CLK Cycles to Timeout
0	0	0	COP disabled
0	0	1	2^6
0	1	0	2^8
0	1	1	2^{10}
1	0	0	2^{12}
1	0	1	2^{14}
1	1	0	2^{15}
1	1	1	2^{16}

Note:
187. Refer to Device User Guide (Section 4.35.4.1, “COP Configuration") for reset values of WCOP, CR2, CR1 and CR0.

4.36 32 kbyte Flash Module (S12SFTSR32KV1)

4.36.1 Introduction

This document describes the S12SFTSR32K module, that includes a 32 kbyte Flash (nonvolatile) memory.

CAUTION

A Flash block address must be in the erased state before being programmed. Cumulative programming of bits within a Flash block address is not allowed, except for status field updates required in EEPROM emulation applications.

The Flash memory is ideal for single-supply applications, allowing for field reprogramming without requiring external high voltage sources for program or erase operations. The Flash module includes a memory controller that executes commands to modify Flash memory contents.

Array read access time is one bus cycle for bytes and aligned words, and two bus cycles for misaligned words. For Flash memory, an erased bit reads 1 and a programmed bit reads 0. It is not possible to read from a Flash block while any command is executing on that specific Flash block.

4.36.1.1 Glossary

Command Write Sequence — A three step MCU instruction sequence to execute built-in algorithms (including program and erase) on the Flash memory.

Flash Array — The Flash array constitutes the main memory portion of a Flash block.

Flash Block — An analog block consisting of the Flash array and Flash IFR with supporting high voltage and parametric test circuitry.

Flash IFR — Nonvolatile information memory, consisting of 128 bytes, located in the Flash block outside of Flash main memory. Refer to the SoC Guide on how to make the Flash IFR visible in the global memory map.

4.36.1.2 Features

- 32 kbytes of Flash memory comprised of one 32 kbyte block divided into 64 sectors of 512 bytes
- Nonvolatile information memory (Flash IFR) comprised of one 128 byte block
- Automated program and erase algorithm
- Interrupt on Flash command completion, command buffer empty
- Fast program and sector erase operation
- Burst program command for faster Flash array program times
- Flexible protection scheme to prevent accidental program or erase
- Single power supply for all Flash operations including program and erase
- Security feature to prevent unauthorized access to the Flash memory

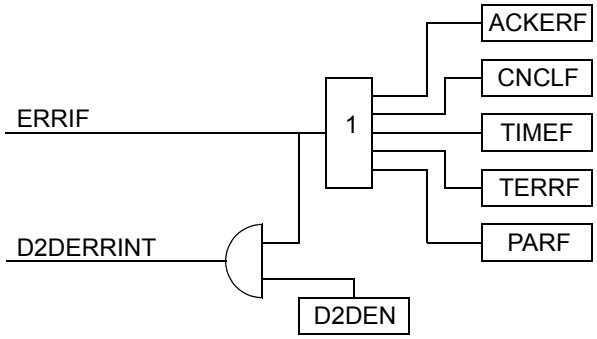


Figure 98. D2D Internal Interrupts

4.37.5 Initialization Information

During initialization the transfer width, clock divider and timeout value must be set according to the capabilities of the target device before starting any transaction. See the D2D Target specification for details.

4.37.6 Application Information

4.37.6.1 Entering low power mode

The D2DI module is typically used on a microcontroller along with an analog companion device containing the D2D target interface and supplying the power. Interface specification does not provide special wires for signalling low power modes to the target device. The CPU should determine when it is time to enter one of the above power modes.The basic flow is as follows:

1. CPU determines there is no more work pending.
2. CPU writes a byte to a register on the analog die using blocking write configuring which mode to enter.
3. Analog die acknowledges that write sending back an acknowledge symbol on the interface.
4. CPU executes WAIT or STOP command.
5. Analog die can enter low-power mode - (S12 needs some more cycles to stack data)

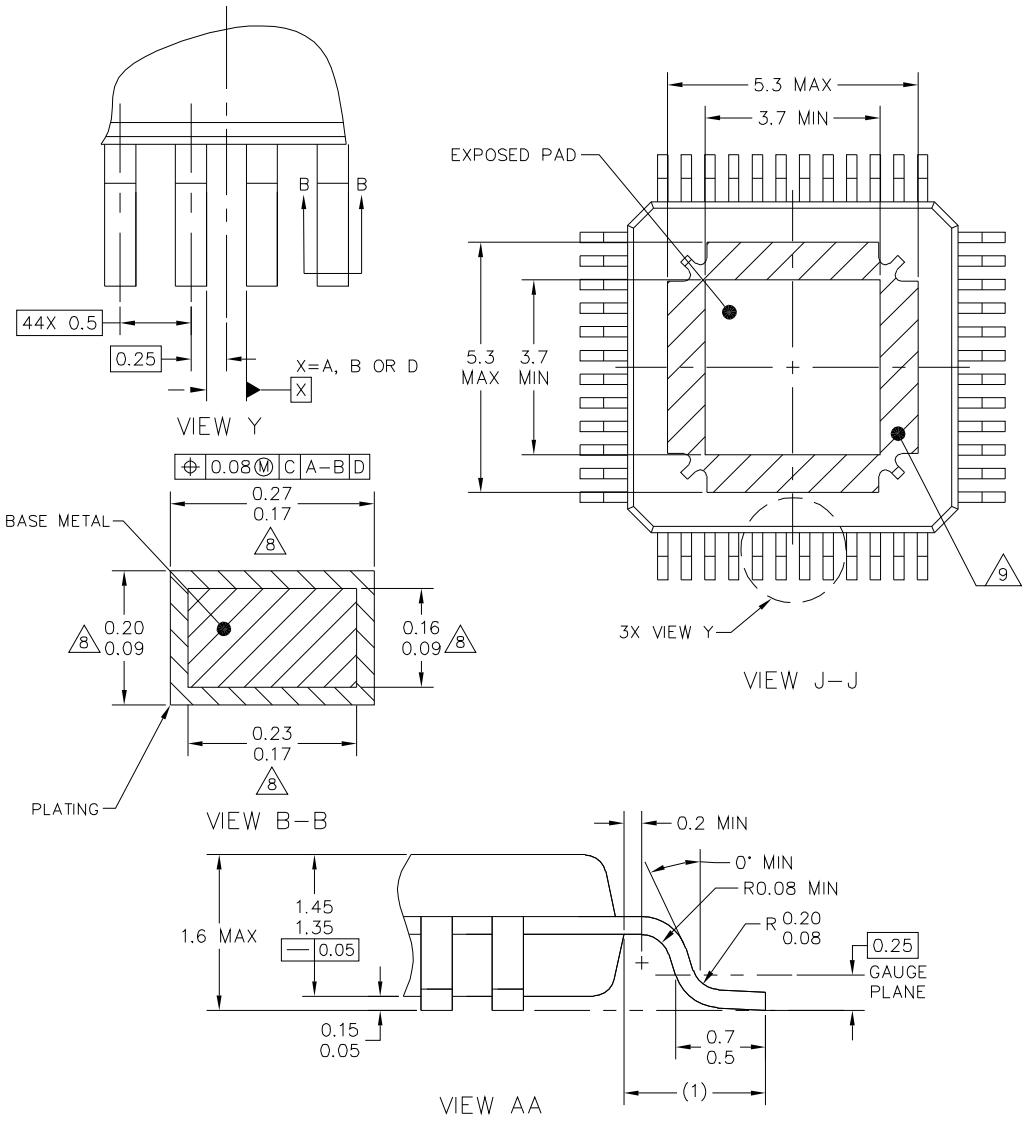
```
; Example shows S12 code
SEI         ; disable interrupts during test
; check is there is work pending?
; if yes, branch off and re-enable interrupt
; else
LDAA        #STOP_ENTRY
STAA        MODE_REG            ; store to the analog die mode reg (use blocking write here)
CLI         ; re-enable right before the STOP instruction
STOP        ; stack and turn off all clocks inc. interface clock
```

For wake-up from STOP the basic flow is as follows:

1. Analog die detects a wake-up condition e.g. on a switch input or start bit of a LIN message.
2. Analog die exits Voltage Regulator low-power mode.
3. Analog die asserts the interrupt signal D2DINT.
4. CPU starts clock generation.
5. CPU enters interrupt handler routine.
6. CPU services interrupt and acknowledges the source on the analog die.

NOTE

Entering STOP mode or WAIT mode with D2DSWAI asserted, the clock will complete the high duty cycle portion and settle at low level.



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