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Details	
Product Status	Active
Applications	Automotive
Core Processor	S12
Program Memory Type	FLASH (32KB)
Controller Series	HCS12
RAM Size	2K x 8
Interface	LIN, SCI
Number of I/O	9
Voltage - Supply	2.25V ~ 5.5V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	48-LQFP Exposed Pad
Supplier Device Package	48-HLQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm912f634dv2aer2

2.2 MCU Die Signal Properties

This section describes the external MCU signals. It includes a table of signal properties.

Table 4. Signal Properties Summary

Pin Name Function 1	Pin Name Function 2	Power Supply	Internal Pull Resistor		Description
			CTRL	Reset State	
EXTAL	—	V_{DD}	NA	NA	Oscillator pins
XTAL	—	V_{DD}	NA	NA	
$\overline{\text{RESET}}$	—	V_{DDX}	Pull-up		External reset
TEST	—	N.A.	$\overline{\text{RESET}}$ pin	Down	Test input
BKGD	MODC	V_{DDX}	Always on	UP	Background debug
PA5	—	V_{DDX}	NA	NA	Port A I/O
PA4	—	V_{DDX}	NA	NA	Port A I/O
PA3	SS	V_{DDX}	NA	NA	Port A I/O, SPI
PA2	SCK	V_{DDX}	NA	NA	Port A I/O, SPI
PA1	MOSI	V_{DDX}	NA	NA	Port A I/O, SPI
PA0	MISO	V_{DDX}	NA	NA	Port A I/O, SPI

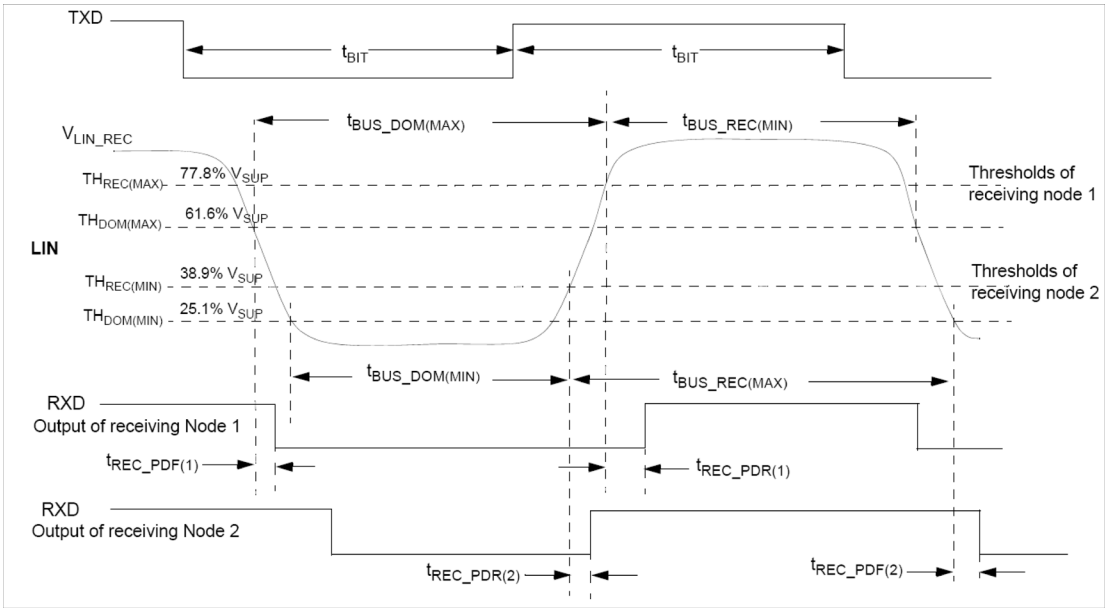

Figure 7. LIN Timing Measurements for Slow Baud Rate

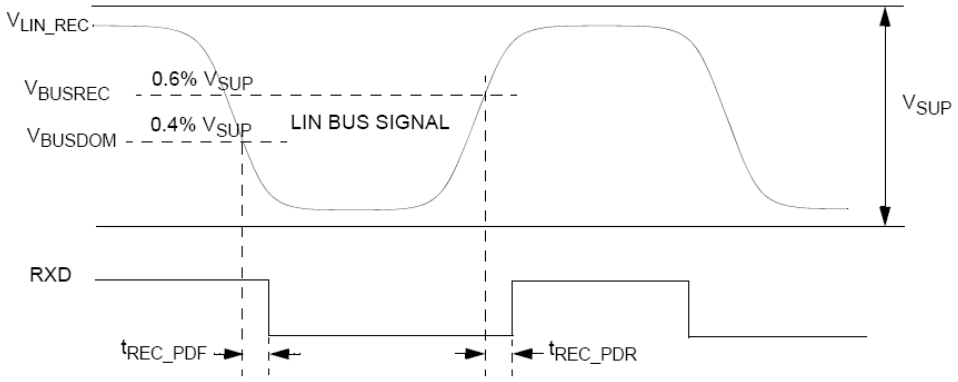

Figure 8. LIN Receiver Timing

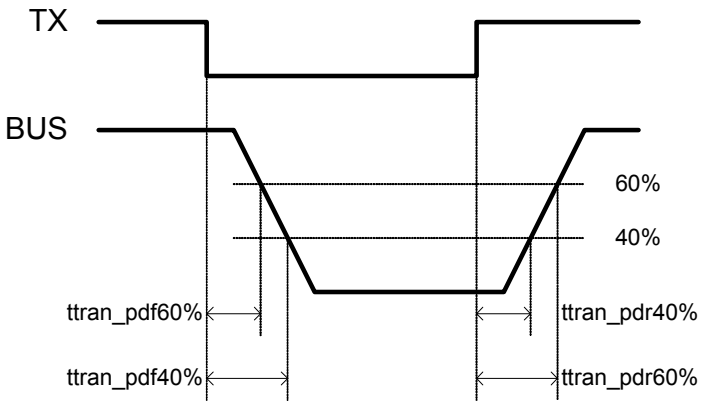

Figure 9. LIN Transmitter Timing

4.11.7 Register Definition

4.11.7.1 High Side Control Register (HSCR)

Table 97. High Side Control Register (HSCR)

Offset[79] 0x28 Access: User read/write

	7	6	5	4	3	2	1	0
R W	HSOTIE	HSHVSDE	PWMCS2	PWMCS1	PWMHS2	PWMHS1	HS2	HS1
Reset	0	0	0	0	0	0	0	0

Note:
79. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 98. HSCR - Register Field Descriptions

Field	Description
7 - HSOTIE	High Side Over-temperature Interrupt Enable
6 - HSHVSDE	High Side High Voltage Shutdown. Once enabled, both high sides will shut down when a high voltage condition - HVC is present. See Section 4.4, “Power Supply" for the Voltage Status Register.
5 - PWMCS2	PWM Channel Select HS2 0 - PWM Channel 0 selected as PWM Channel 1 - PWM Channel 1 selected as PWM Channel
4 - PWMCS1	PWM Channel Select HS1 0 - PWM Channel 0 selected as PWM Channel 1 - PWM Channel 1 selected as PWM Channel
3 - PWMHS2	PWM Enable for HS2 0 - PWM disabled on HS2 1 - PWM enabled on HS2 (Channel as selected with PWMCS2)
2 - PWMHS1	PWM Enable for HS1 0 - PWM disabled on HS1 1 - PWM enabled on HS1 (Channel as selected with PWMCS1)
1 - HS2	HS2 Control 0 - HS2 disabled 1 - HS2 enabled
0 - HS1	HS2 Control 0 - HS1 disabled 1 - HS1 enabled

Table 104. LSCR - Register Field Descriptions (continued)

Field	Description
3 - PWMLS2	PWM Enable for LS2 0 - PWM disabled on LS2 1 - PWM enabled on LS2 (Channel as selected with PWMCS2)
2 - PWMLS1	PWM Enable for LS1 0 - PWM disabled on LS1 1 - PWM enabled on LS1 (Channel as selected with PWMCS1)
1 - LS2	LS2 Enable; LSEN has to be written once to control the LS2 Driver
0 - LS1	LS1 Enable; LSEN has to be written once to control the LS1 Driver

4.12.3.2.2 Low Side Status Register (LSSR)

Table 105. Low Side Status Register (LSSR)

Offset[83] 0x31 Access: User read

	7	6	5	4	3	2	1	0
R	LSOTC	0	0	0	LS2CL	LS1CL	LS2OL	LS1OL
W								
Reset	0	0	0	0	0	0	0	0

Note:

83. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 106. LSSR - Register Field Descriptions

Field	Description
7 - LSOTC	Low Side Over-temperature condition present. Both drivers are turned off. Reading the register will clear the LSOT interrupt flag if present. See Section 4.6, “Interrupts" for details.
3 - LS2CL	Low Side 2 Current Limitation
2 - LS1CL	Low Side 1 Current Limitation
1 - LS2OL	Low Side 2 Open Load [84]
0 - LS1OL	Low Side 1Open Load [84]

Note:

84. When the Low Side is in OFF state, the Open Load Detection function is not operating. When reading the LSSR register while the Low Side is operating in PWM and is in the OFF state, the LS1OL and LS2OL bits will not indicate Open Load.

4.12.3.2.3 Low Side Control Enable Register (LSCEN)

Table 107. Low Side Enable Register (LSEN)

Offset[85] 0x32 Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	LSCEN			
W								
Reset	0	0	0	0	0	0	0	0

Note:

85. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 108. LSEN - Register Field Descriptions

Field	Description
3-0 LSCEN	Low Side Control Enable - To allow the LS Control via LSx, the correct value has to be written into the LSCEN Register. 0x5 - Low Side Control Enabled all other values - Low Side Control Disabled

Table 111. PWMCTL - Register Field Descriptions

Field	Description
7–6 CAE[1:0]	Center Aligned Output Modes on Channels 1–0 0 Channels 1–0 operate in left aligned output mode. 1 Channels 1–0 operate in center aligned output mode.
5 PCLK1	Pulse Width Channel 1 Clock Select 0 Clock B is the clock source for PWM channel 1. 1 Clock SB is the clock source for PWM channel 1.
4 PCLK0	Pulse Width Channel 0 Clock Select 0 Clock A is the clock source for PWM channel 0. 1 Clock SA is the clock source for PWM channel 0.
3–2 PPOL[1:0]	Pulse Width Channel 1–0 Polarity Bits 0 PWM channel 1–0 outputs are low at the beginning of the period, then go high when the duty count is reached. 1 PWM channel 1–0 outputs are high at the beginning of the period, then go low when the duty count is reached.
1-0 PWME[1:0]	Pulse Width Channel 1–0 Enable 0 Pulse width channel 1–0 is disabled. 1 Pulse width channel 1–0 is enabled. The pulse modulated signal becomes available at PWM, output bit 1 when its clock source begins its next cycle.

4.13.3.1.1 PWM Enable (PWMEx)

NOTE

The first PWM cycle after enabling the channel can be irregular. If both PWM channels are disabled (PWME1–0 = 0), the prescaler counter shuts off for power savings.

Each PWM channel has an enable bit (PWMEx) to start its waveform output. When any of the PWMEx bits are set (PWMEx = 1), the associated PWM output is enabled immediately. However, the actual PWM waveform is not available on the associated PWM output until its clock source begins its next cycle, due to the synchronization of PWMEx and the clock source.

4.13.3.1.2 PWM Polarity (PPOLx)

NOTE

PPOLx register bits can be written anytime. If the polarity changes while a PWM signal is being generated, a truncated or stretched pulse can occur during the transition

The starting polarity of each PWM channel waveform is determined by the associated PPOLx bit. If the polarity bit is one, the PWM channel output is high at the beginning of the cycle and then goes low when the duty count is reached. Conversely, if the polarity bit is zero, the output starts low and then goes high when the duty count is reached.

4.13.3.1.3 PWM Clock Select (PCLKx)

NOTE

Register bits PCLK0 and PCLK1 can be written anytime. If a clock select changes while a PWM signal is being generated, a truncated or stretched pulse can occur during the transition.

Each PWM channel has a choice of two clocks to use as the clock source for that channel as described by the following.

The output waveform generated is shown in Figure 28.

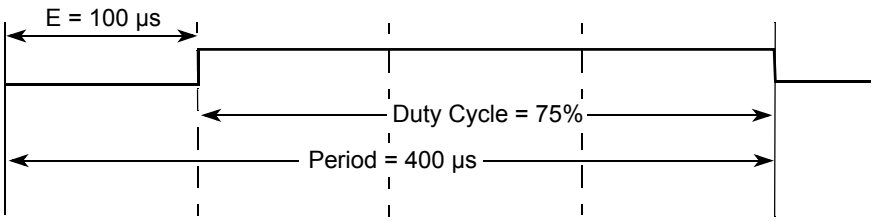

Figure 28. PWM Left Aligned Output Example Waveform

4.13.4.2.6 Center Aligned Outputs

NOTE

Changing the PWM output mode from left aligned to center aligned output (or vice versa) while channels are operating can cause irregularities in the PWM output. It is recommended to program the output mode before enabling the PWM channel.

For a center aligned output mode selection, set the CAEx bit (CAEx = 1) in the PWMCTL register, and the corresponding PWM output will be center aligned.

The 8-bit counter operates as an up/down counter in this mode, and is set to up whenever the counter is equal to $00. The counter compares to two registers, a duty register and a period register, as shown in the block diagram in Figure 26. When the PWM counter matches the duty register, the output flip-flop changes state, causing the PWM waveform to also change state. A match between the PWM counter and the period register changes the counter direction from an up-count to a down-count. When the PWM counter decrements and matches the duty register again, the output flip-flop changes state, causing the PWM output to also change state. When the PWM counter decrements and reaches zero, the counter direction changes from a down-count back to an up-count, and a load from the double buffer period and duty registers to the associated registers is performed, as described in Section 4.13.4.2.3, “PWM Period and Duty"”. The counter counts from 0 up to the value in the period register and then back down to 0. Thus the effective period is PWMPERx*2.

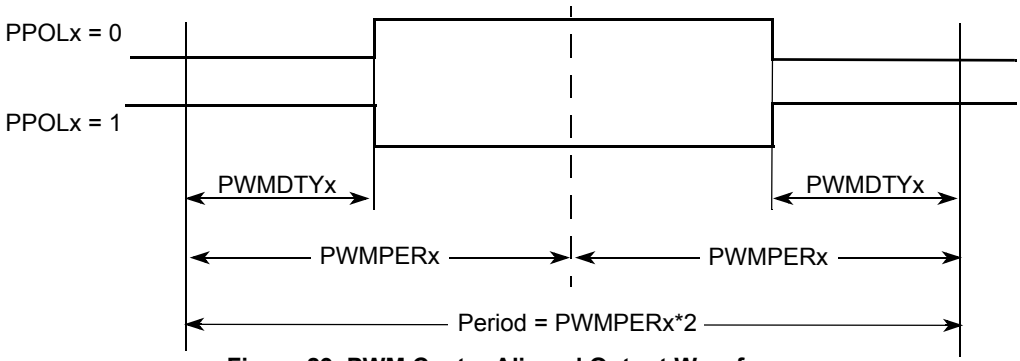

Figure 29. PWM Center Aligned Output Waveform

To calculate the output frequency in center aligned output mode for a particular channel, take the selected clock source frequency for the channel (A, B, SA, or SB) and divide it by twice the value in the period register for that channel.

- PWMx Frequency = Clock (A, B, SA, or SB) / (2*PWMPERx)
- PWMx Duty Cycle (high time as a% of period):
  — Polarity = 0 (PPOLx = 0)
  Duty Cycle = [(PWMPERx-PWMDTYx)/PWMPERx] * 100%
  — Polarity = 1 (PPOLx = 1)
  Duty Cycle = [PWMDTYx / PWMPERx] * 100%

4.18 Basic Timer Module - TIM (TIM16B4C)

4.18.1 Introduction

4.18.1.1 Overview

The basic timer consists of a 16-bit, software-programmable counter driven by a seven-stage programmable prescaler.

This timer can be used for many purposes, including input waveform measurements while simultaneously generating an output waveform. Pulse widths can vary from microseconds to many seconds.

This timer contains 4 complete input capture/output compare channels [IOC 3:2]. The input capture function is used to detect a selected transition edge and record the time. The output compare function is used for generating output signals or for timer software delays.

A full access for the counter registers or the input capture/output compare registers should take place in 16bit word access. Accessing high byte and low byte separately for all of these registers may not yield the same result as accessing them in one word.

4.18.1.2 Features

The TIM16B4C includes these distinctive features:

- Four input capture/output compare channels.
- Clock prescaler
- 16-bit counter

4.18.1.3 Modes of Operation

The TIM16B4C is only active during Normal mode.

4.18.1.4 Block Diagram

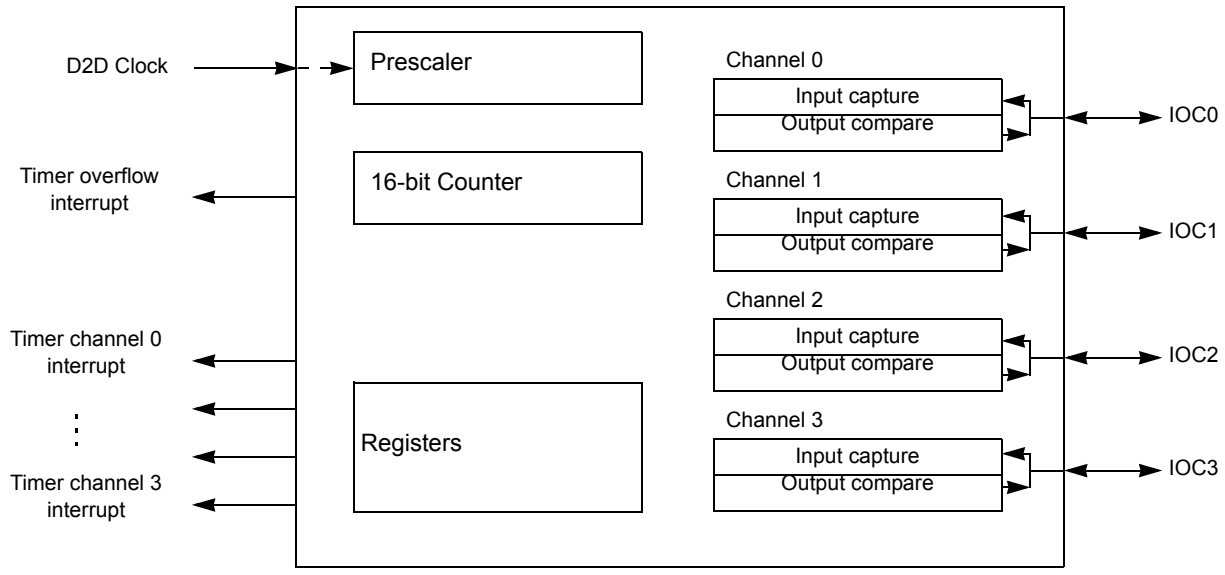

Figure 35. Timer Block Diagram

For more information see the respective functional descriptions see Section 4.18.4, “Functional Description" of this chapter.

4.18.3.3.8 Timer Control Register 1 (TCTL1)

NOTE

These four pairs of control bits are encoded to specify the output action to be taken as a result of a successful Output Compare on “n” channel. When either OMn or OLn, the pin associated with the corresponding channel becomes an output tied to its IOC. To enable output action by the OMn and OLn bits on a timer port, the corresponding bit in OC3M should be cleared.

Table 166. Timer Control Register 1 (TCTL1)

Offset[122] 0xC8 Access: User read/write

	7	6	5	4	3	2	1	0
R W	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
Reset	0	0	0	0	0	0	0	0

Note:
122. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 167. TCTL1 - Register Field Descriptions

Field	Description
7,5,3,1 OMn	Output Mode bit
6,4,2,0 OLn	Output Level bit

Table 168. Compare Result Output Action

OMn	OLn	Action
0	0	Timer disconnected from output pin logic
0	1	Toggle OCn output line
1	0	Clear OCn output line to zero
1	1	Set OCn output line to one

4.18.3.3.9 Timer Control Register 2 (TCTL2)

Table 169. Timer Control Register 2 (TCTL2)

Offset 0xC9 Access: User read/write

	7	6	5	4	3	2	1	0
R W	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
Reset	0	0	0	0	0	0	0	0

Note:
123. [123]Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 170. TCTL2 - Register Field Descriptions

Field	Description
EDGnB,EDGnA	Input Capture Edge Control

These four pairs of control bits configure the input capture edge detector circuits.

4.18.6.2 Description of Interrupt Operation

The TIM16B4C uses a total of 5 interrupt vectors. The interrupt vector offsets and interrupt numbers are chip dependent. More information on interrupt vector offsets and interrupt numbers can be found in the Section 4.6, “Interrupts"

4.18.6.2.1 Channel [3:0] Interrupt

These active high outputs are asserted by the module to request a timer channel 3–0 interrupt, following an input capture or output compare event on these channels [3-0]. For the interrupt to be asserted on a specific channel, the enable, CnI bit of TIE register should be set. These interrupts are serviced by the system controller.

4.18.6.2.2 Timer Overflow Interrupt (TOF)

This active high output will be asserted by the module to request a timer overflow interrupt, following the timer counter overflow when the overflow enable bit (TOI) bit of TFLG2 register is set. This interrupt is serviced by the system controller.

4.19.3 External Signal Description

This section lists and describes the signals that do connect off-chip. Table 187 shows all the pins and their functions that are controlled by the Analog Digital Converter Module.

Table 187. ADC - Pin Functions and Priorities

Pin Name	Pin Function & Priority	I/O	Description	Pin Function after Reset
AGND	Analog Ground	-	Analog Ground Connection	-
ADC2p5	Analog Regulator	-	Analog Digital Converter Regulator Filter Terminal. A capacitor C_{ADC2p5} is required for operation.	-

4.19.4 Memory Map and Register Definition

4.19.4.1 Module Memory Map

Table 188 shows the register map of the Analog Digital Converter Module. All Register addresses given are referenced to the D2D interface offset.

Table 188. Analog Digital Converter Module - Memory Map

Register / Offset[132]		Bit 7	6	5	4	3	2	1	Bit 0
0x80 ACR	R	SCIE	CCE	OCE	ADCRST	0	PS2	PS1	PS0
	W								
0x81 ASR	R	SCF	2p5CLF	0	0	CCNT3	CCNT2	CCNT1	CCNT0
	W								
0x82 ACCR (hi)	R	CH15	CH14	0	CH12	CH11	CH10	CH9	CH8
	W								
0x83 ACCR (lo)	R	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
	W								
0x84 ACCSR (hi)	R	CC15	CC14	0	CC12	CC11	CC10	CC9	CC8
	W								
0x85 ACCSR (lo)	R	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0
	W								
0x86 ADR0 (hi)	R	ADR0[9:2]							
	W								
0x87 ADR0 (lo)	R	ADR0[1:0]							
	W								
0x88 ADR1 (hi)	R	ADR1[9:2]							
	W								
0x89 ADR1 (lo)	R	ADR1[1:0]							
	W								
0x8A ADR2 (hi)	R	ADR2[9:2]							
	W								
0x8B ADR2 (lo)	R	ADR2[1:0]							
	W								
0x8C ADR3 (hi)	R	ADR3[9:2]							
	W								

Table 207. CTR1 - Register Field Descriptions

Field	Description
7 BGTRE	Bandgap trim enable 0 - no trim can be done 1 - trim can be done by setting BGTRIMUP and BGTRIMDN bits
6 CTR1_6	Spare Trim Bit
5 BGTRIMUP	Bandgap trim up bit 0 - default slope 1 - increase bandgap slope
4 BGTRIMDN	Bandgap trim down bit 0 - default slope 1 - decrease bandgap slope
3 IREFTRE	Iref trim enable bit 0 - no trim can be done 1 - trim can be done by setting IREFTR[2:0] bits
2-0 IREFTR2…0	Iref trim - This trim is used to adjust the internal zero TC current reference 000: 0% 001: +7.6% 010: +16.43% 011: +26.83% 100: -8.54% 101: -15.75% 110: -21.79% 111: 0%

4.25.1.2.3 Trimming Register 2 (CTR2)

Table 208. Trimming Register 2 (CTR2)

Offset[146] 0xF2 Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	SLPBGTRE	SLPBG_LOCK	SLPBGTR2	SLPBGTR1	SLPBGTR0
W								
Reset	0	0	0	0	0	0	0	0

Note:
146. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 209. CTR2 - Register Field Descriptions

Field	Description
4 SLPBGTRE	Sleep Bandgap trim enable 0 no trim can be done 1 trim lock can be done by setting SLPBGTR[2:0] bits and SLPBG_LOCK bit
3 SLPBG_LOCK	bg1p25sleep trim lock bit

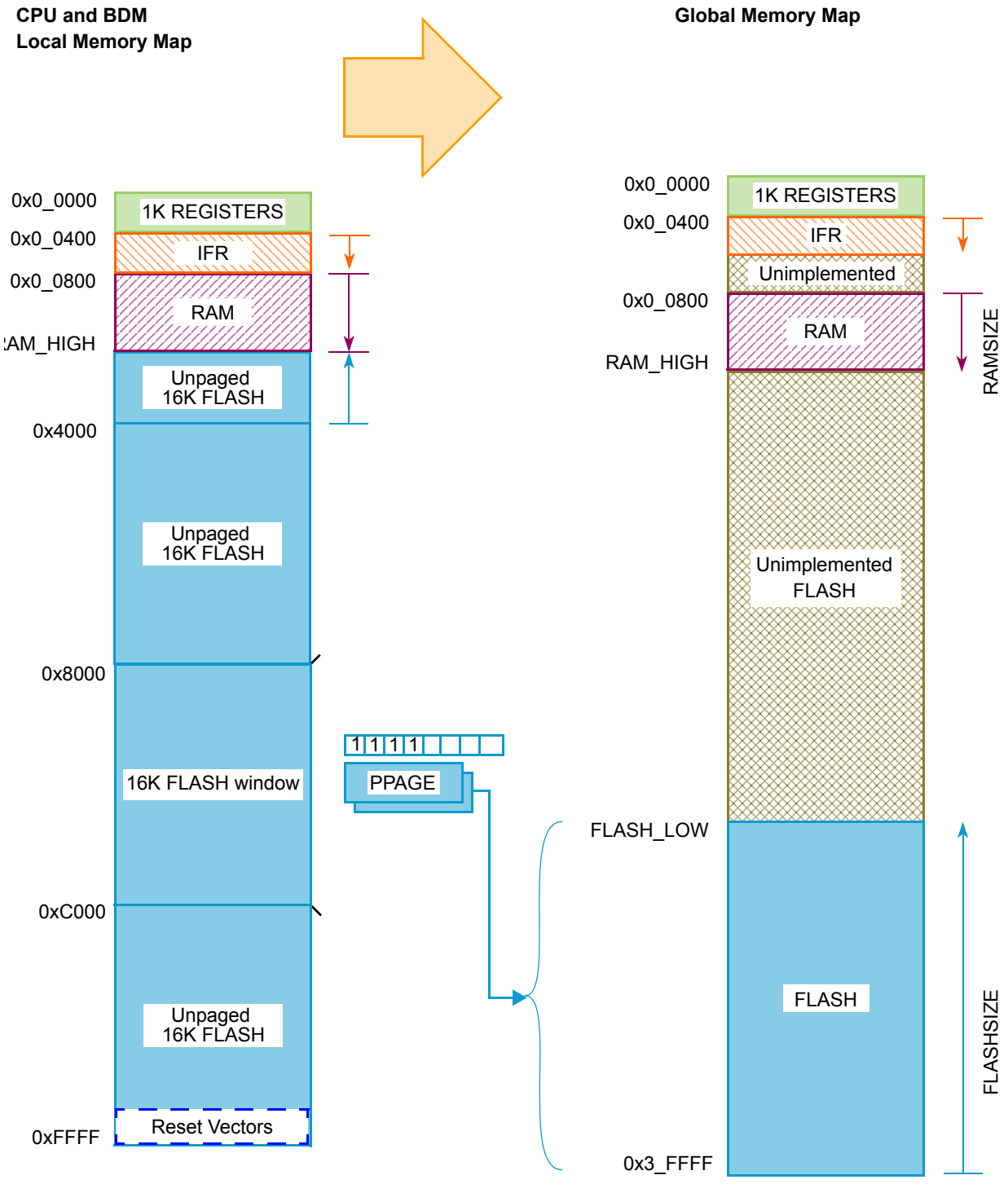

Figure 55. Implemented Global Address Mapping

"BDM Serial Interface"" and Section 4.30.3.2.1, "BDM Status Register (BDMSTS)"" for information on how serial clock rate is selected.

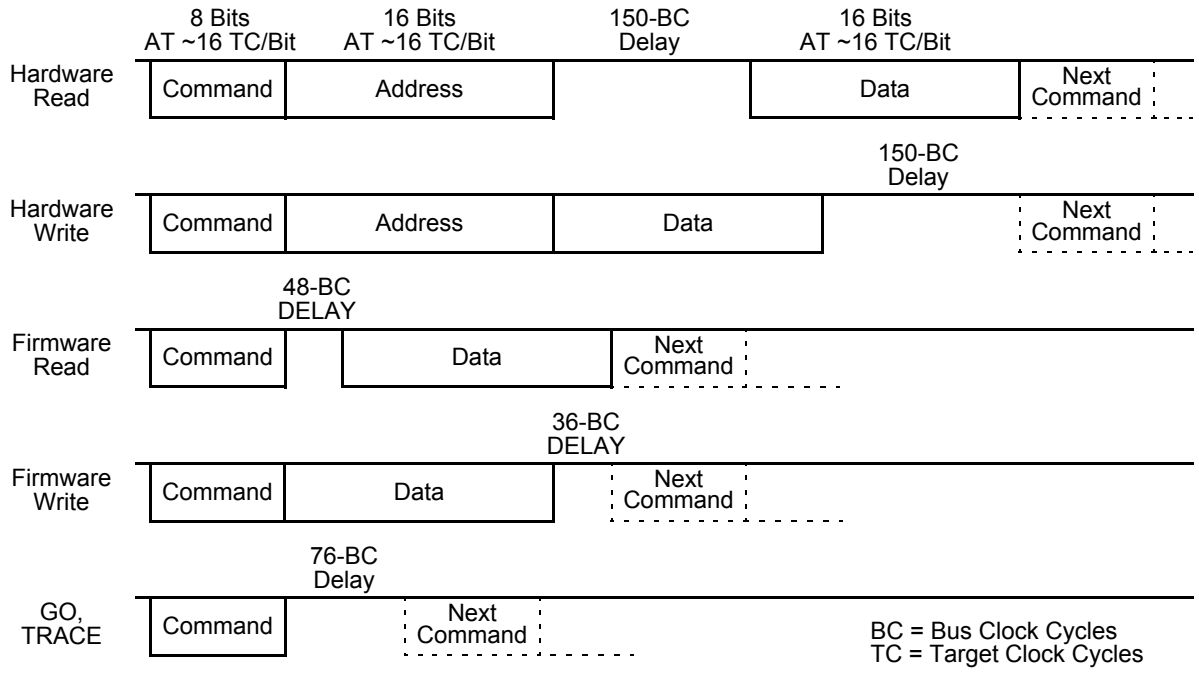

Figure 61. BDM Command Structure

4.30.4.6 BDM Serial Interface

The BDM communicates with external devices serially via the BKGD pin. During reset, this pin is a mode select input which selects between normal and special modes of operation. After reset, this pin becomes the dedicated serial interface pin for the BDM.

The BDM serial interface is timed based on DCO clock or external reference clock depending on the configuration used (refer to the CRG Block Guide for more details), which gets divided by five. This clock will be referred to as the target clock in the following explanation.

The BDM serial interface uses a clocking scheme in which the external host generates a falling edge on the BKGD pin to indicate the start of each bit time. This falling edge is sent for every bit whether data is transmitted or received. Data transfers the most significant bit (MSB) first at 16 target clock cycles per bit. The interface times out if 512 clock cycles occur between the falling edges from the host. The BKGD pin is a pseudo open-drain pin and has an weak on-chip active pull-up that is enabled at all times. It is assumed that there is an external pull-up and that drivers connected to BKGD do not typically drive the high level. Since R-C rise time could be unacceptably long, the target system and host provide brief driven high (speedup) pulses to drive BKGD to a logic 1. The source of this speedup pulse is the host for transmit cases and the target for receive cases.

The timing for host-to-target is shown in Figure 62 and that of target-to-host in Figure 63 and Figure 64. All four cases begin when the host drives the BKGD pin low to generate a falling edge. Since the host and target are operating from separate clocks, it can take the target system up to one full clock cycle to recognize this edge. The target measures delays from this perceived start of the bit time while the host measures delays from the point it actually drove BKGD low to start the bit up to one target clock cycle earlier. Synchronization between the host and target is established in this manner at the start of every bit time.

Figure 62 shows an external host transmitting a logic 1 and transmitting a logic 0 to the BKGD pin of a target system. The host is asynchronous to the target, so there is up to a one clock-cycle delay from the host-generated falling edge to where the target recognizes this edge as the beginning of the bit time. Ten target clock cycles later, the target senses the bit level on the BKGD

pin. Internal glitch detect logic requires the pin be driven high no later that eight target clock cycles after the falling edge for a logic 1 transmission.

Since the host drives the high speedup pulses in these two cases, the rising edges look like digitally driven signals.

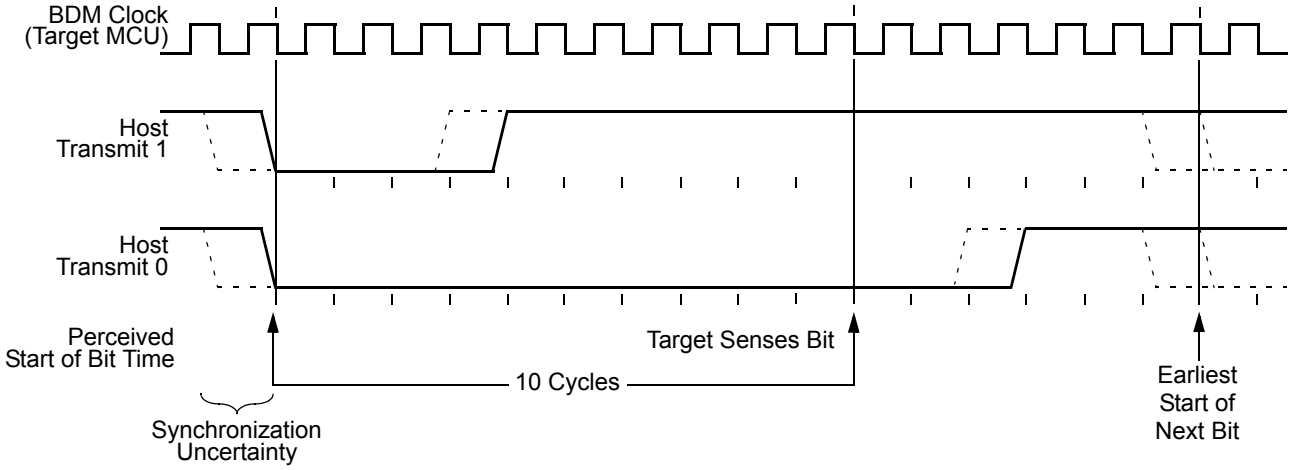

Figure 62. BDM Host-to-Target Serial Bit Timing

The receive cases are more complicated. Figure 63 shows the host receiving a logic 1 from the target system. Since the host is asynchronous to the target, there is up to one clock-cycle delay from the host-generated falling edge on BKGD to the perceived start of the bit time in the target. The host holds the BKGD pin low long enough for the target to recognize it (at least two target clock cycles). The host must release the low drive before the target drives a brief high speedup pulse seven target clock cycles after the perceived start of the bit time. The host should sample the bit level about 10 target clock cycles after it started the bit time.

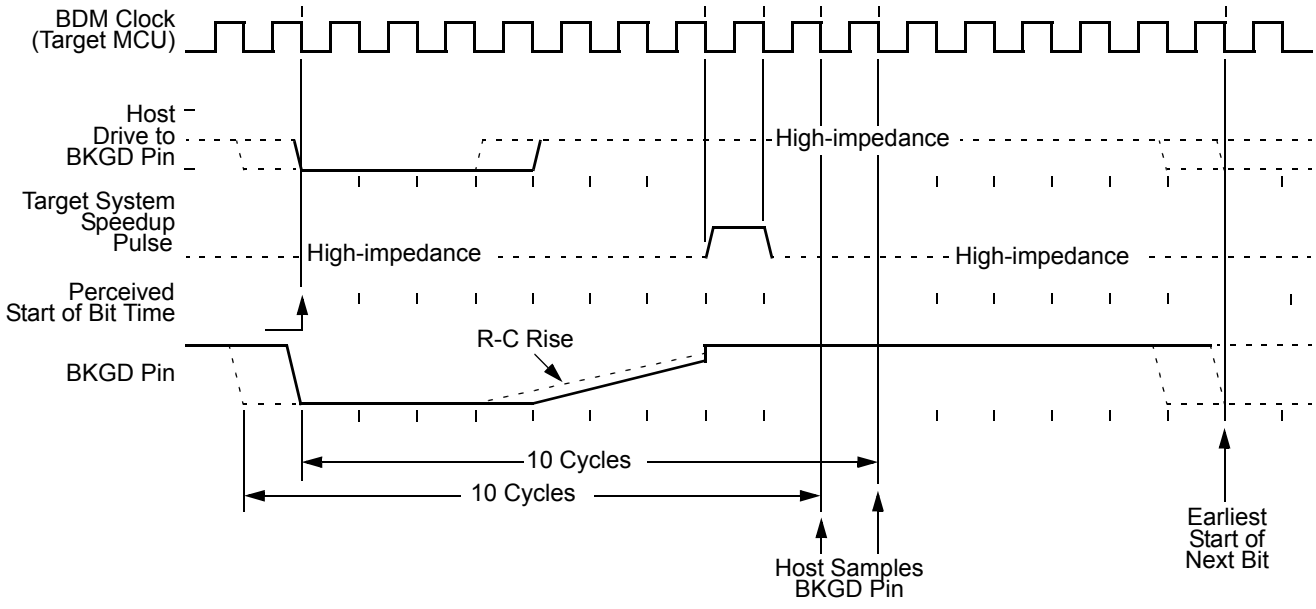

Figure 63. BDM Target-to-Host Serial Bit Timing (Logic 1)

Table 292. DBGXCTL Field Descriptions (continued)

Field	Description
5 TAG	**Tag Select**— This bit controls whether the comparator match has immediate effect, causing an immediate state sequencer transition or tag the opcode at the matched address. Tagged opcodes trigger only if they reach the execution stage of the instruction queue. 0 Allow state sequencer transition immediately on match 1 On match, tag the opcode. If the opcode is about to be executed allow a state sequencer transition
4 BRK	**Break**— This bit controls whether a comparator match terminates a debug session immediately, independent of state sequencer state. To generate an immediate breakpoint the module breakpoints must be enabled using the DBGC1 bit DBGBRK. 0 The debug session termination is dependent upon the state sequencer and trigger conditions. 1 A match on this channel terminates the debug session immediately; breakpoints if active are generated, tracing, if active, is terminated and the module disarmed.
3 RW	**Read/Write Comparator Value Bit** — The RW bit controls whether read or write is used in compare for the associated comparator. The RW bit is not used if RWE = 0. This bit is ignored if the TAG bit in the same register is set. 0 Write cycle will be matched 1 Read cycle will be matched
2 RWE	**Read/Write Enable Bit** — The RWE bit controls whether read or write comparison is enabled for the associated comparator.This bit is ignored if the TAG bit in the same register is set 0 Read/Write is not used in comparison 1 Read/Write is used in comparison
0 COMPE	Determines if comparator is enabled 0 The comparator is not enabled 1 The comparator is enabled

Table 293 shows the effect for RWE and RW on the comparison conditions. These bits are ignored if the corresponding TAG bit is set since the match occurs based on the tagged opcode reaching the execution stage of the instruction queue.

Table 293. Read or Write Comparison Logic Table

RWE Bit	RW Bit	RW Signal	Comment
0	x	0	RW not used in comparison
0	x	1	RW not used in comparison
1	0	0	Write data bus
1	0	1	No match
1	1	0	No match
1	1	1	Read data bus

4.31.3.2.8.2 Debug Comparator Address High Register (DBGXAH)

Table 294. Debug Comparator Address High Register (DBGXAH)

Address: 0x0029

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	Bit 17	Bit 16
W								
Reset	0	0	0	0	0	0	0	0

The DBGC1_COMRV bits determine which comparator address registers are visible in the 8-byte window from 0x0028 to 0x002F.

Table 295. Comparator Address Register Visibility

COMRV	Visible Comparator
00	DBGAAH, DBGAAM, DBGAAL

4.31.4.2.3 Range Comparisons

Using the AB comparator pair for a range comparison, the data bus can also be used for qualification by using the comparator A data registers. Furthermore the DBGACTL RW and RWE bits can be used to qualify the range comparison on either a read or a write access. The corresponding DBGBCTL bits are ignored. The SZE and SZ control bits are ignored in range mode. The comparator A TAG bit is used to tag range comparisons. The comparator B TAG bit is ignored in range modes. In order for a range comparison using comparators A and B, both COMPEA and COMPEB must be set; to disable range comparisons both must be cleared. The comparator A BRK bit is used to for the AB range, the comparator B BRK bit is ignored in range mode.

When configured for range comparisons and tagging, the ranges are accurate only to word boundaries.

4.31.4.2.3.1 Inside Range (CompA_Addr $\leq$ address $\leq$ CompB_Addr)

In the Inside Range comparator mode, comparator pair A and B can be configured for range comparisons. This configuration depends upon the control register (DBGC2). The match condition requires that a valid match for both comparators happens on the same bus cycle. A match condition on only one comparator is not valid. An aligned word access which straddles the range boundary is valid only if the aligned address is inside the range.

4.31.4.2.3.2 Outside Range (address < CompA_Addr or address > CompB_Addr)

In the outside range comparator mode, comparator pair A and B can be configured for range comparisons. A single match condition on either of the comparators is recognized as valid. An aligned word access which straddles the range boundary is valid only if the aligned address is outside the range.

Outside range mode in combination with tagging can be used to detect if the opcode fetches are from an unexpected range. In forced match mode the outside range match would typically be activated at any interrupt vector fetch or register access. This can be avoided by setting the upper range limit to $3FFFF or lower range limit to $00000 respectively.

4.31.4.3 Match Modes (Forced or Tagged)

Match modes are used as qualifiers for a state sequencer change of state. The Comparator control register TAG bits select the match mode. The modes are described in the following sections.

4.31.4.3.1 Forced Match

When configured for forced matching, a comparator channel match can immediately initiate a transition to the next state sequencer state whereby the corresponding flags in DBGSR are set. The state control register for the current state determines the next state. Forced matches are typically generated 2-3 bus cycles after the final matching address bus cycle, independent of comparator RWE/RW settings. Furthermore since opcode fetches occur several cycles before the opcode execution a forced match of an opcode address typically precedes a tagged match at the same address.

4.31.4.3.2 Tagged Match

If a CPU taghit occurs a transition to another state, sequencer state is initiated, and the corresponding DBGSR flags are set. For a comparator related taghit to occur, the DBG must first attach tags to instructions as they are fetched from memory. When the tagged instruction reaches the execution stage of the instruction queue a taghit is generated by the CPU. This can initiate a state sequencer transition.

4.31.4.3.3 Immediate Trigger

Independent of comparator matches it is possible to initiate a tracing session and/or breakpoint, by writing to the TRIG bit in DBGC1. This forces the state sequencer into the Final State and issues a forced breakpoint request to the CPU.

4.32.3.2.2 9S12I32PIMV1 Control Register 1 (CRGCTL1)

Table 322. 9S12I32PIMV1 Control Register (CRGCTL1)

0x0035

	7	6	5	4	3	2	1	0
R	BDIV[3:0]				0	0	LOCKIE	0
W								
Reset	0	0	0	0	0	0	0	0

Read: Anytime

Write: Anytime

Table 323. CRGCTL1 Field Descriptions

Field	Description
7, 6, 5, 4 BDIV[3:0]	Bus Divider Bits Depending on the setting of the BCLKS bit, either the DCO Clock or the Oscillator Clock is divided down in frequency to create the Core Clock. Bus frequency is Core frequency divided by 2. 0000 divide by 1 0001 divide by 2 0010 divide by 3 0011 divide by 4 0100 divide by 5 0101 divide by 6 0110 divide by 7 0111 divide by 8 1000 divide by 9 1001 divide by 10 1010 divide by 11 1011 divide by 12 1100 divide by 13 1101 divide by 14 1110 divide by 15 1111 divide by 16
1 LOCKIE	FLL Lock Interrupt Enable Bit 0 FLL Lock Interrupt requests are disabled. 1 FLL Lock Interrupt will be requested whenever LOCKIF is set.

4.32.3.2.3 9S12I32PIMV1 FLL Multiply Register (CRGMULT)

This register determines the multiplication factor to generate the DCO Clock.

Table 324. 9S12I32PIMV1 FLL Multiply Register (CRGMULT)

0x0036

	7	6	5	4	3	2	1	0
R	0	MULT[6:0]						
W								
Reset	0	0	0	0	0	0	0	0

Read: Anytime

Write: Anytime

Writing the CRGMULT register clears the LOCKST bit, but does not set the LOCKIF bit in the CRGFLG register.

4.32.5.2 Description of Reset Operation

NOTE

External circuitry connected to the RESET pin should not include a large capacitance that would interfere with the ability of this signal to rise to a valid logic one within 256 DCO Clock cycles after the low drive is released.

The reset sequence is initiated by any of the following events:

- Low level is detected at the RESET pin (External Reset).
- Power-on is detected.
- Illegal Address Access is detected (see MMC Block Guide for details).
- COP watchdog times out.
- Oscillator monitor failure is detected.

Upon detection of any reset event, an internal circuit drives the RESET pin low for 516 DCO Clock cycles. Depending on internal synchronization latency, it can also be 517 DCO Clock cycles (see Figure 77). Since entry into reset is asynchronous, it does not require a running DCO Clock. However, the internal reset circuit of the 9S12I32PIMV1 cannot sequence out of current reset condition without a running DCO Clock. After 516 DCO Clock cycles, the RESET pin is released. The reset generator of the 9S12I32PIMV1 waits for additional 256 DCO Clock cycles and then samples the RESET pin to determine the originating source. Table 334 shows which vector will be fetched.

Table 334. Reset Vector Selection

Sampled RESET Pin (256 cycles after release)	Oscillator monitor fail pending	COP timeout pending	Vector Fetch
1	0	0	POR /Illegal Address Access/External pin RESET
1	1	X	Oscillator Monitor Fail
1	0	1	COP time out
0	X	X	POR /Illegal Address Access/ External pin RESET

The internal reset of the MCU remains asserted while the reset generator completes the 768 DCO Clock long reset sequence. In case the RESET pin is externally driven low for more than these 768 DCO Clock cycles (External Reset), the internal reset remains asserted longer.

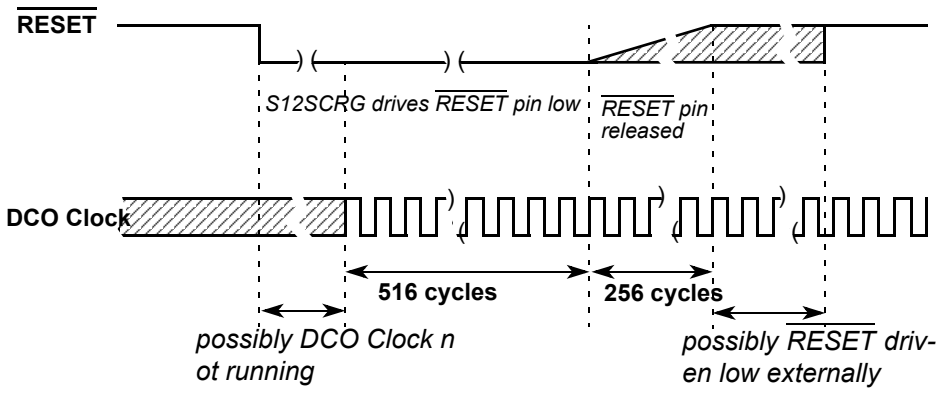

Figure 77. RESET Timing

4.32.5.2.1 Oscillator Monitor Reset

In case of loss of clock, or the oscillator frequency is below the failure assert frequency f_{OMFA} (see device electrical characteristics for values), the 9S12I32PIMV1 generates a Oscillator Monitor Reset.

4.38.3.2.1 SPI Control Register 1 (SPICR1)

Table 401. SPI Control Register 1 (SPICR1)

0x00E8

	7	6	5	4	3	2	1	0
R W	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
Reset	0	0	0	0	0	1	0	0

Read: Anytime

Write: Anytime

Table 402. SPICR1 Field Descriptions

Field	Description
7 SPIE	**SPI Interrupt Enable Bit** — This bit enables SPI interrupt requests, if the SPIF or MODF status flag is set. 0 SPI interrupts disabled. 1 SPI interrupts enabled.
6 SPE	**SPI System Enable Bit** — This bit enables the SPI system and dedicates the SPI port pins to SPI system functions. If SPE is cleared, SPI is disabled and forced into idle state, status bits in SPISR register are reset. 0 SPI disabled (lower power consumption). 1 SPI enabled, port pins are dedicated to SPI functions.
5 SPTIE	**SPI Transmit Interrupt Enable** — This bit enables SPI interrupt requests, if the SPTEF flag is set. 0 SPTEF interrupt disabled. 1 SPTEF interrupt enabled.
4 MSTR	**SPI Master/Slave Mode Select Bit** — This bit selects whether the SPI operates in master or slave mode. Switching the SPI from master to slave or vice versa forces the SPI system into idle state. 0 SPI is in slave mode. 1 SPI is in master mode.
3 CPOL	**SPI Clock Polarity Bit** — This bit selects an inverted or non-inverted SPI clock. To transmit data between SPI modules, the SPI modules must have identical CPOL values. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 Active-high clocks selected. In idle state SCK is low. 1 Active-low clocks selected. In idle state SCK is high.
2 CPHA	**SPI Clock Phase Bit** — This bit is used to select the SPI clock format. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 Sampling of data occurs at odd edges (1,3,5,...,15) of the SCK clock. 1 Sampling of data occurs at even edges (2,4,6,...,16) of the SCK clock.
1 SSOE	**Slave Select Output Enable** — The $\overline{SS}$ output feature is enabled only in master mode, if MODFEN is set, by asserting the SSOE as shown in Table 403. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state.
0 LSBFE	**LSB-First Enable** — This bit does not affect the position of the MSB and LSB in the data register. Reads and writes of the data register always have the MSB in bit 7. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 Data is transferred most significant bit first. 1 Data is transferred least significant bit first.