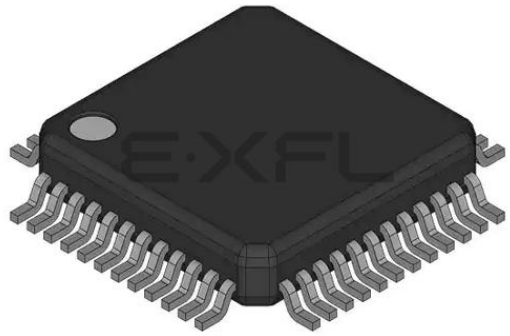

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RAM Size	2K x 8
Interface	LIN, SCI
Number of I/O	9
Voltage - Supply	2.25V ~ 5.5V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mm912f634dv2ap

3.4 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

3.4.1 Measurement Conditions

All measurements are without output loads. Unless otherwise noted, the currents are measured in MCU special single chip mode and the CPU code is executed from RAM.

Table 9. Supply Currents

Ratings	Symbol	Min	Typ[11]	Max	Unit
Normal Mode analog die only, excluding external loads, LIN Recessive State (5.5 V ≤ V_{SUP} ≤ 18 V, 2.25 V ≤ E_{VDD} ≤ 2.75 V, 4.5 V ≤ E_{VDDX} ≤ 5.5 V, -40 °C ≤ T_{J_A} ≤ 150 °C).	I_{RUN_A}	-	5.0	8.0	mA
Normal Mode MCU die only (T_{J_M} = 140 °C; V_{DD} = 2.75 V, V_{DDX} = 5.5 V, f_{OSC} = 4.0 MHz, f_{BUS} = f_{BUSMAX}[15])[12]	I_{RUN_M}	-	12.5	15	mA
Stop Mode internal analog die only, excluding external loads, LIN Recessive State, Lx enabled, measured at VS1+VS2 (5.5 V ≤ V_{SUP} ≤ 18 V, 2.25 V ≤ E_{VDD} ≤ 2.75 V, 4.5 V ≤ E_{VDDX} ≤ 5.5 V) -40 °C ≤ T_{J_A} ≤ 125 °C 125 °C < T_{J_A} ≤ 140 °C	I_{STOP_A}	 - -	 20 -	 40 50	µA
Stop Mode MCU die only (V_{DD} = 2.75 V, V_{DDX} = 5.5 V, f_{OSC} = 4.0 MHz, f_{BUS} = f_{BUSMAX}[15]; MCU in STOP; RTI and COP off)[13] T_{J_M} = 140 °C T_{J_M} = 105 °C T_{J_M} = 25 °C	I_{STOP_M}	 - - -	 0.135 0.035 0.010	 0.400 0.200 0.030	mA
Stop Mode MCU die only (V_{DD} = 2.75 V, V_{DDX} = 5.5 V, f_{OSC} = 4.0 MHz, f_{BUS} = f_{BUSMAX}[15]; MCU in STOP; RTI and COP on)[13] T_{J_M} = 140 °C T_{J_M} = 105 °C T_{J_M} = 25 °C	I_{STOP_M}	 - - -	 0.205 0.104 0.079	 0.500 0.300 0.110	mA
Wait Mode MCU die only (T_{J_M} = 140 °C; V_{DD} = 2.75 V, V_{DDX} = 5.5 V, f_{OSC} = 4.0 MHz, f_{BUS} = f_{BUSMAX}[15]; All modules except RTI disabled)[14]	I_{WAIT_M}	-	7.0	12	mA
Sleep Mode (VDD = VDDX = OFF; 5.5 V ≤ V_{SUP} ≤ 18 V; -40 °C ≤ T_{J_A} ≤ 150 °C; 3.0 V < L_X < 1.0 V).	I_{SLEEP}	-	15	28	µA
Cyclic Sense Supply Current Adder (5.0 ms Cycle)	I_{CS}	-	15	20	µA

Note:
11. Typical values noted reflect the approximate parameter mean at T_A = 25 °C
12. I_{RUN_M} denotes the sum of the currents flowing into VDD and VDDX.
13. I_{STOP_M} denotes the sum of the currents flowing into VDD and VDDX.
14. I_{WAIT_M} denotes the sum of the currents flowing into VDD and VDDX.
15. f_{BUSMAX} frequency ratings differ by device and is specified in Table 1.

3.8 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 stress test qualification for automotive grade integrated circuits. During the device qualification, ESD stresses were performed for the Human Body Model (HBM), Machine Model (MM), Charge Device Model (CDM), as well as LIN transceiver specific specifications.

A device will be defined as a failure if after exposure to ESD pulses, the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature, followed by hot temperature, unless specified otherwise in the device specification.

Table 46. ESD and Latch-up Protection Characteristics

Ratings	Symbol	Value	Unit
ESD - Human Body Model (HBM) following AEC-Q100 / JESD22-A114 (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω) - LIN (DGND, PGND, AGND, and LGND shorted) - VS1, VS2, VSENSE, Lx - HSx - All other Pins	V_{HBM}	 ±8000 ±4000 ±3000 ±2000	V
ESD - Charged Device Model (CDM) following AEC-Q100, Corner Pins (1, 12, 13, 24, 25, 36, 37, and 48) All other Pins	V_{CDM}	 ±750 ±500	V
ESD - Machine Model (MM) following AEC-Q100 (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), All Pins	V_{MM}	±200	V
Latch-up current at T_A = 125 °C[52]	I_{LAT}	±100	mA
ESD GUN - LIN Conformance Test Specification[54], unpowered, contact discharge, C_{ZAP}= 150 pF, R_{ZAP} = 330 Ω. - LIN (with or without bus filter C_{BUS}=220 pF) - VS1, VS2 with C_{VS} - Lx with serial R_{LX}		 ±15000 ±20000 ±6000	V
ESD GUN - IEC 61000-4-2 Test Specification[55], unpowered, contact discharge, C_{ZAP}= 150 pF, R_{ZAP} = 330 Ω - LIN (with or without bus filter C_{BUS}=220 pF) - VSENSE with serial R_{VSENSE}[53] - VS1, VS2 with C_{VS} - Lx with serial R_{LX}		 ±8000 ±8000 ±8000 ±8000	V
ESD GUN - ISO10605 Test Specification[55], unpowered, contact discharge, C_{ZAP}= 150 pF, R_{ZAP} = 2.0 kΩ - LIN (with or without bus filter C_{BUS}=220pF) - VSENSE with serial R_{VSENSE}[53] - VS1, VS2 with C_{VS} - Lx with serial R_{LX}		 ±6000 ±6000 ±6000 ±6000	V
ESD GUN - ISO10605 Test Specification[55], powered, contact discharge, C_{ZAP}= 330 pF, R_{ZAP} = 2.0 kΩ - LIN (with or without bus filter C_{BUS}=220 pF) - VSENSE with serial R_{VSENSE}[53] - VS1, VS2 with C_{VS} - Lx with serial R_{LX}		 ±8000 ±8000 ±8000 ±8000	V

Note:
52. Input Voltage Limit = -2.5 to 7.5 V.
53. With C_{VBAT} (10…100 nF) as part of the battery path.
54. Certification available on request
55. Tested internally only; certification pending

Table 59. 0x00E8–0x00EF Serial Peripheral Interface (SPI) (continued)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00ED	SPI0DR	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		W								
0x00EE	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x00EF	Reserved	R	0	0	0	0	0	0	0	0
		W								

Table 60. 0x00F0–0x00FF Reserved Register Space

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00F0-0x00FF	Reserved	R	0	0	0	0	0	0	0	0
		W								

Table 61. 0x0100–0x0113 Flash Control & Status Register FTSR

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0100	FCLKDIV	R	FDIVLD	PRDIV8	FDIV5	FDIV4	FDIV3	FDIV2	FDIV1	FDIV0
		W								
0x0101	FSEC	R	KEYEN1	KEYEN0	0	0	0	0	SEC1	SEC0
		W								
0x0102	FRSV0	R	0	0	0	0	0	0	0	0
		W								
0x0103	FCNFG	R	CBEIE	CCIE	KEYACC	0	0	0	0	0
		W								
0x0104	FPROT	R	FPHS4	FPHS3	FPHS2	FPHS1	FPHS0	FPLS2	FPLS1	FPLS0
		W								
0x0105	FSTAT	R	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
		W								
0x0106	FCMD	R	0	CMDB6	CMDB5	CMDB4	CMDB3	CMDB2	CMDB1	CMDB0
		W								
0x0107	FRSV1	R	0	0	0	0	0	0	0	0
		W								
0x0108	FADDRHI	R	0	0	0	0	0	0	0	0
		W			FAB13	FAB12	FAB11	FAB10	FAB9	FAB8
0x0109	FADDRLO	R	0	0	0	0	0	0	0	0
		W	FAB7	FAB6	FAB5	FAB4	FAB3	FAB2	FAB1	FAB0
0x010A	FDATAHI	R	FD15	FD14	FD13	FD12	FD11	FD10	FD9	FD8
		W								
0x010B	FDATALO	R	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
		W								
0x010C	FRSV2	R	0	0	0	0	0	0	0	0
		W								
0x010D	FRSV3	R	0	0	0	0	0	0	0	0
		W								

The Conversion Complete Register for the not available Lx analog input (3.8) must be ignored.

0x84	ACCSR (hi)	R	CC15	CC14	0	CC12	CC11	CC10	CC9	CC8
	ADC Conv Complete Reg	W								
0x85	ACCSR (lo)	R	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0
	ADC Conv Complete Reg	W								

The ADC Data Result Register for the not available Lx analog input (3.8) must be ignored.

0x8C-0 x97	ADRx (hi)	R	adrx 9	adrx 8	adrx 7	adrx 6	adrx 5	adrx 4	adrx 3	adrx 2
	ADC Data Result Register x	W								
	ADRx (lo)	R	adrx 1	adrx 0	0	0	0	0	0	0
	ADC Data Result Register x	W								

4.2.3.2.3 Functional Considerations

For the not available Lx inputs, the following functions are limited:

- No Wake-up feature / Cyclic Sense
- No Digital Input
- No Analog Input and conversion via ADC

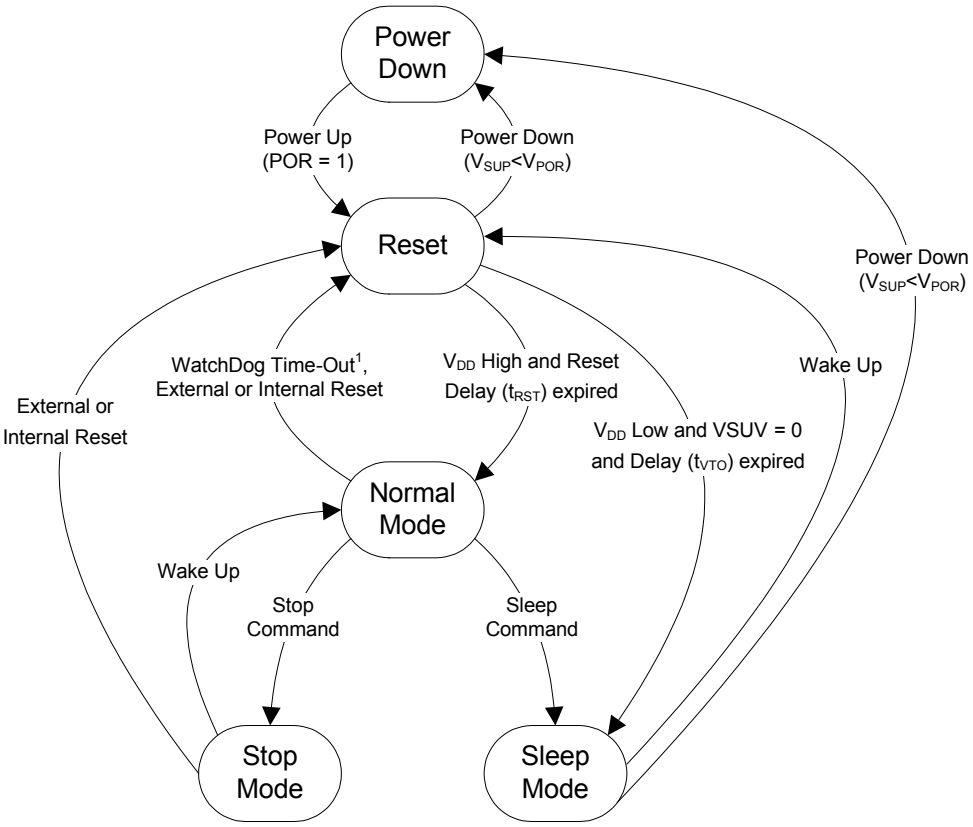
4.3 Modes of Operation

The MM912F634 analog die offers three main operating modes: Normal (Run), Stop, and Sleep. In Normal mode, the device is active and is operating under normal application conditions. In Stop mode, the voltage regulator operates with limited current capability, the external load is expected to be reduced while in Stop mode. In Sleep mode both voltage regulators are turned off (V_{DD} = V_{DDX} = 0 V).

Wake-up from Stop mode is indicated by an interrupt signal. Wake-up from Sleep mode will change the MM912F634 analog die into reset mode while the voltage regulator is turned back on.

The selection of the different modes is controlled by the Mode Control Register (MCR).

Figure 16 describes how transitions are done between the different operating modes.



[1] Initial WD to be served within t_{WDTO} to enable Window WD

Figure 16. Modes of Operation and Transitions

4.3.1 Power Down Mode

For the device power (VS1) below V_{POR}, the MM912F634 analog die is virtually in Power Down mode. Once VS1>V_{POR}, the MM912F634 analog die will enter Reset mode with the condition “Power On Reset - POR”.

4.3.2 Reset Mode

The MM912F634 analog die enters Reset mode if a reset condition occurs (POR - Power On Reset, LVR- Low Voltage Reset, Low Voltage VDDX Reset - LVRX, WDR - Watchdog Reset, EXR - External Reset, and WUR - Wake-up Sleep Reset).

Table 111. PWMCTL - Register Field Descriptions

Field	Description
7–6 CAE[1:0]	Center Aligned Output Modes on Channels 1–0 0 Channels 1–0 operate in left aligned output mode. 1 Channels 1–0 operate in center aligned output mode.
5 PCLK1	Pulse Width Channel 1 Clock Select 0 Clock B is the clock source for PWM channel 1. 1 Clock SB is the clock source for PWM channel 1.
4 PCLK0	Pulse Width Channel 0 Clock Select 0 Clock A is the clock source for PWM channel 0. 1 Clock SA is the clock source for PWM channel 0.
3–2 PPOL[1:0]	Pulse Width Channel 1–0 Polarity Bits 0 PWM channel 1–0 outputs are low at the beginning of the period, then go high when the duty count is reached. 1 PWM channel 1–0 outputs are high at the beginning of the period, then go low when the duty count is reached.
1-0 PWME[1:0]	Pulse Width Channel 1–0 Enable 0 Pulse width channel 1–0 is disabled. 1 Pulse width channel 1–0 is enabled. The pulse modulated signal becomes available at PWM, output bit 1 when its clock source begins its next cycle.

4.13.3.1.1 PWM Enable (PWMEx)

NOTE

The first PWM cycle after enabling the channel can be irregular. If both PWM channels are disabled (PWME1–0 = 0), the prescaler counter shuts off for power savings.

Each PWM channel has an enable bit (PWMEx) to start its waveform output. When any of the PWMEx bits are set (PWMEx = 1), the associated PWM output is enabled immediately. However, the actual PWM waveform is not available on the associated PWM output until its clock source begins its next cycle, due to the synchronization of PWMEx and the clock source.

4.13.3.1.2 PWM Polarity (PPOLx)

NOTE

PPOLx register bits can be written anytime. If the polarity changes while a PWM signal is being generated, a truncated or stretched pulse can occur during the transition

The starting polarity of each PWM channel waveform is determined by the associated PPOLx bit. If the polarity bit is one, the PWM channel output is high at the beginning of the cycle and then goes low when the duty count is reached. Conversely, if the polarity bit is zero, the output starts low and then goes high when the duty count is reached.

4.13.3.1.3 PWM Clock Select (PCLKx)

NOTE

Register bits PCLK0 and PCLK1 can be written anytime. If a clock select changes while a PWM signal is being generated, a truncated or stretched pulse can occur during the transition.

Each PWM channel has a choice of two clocks to use as the clock source for that channel as described by the following.

Table 175. TIE - Register Field Descriptions (continued)

Field	Description
3 TCRE	TCRE — Timer Counter Reset Enable 1 = Enables Timer Counter reset by a successful output compare on channel 3 0 = Inhibits Timer Counter reset and counter continues to run.
3-0 PR[2:0]	Timer Prescaler Select These three bits select the frequency of the timer prescaler clock derived from the Bus Clock as shown in Table 176.

Table 176. Timer Clock Selection

PR2	PR1	PR0	Timer Clock
0	0	0	D2D Clock / 1
0	0	1	D2D Clock / 2
0	1	0	D2D Clock / 4
0	1	1	D2D Clock / 8
1	0	0	D2D Clock / 16
1	0	1	D2D Clock / 32
1	1	0	D2D Clock / 64
1	1	1	D2D Clock / 128

4.18.3.3.12 Main Timer Interrupt Flag 1 (TFLG1)

NOTE

These flags are set when an input capture or output compare event occurs. Flag set on a particular channel is cleared by writing a one to that corresponding CnF bit. Writing a zero to CnF bit has no effect on its status. When TFFCA bit in TSCR register is set, a read from an input capture or a write into an output compare channel will cause the corresponding channel flag CnF to be cleared.

Table 177. Main Timer Interrupt Flag 1 (TFLG1)

Offset[126] 0xCC Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	C3F	C2F	C1F	C0F
W								
Reset	0	0	0	0	0	0	0	0

Note:
126. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 178. TFLG1 - Register Field Descriptions

Field	Description
3-0 C[3:0]F	Input Capture/Output Compare Channel Flag. 1 = Input Capture or Output Compare event occurred 0 = No event (Input Capture or Output Compare event) occurred.

Table 188. Analog Digital Converter Module - Memory Map (continued)

Register / Offset[132]		Bit 7	6	5	4	3	2	1	Bit 0
0x8D ADR3 (lo)	R	ADR3[1:0]							
	W								
0x8E ADR4 (hi)	R	ADR4[9:2]							
	W								
0x8F ADR4 (lo)	R	ADR4[1:0]							
	W								
0x90 ADR5 (hi)	R	ADR5[9:2]							
	W								
0x91 ADR5 (lo)	R	ADR5[1:0]							
	W								
0x92 ADR6 (hi)	R	ADR6[9:2]							
	W								
0x93 ADR6 (lo)	R	ADR6[1:0]							
	W								
0x94 ADR7 (hi)	R	ADR7[9:2]							
	W								
0x95 ADR7 (lo)	R	ADR7[1:0]							
	W								
0x96 ADR8 (hi)	R	ADR8[9:2]							
	W								
0x97 ADR8 (lo)	R	ADR8[1:0]							
	W								
0x98 ADR9 (hi)	R	ADR9[9:2]							
	W								
0x99 ADR9 (lo)	R	ADR9[1:0]							
	W								
0x9A ADR10 (hi)	R	ADR10[9:2]							
	W								
0x9B ADR10 (lo)	R	ADR10[1:0]							
	W								
0x9C ADR11 (hi)	R	ADR11[9:2]							
	W								
0x9D ADR11 (lo)	R	ADR11[1:0]							
	W								
0x9E ADR12 (hi)	R	ADR12[9:2]							
	W								
0x9F ADR12 (lo)	R	ADR12[1:0]							
	W								
0xA0 Reserved	R								
	W								
0xA1 Reserved	R								
	W								

Table 190. ACR - Register Field Descriptions (continued)

Field	Description
4 - ADCRST	Analog Digital Converter RESET 0 - Analog Digital Converter in Normal Operation 1 - Analog Digital Converter in Reset Mode, all ADC registers will reset to initial values. The bit has to be cleared to allow ADC operation.
2-0 PS2…0	ADC Clock Prescaler Select (D2DCLK to ADCCLK divider) 000 - 10 001 - 8 010 - 6 011 - 4 100 - 2 101 - 1 110 - 1 111 - 1

4.19.4.2.2 ADC Status Register (ASR)

Table 191. ADC Status Register (ASR)

Offset[134] 0x81 Access: User read/write

	7	6	5	4	3	2	1	0
R	SCF	2p5CLF	0	0	CCNT3	CCNT2	CCNT1	CCNT0
W								
Reset	0	0	0	0	1	1	1	1

Note:
134. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 192. ACR - Register Field Descriptions

Field	Description
7 - SCF	Sequence Complete Flag. Reading the ADC Status Register (ASR) will clear the Flag.
6 - 2p5CLF	ADC Reference Voltage Current Limitation Flag
3-0 CCNT3…0	Conversion Counter Status. The content of CCNT reflects the current channel in conversion and the conversion of CCNT-1 being complete. The conversion order is CH15, CH0, CH1,..., CH14.

4.19.4.2.3 ADC Conversion Control Register (ACCR)

Table 193. ADC Conversion Control Register (ACCR)

Offset[135] 0x82 (0x82 and 0x83 for 8-Bit access) Access: User read/write

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	CH15	CH14	0	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
135. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 215. Interrupt Vector Locations (continued)

Vector Address[153]	Interrupt Source	CCR Mask	Local Enable
Vector base+ $F0	Real time interrupt	I bit	(RTIE)
Vector base + $D8	SPI	I bit	SPICR1 (SPIE, SPTIE)
Vector base + $C6	CRG FLL lock	I bit	CRGCTL1(LOCKIE)
Vector base + $B8	FLASH	I bit	FCNFG (CBEIE, CCIE)
Vector base + $80	Spurious Interrupt	-	None

Note:
153. 16 bits vector address based

4.26.8.3 Effects of Reset

When a reset occurs, MCU registers and control bits are changed to known start-up states. Refer to the respective block descriptions for register reset states.

4.26.8.3.1 I/O Pins

Refer to the 4.27, “Port Integration Module (9S12I32PIMV1)“ description for reset configurations of all peripheral module ports.

4.26.8.3.2 Memory

The RAM array is not initialized out of reset.

The hardware handshake protocol is enabled by the ACK_ENABLE and disabled by the ACK_DISABLE BDM commands. This provides backwards compatibility with the existing POD devices which are not able to execute the hardware handshake protocol. It also allows for new POD devices, that support the hardware handshake protocol, to freely communicate with the target device. If desired, without the need for waiting for the ACK pulse.

The commands are described as follows:

- ACK_ENABLE — enables the hardware handshake protocol. The target will issue the ACK pulse when a CPU command is executed by the CPU. The ACK_ENABLE command itself also has the ACK pulse as a response.
- ACK_DISABLE — disables the ACK pulse protocol. In this case, the host needs to use the worst case delay time at the appropriate places in the protocol.

The default state of the BDM after reset is hardware handshake protocol disabled.

All the read commands will ACK (if enabled) when the data bus cycle has completed, and the data is then ready for reading out by the BKGD serial pin. All the write commands will ACK (if enabled) after the data has been received by the BDM through the BKGD serial pin, and when the data bus cycle is complete. See Section 4.30.4.3, “BDM Hardware Commands"” and Section 4.30.4.4, “Standard BDM Firmware Commands"” for more information on the BDM commands.

The ACK_ENABLE sends an ACK pulse when the command has been completed. This feature could be used by the host to evaluate if the target supports the hardware handshake protocol. If an ACK pulse is issued in response to this command, the host knows that the target supports the hardware handshake protocol. If the target does not support the hardware handshake protocol the ACK pulse is not issued. In this case, the ACK_ENABLE command is ignored by the target since it is not recognized as a valid command.

The BACKGROUND command will issue an ACK pulse when the CPU changes from normal to background mode. The ACK pulse related to this command could be aborted using the SYNC command.

The GO command will issue an ACK pulse when the CPU exits from background mode. The ACK pulse related to this command could be aborted using the SYNC command.

The GO_UNTIL[(169)] command is equivalent to a GO command with exception that the ACK pulse, in this case, is issued when the CPU enters into background mode. This command is an alternative to the GO command and should be used when the host wants to trace if a breakpoint match occurs, and causes the CPU to enter active background mode. Note that the ACK is issued whenever the CPU enters BDM, which could be caused by a breakpoint match or by a BGND instruction being executed. The ACK pulse related to this command could be aborted using the SYNC command.

The TRACE1 command has the related ACK pulse issued when the CPU enters background active mode after one instruction of the application program is executed. The ACK pulse related to this command could be aborted using the SYNC command.

4.30.4.9 SYNC — Request Timed Reference Pulse

The SYNC command is unlike other BDM commands, because the host does not necessarily know the correct communication speed to use for BDM communications until after it has analyzed the response to the SYNC command. To issue a SYNC command, the host should perform the following steps:

1. Drive the BKGD pin low for at least 128 cycles at the lowest possible BDM serial communication frequency (the lowest serial communication frequency is determined by either DCO clock or external crystal oscillator depending on the configuration chosen in the CRG.)
2. Drive BKGD high for a brief speedup pulse to get a fast rise time (this speedup pulse is typically one cycle of the host clock.)
3. Remove all drive to the BKGD pin so it reverts to high-impedance.
4. Listen to the BKGD pin for the sync response pulse.

4.31.4.5.3.1 Loop1 Mode

NOTE

In certain very tight loops, the source address will have already been fetched again before the background comparator is updated. This results in the source address being stored twice before further duplicate entries are suppressed. This condition occurs with branch-on-bit instructions when the branch is fetched by the first P-cycle of the branch or with loop-construct instructions in which the branch is fetched with the first or second P cycle. See examples below:

Loop1 mode, similarly to Normal mode also stores only COF address information to the trace buffer, it however allows the filtering out of redundant information.

The intent of Loop1 mode is to prevent the Trace Buffer from being filled entirely with duplicate information from a looping construct such as delays using the DBNE instruction or polling loops using BRSET/BRCLR instructions. Immediately after address information is placed in the Trace Buffer, the DBG module writes this value into a background register. This prevents consecutive duplicate address entries in the Trace Buffer resulting from repeated branches.

Loop1 mode only inhibits consecutive duplicate source address entries that would typically be stored in most tight looping constructs. It does not inhibit repeated entries of destination addresses or vector addresses, since repeated entries of these would most likely indicate a bug in the user's code that the DBG module is designed to help find.

```
LOOP    INX                     ; 1-byte instruction fetched by 1st P-cycle of BRCLR
        BRCLR       CMPTMP,#$0c,LOOP ; the BRCLR instruction also will be fetched by 1st
                                ; P-cycle of BRCLR

LOOP2   BRN     *               ; 2-byte instruction fetched by 1st P-cycle of DBNE
        NOP                     ; 1-byte instruction fetched by 2nd P-cycle of DBNE
        DBNE        A,LOOP2     ; this instruction also fetched by 2nd P-cycle of DBNE
```

4.31.4.5.3.2 Detail Mode

In Detail Mode, address and data for all memory and register accesses is stored in the trace buffer. This mode is intended to supply additional information on indexed, indirect addressing modes, where storing only the destination address would not provide all information required for a user to determine where the code is in error. This mode also features information bit storage to the trace buffer, for each address byte storage. The information bits indicates the size of access (word or byte) and the type of access (read or write).

When tracing in Detail mode, all cycles are traced except those when the CPU is either in a free or opcode fetch cycle.

4.31.4.5.3.3 Pure PC Mode

NOTE:

When tracing is terminated using forced breakpoints, latency in breakpoint generation means that opcodes following the opcode causing the breakpoint can be stored to the trace buffer. The number of opcodes is dependent on program flow. This should be avoided by using tagged breakpoints.

In Pure PC mode, tracing from the CPU the PC addresses of all executed opcodes, including illegal opcodes are stored.

4.32.3.2.2 9S12I32PIMV1 Control Register 1 (CRGCTL1)

Table 322. 9S12I32PIMV1 Control Register (CRGCTL1)

0x0035

	7	6	5	4	3	2	1	0
R	BDIV[3:0]				0	0	LOCKIE	0
W								
Reset	0	0	0	0	0	0	0	0

Read: Anytime

Write: Anytime

Table 323. CRGCTL1 Field Descriptions

Field	Description
7, 6, 5, 4 BDIV[3:0]	Bus Divider Bits Depending on the setting of the BCLKS bit, either the DCO Clock or the Oscillator Clock is divided down in frequency to create the Core Clock. Bus frequency is Core frequency divided by 2. 0000 divide by 1 0001 divide by 2 0010 divide by 3 0011 divide by 4 0100 divide by 5 0101 divide by 6 0110 divide by 7 0111 divide by 8 1000 divide by 9 1001 divide by 10 1010 divide by 11 1011 divide by 12 1100 divide by 13 1101 divide by 14 1110 divide by 15 1111 divide by 16
1 LOCKIE	FLL Lock Interrupt Enable Bit 0 FLL Lock Interrupt requests are disabled. 1 FLL Lock Interrupt will be requested whenever LOCKIF is set.

4.32.3.2.3 9S12I32PIMV1 FLL Multiply Register (CRGMULT)

This register determines the multiplication factor to generate the DCO Clock.

Table 324. 9S12I32PIMV1 FLL Multiply Register (CRGMULT)

0x0036

	7	6	5	4	3	2	1	0
R	0	MULT[6:0]						
W								
Reset	0	0	0	0	0	0	0	0

Read: Anytime

Write: Anytime

Writing the CRGMULT register clears the LOCKST bit, but does not set the LOCKIF bit in the CRGFLG register.

Table 338. RTICTL Field Descriptions (continued)

Field	Description
4 RTISWAI	RTI Stops in Wait Mode Bit Normal modes: Write once Special modes: Write anytime. 0 RTI keeps running in Wait mode. 1 RTI stops and initializes the RTI counter whenever the part enters Wait mode.
3 RTIRSTP	**RTI Runs in Stop Mode Bit** Normal modes: Write once Special modes: Write anytime. 0 RTI stops in Stop mode 1 RTI continues in Stop mode **Note:** If the RTIRSTP bit is cleared the RTI counter will go static while in Stop mode. The RTI counter will not initialize like in Wait mode with RTISWAI bit set.
2 RTIE	Real Time Interrupt Enable Bit Write anytime. 0 Interrupt requests from RTI are disabled. 1 Interrupt will be requested whenever RTIF is set.
1–0 RTIRT[1:0]	**RTI Interrupt Prescaler Rate Select Bits** — These bits select the prescaler rate for the RTI. See Table 340., “RTI Frequency Divide Rates“ for selectable ratios in conjunction with RTICNT[7:0] counter select bits Write anytime in appliance of the write protection rules (see 4.34.7.1, “RTI register write protection rules“).

4.34.6.2.2 RTI Counter select bits (RTICNT)

This register is used to restart the RTI time-out period.

Table 339. RTICNT Register Diagram

0x003D

	7	6	5	4	3	2	1	0
R W	RTICNT7	RTICNT6	RTICNT5	RTICNT4	RTICNT3	RTICNT2	RTICNT1	RTICNT0
Reset	0	0	0	0	0	0	0	0

Read: Anytime

Write: Anytime in appliance of the write protection rules (see 4.34.7.1, “RTI register write protection rules“)

When the RTI is turned on the RTIF bit can be set with the following rates:

Table 340. RTI Frequency Divide Rates

RTICNT[7:0]	RTIRT[1:0] =			
	00 (OFF)	**01 (1)**	**10 (16)**	**11 (256)**
0000 0000 (÷1)	OFF(185)	OFF	16	256
0000 0001 (÷2)	OFF	2x1	2x16	2x256
0000 0010 (÷3)	OFF	3x1	3x16	3x256
0000 0011 (÷4)	OFF	4x1	4x16	4x256
.....	....	....	....	....
1111 1110 (÷255)	OFF	255x1	255x16	255x256

Table 343. COPCTL Field Descriptions (continued)

Field	Description
3 COPRSTP	**COP Runs in Stop Mode Bit** Normal modes: Write once Special modes: Write anytime 0 COP stops in Stop mode 1 COP continues in Stop mode **Note:** If the COPRSTP bit is cleared the COP counter will go static while in Stop mode. The COP counter will not initialize like in Wait mode with COPSWAI bit set.
2–0 CR[2:0]	**COP Watchdog Timer Rate Select Bits** — These bits select the COP timeout rate (see Table 344). Writing a non-zero value to CR[2:0] enables the COP counter and starts the timeout period. A COP counter timeout causes a system reset. This can be avoided by periodically (before timeout) re-initialize the COP counter via the ARMCOP register. While all of the following four conditions are true the CR[2:0], WCOP bits are ignored and the COP operates at highest timeout period (2^{16} cycles) in normal COP mode (Window COP mode disabled): 1) COP is enabled (CR[2:0] is not 000) 2) BDM mode active 3) RSBCK = 0 4) Operation in special mode

Table 344. COP Watchdog Rates(187)

CR2	CR1	CR0	Input_CLK Cycles to Timeout
0	0	0	COP disabled
0	0	1	2^6
0	1	0	2^8
0	1	1	2^{10}
1	0	0	2^{12}
1	0	1	2^{14}
1	1	0	2^{15}
1	1	1	2^{16}

Note:
187. Refer to Device User Guide (Section 4.35.4.1, “COP Configuration") for reset values of WCOP, CR2, CR1 and CR0.

4.36.1.3 Block Diagram

A block diagram of the Flash module is shown in Figure 83.

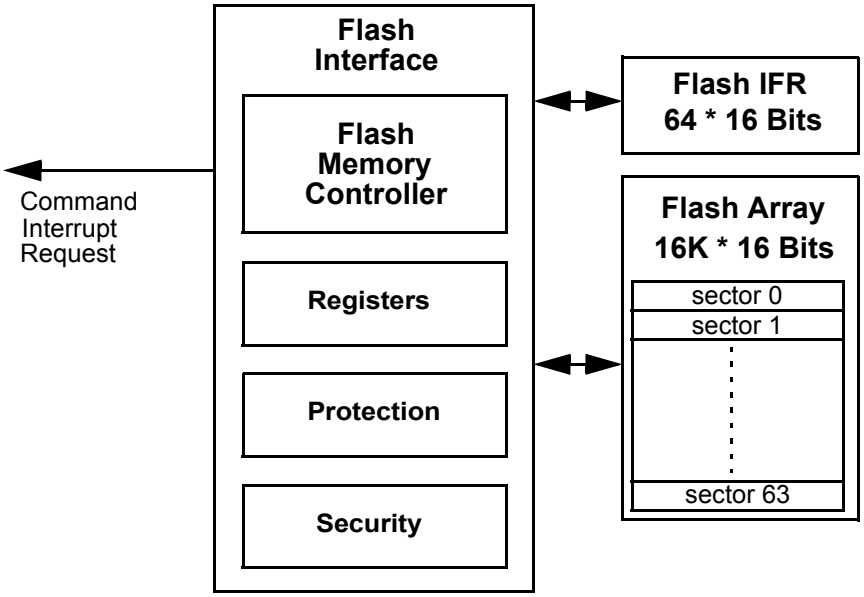


Figure 83. S12SFTSR32K Block Diagram

4.36.2 External Signal Description

The Flash module has no external signals.

If an address to be programmed is in a protected area of the Flash block, the PVIOL flag in the FSTAT register will set and the program command will not launch. Once the program command has successfully launched, the CCIF flag in the FSTAT register will set after the program operation has completed.

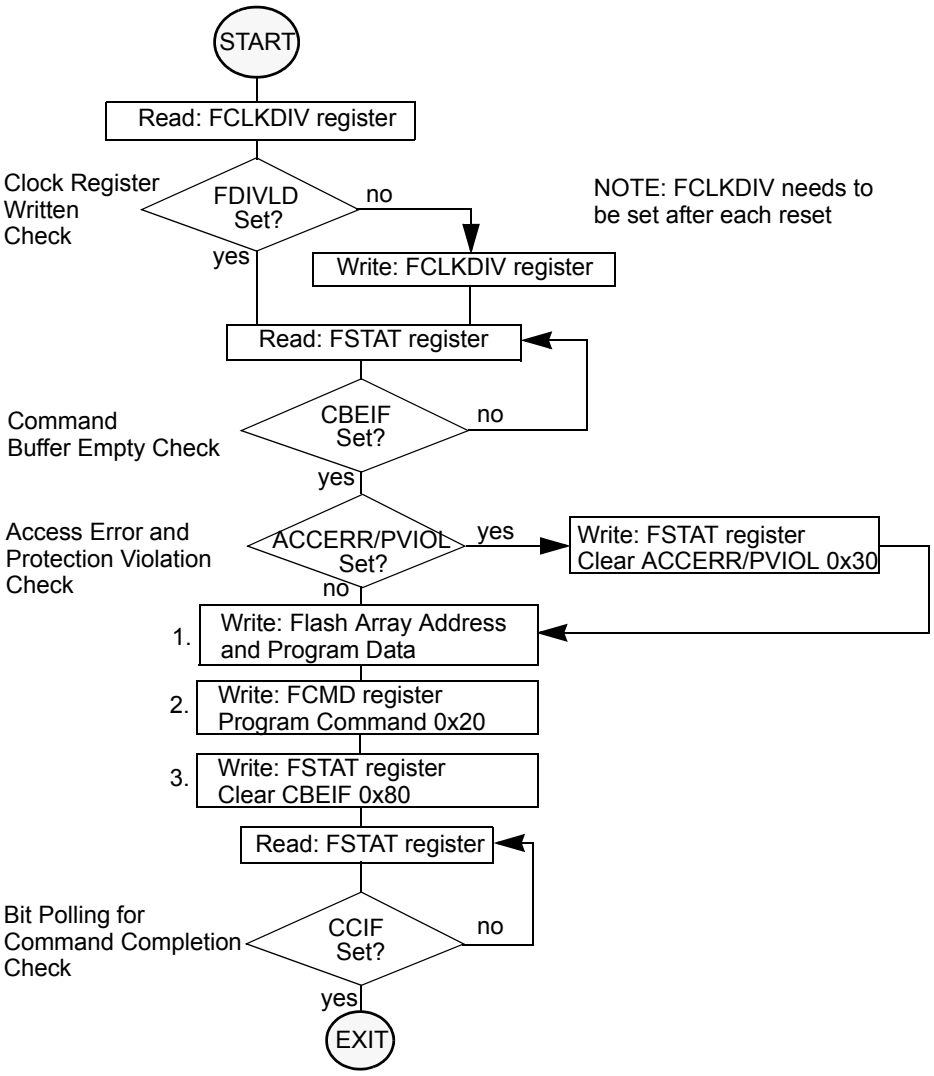


Figure 87. Example Program Command Flow

4.36.4.2.3 Burst Program Command

The burst program operation will program previously erased data in the Flash memory using an embedded algorithm.

While burst programming, two internal data registers operate as a buffer and a register (2-stage FIFO), so that a second burst programming command along with the necessary data can be stored to the buffers, while the first burst programming command is still in progress. This pipelined operation allows a time optimization when programming more than one consecutive address on a specific row in the Flash array as the high voltage generation can be kept active in between two programming commands.

An example flow to execute the burst program operation is shown in Figure 88. The burst program command write sequence is as follows:

1. Write to an aligned Flash block address to start the command write sequence for the burst program command. The data written will be programmed to the address written.

4.36.4.2.5 Mass Erase Command

The mass erase operation will erase the entire Flash array memory using an embedded algorithm.

An example flow to execute the mass erase operation is shown in Figure 90. The mass erase command write sequence is as follows:

1. Write to an aligned Flash block address to start the command write sequence for the mass erase command. The address and data written will be ignored.
2. Write the mass erase command, 0x41, to the FCMD register.
3. Clear the CBEIF flag in the FSTAT register by writing a 1 to CBEIF to launch the mass erase command.

If the Flash array memory to be mass erased contains any protected area, the PVIOL flag in the FSTAT register will set and the mass erase command will not launch. Once the mass erase command has successfully launched, the CCIF flag in the FSTAT register will set after the mass erase operation has completed.

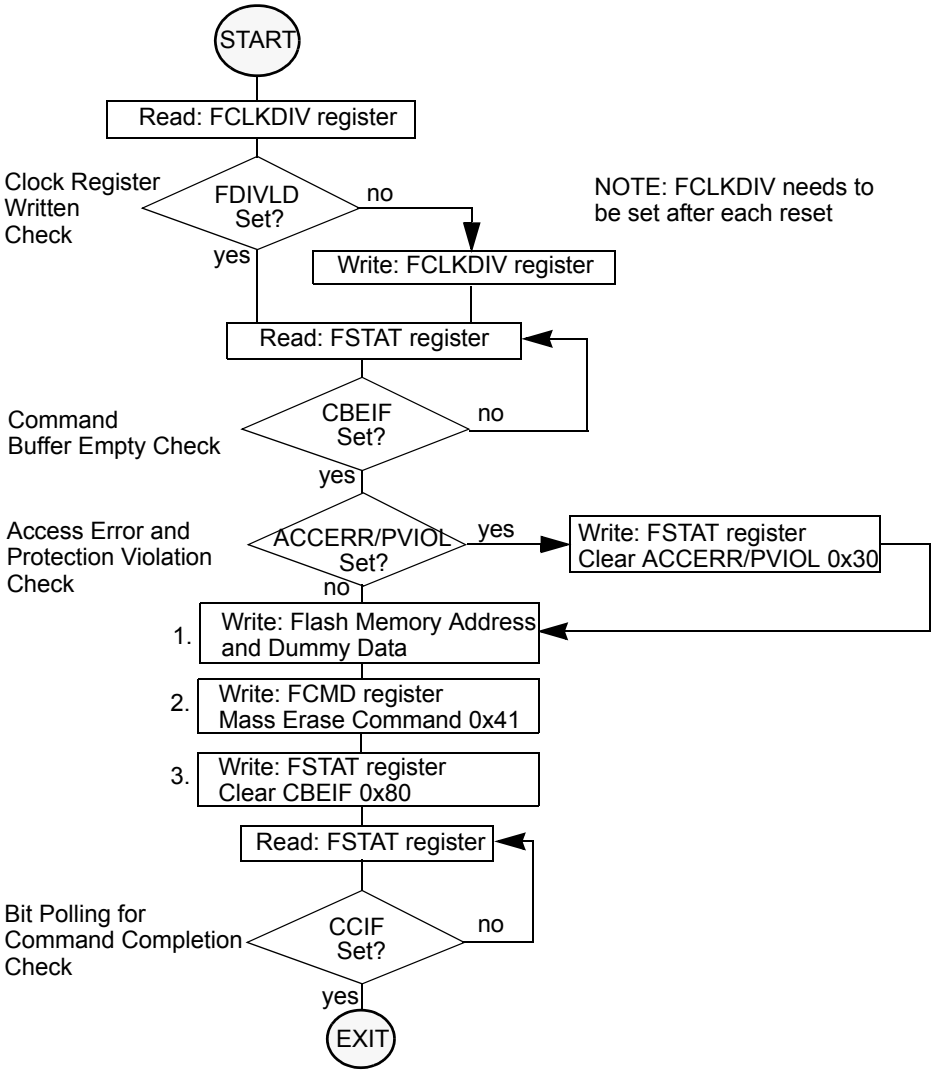


Figure 90. Example Mass Erase Command Flow

Table 406. Bidirectional Pin Configurations

Pin Mode	SPC0	BIDIROE	MISO	MOSI
Master Mode of Operation				
Normal	0	X	Master In	Master Out
Bidirectional	1	0	MISO not used by SPI	Master In
		1		Master I/O
Slave Mode of Operation				
Normal	0	X	Slave Out	Slave In
Bidirectional	1	0	Slave In	MOSI not used by SPI
		1	Slave I/O	

4.38.3.2.3 SPI Baud Rate Register (SPIBR)

NOTE

For maximum allowed baud rates, refer to Section 3.6.2.4, “SPI Timing" in this data sheet.

Table 407. SPI Baud Rate Register (SPIBR)

0x00EA

	7	6	5	4	3	2	1	0
R	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
W								
Reset	0	0	0	0	0	0	0	0

Read: Anytime

Write: Anytime; writes to the reserved bits have no effect

Table 408. SPIBR Field Descriptions

Field	Description
6–4 SPPR[2:0]	**SPI Baud Rate Preselection Bits** — These bits specify the SPI baud rates as shown in Table 409. In master mode, a change of these bits will abort a transmission in progress and force the SPI system into idle state.
2–0 SPR[2:0]	**SPI Baud Rate Selection Bits** — These bits specify the SPI baud rates as shown in Table 409. In master mode, a change of these bits will abort a transmission in progress and force the SPI system into idle state.

The baud rate divisor equation is as follows:

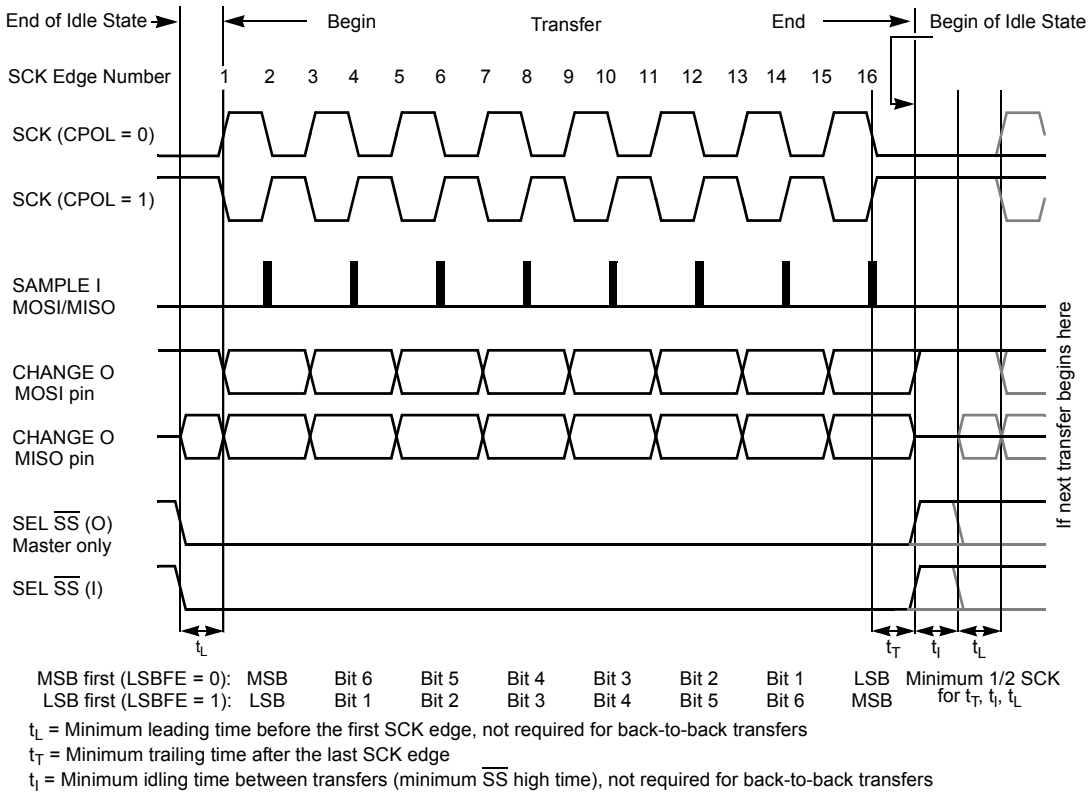
$$\text{BaudRateDivisor} = (\text{SPPR} + 1) \bullet 2^{(\text{SPR} + 1)} \qquad \textit{Eqn. 2}$$

The baud rate can be calculated with the following equation:

$$\text{Baud Rate} = \text{BusClock} / \text{BaudRateDivisor} \qquad \textit{Eqn. 3}$$

Table 409. Example SPI Baud Rate Selection (20 MHz Bus Clock)

SPPR2	SPPR1	SPPR0	SPR2	SPR1	SPR0	Baud Rate Divisor	Baud Rate
0	0	0	0	0	0	2	10.0 MHz
0	0	0	0	0	1	4	5.00 MHz
0	0	0	0	1	0	8	2.50 MHz



t_L = Minimum leading time before the first SCK edge, not required for back-to-back transfers
t_T = Minimum trailing time after the last SCK edge
t_I = Minimum idling time between transfers (minimum $\overline{SS}$ high time), not required for back-to-back transfers

Figure 104. SPI Clock Format 1 (CPHA = 1)

The $\overline{SS}$ line can remain active low between successive transfers (can be tied low at all times). This format is sometimes preferred in systems having a single fixed master and a single slave that drive the MISO data line.

- Back-to-back transfers in master mode
  In master mode, if a transmission has completed and a new data byte is available in the SPI data register, this byte is sent out immediately without a trailing and minimum idle time.

The SPI interrupt request flag (SPIF) is common to both the master and slave modes. SPIF gets set one half SCK cycle after the last SCK edge.

4.38.4.4 SPI Baud Rate Generation

NOTE

For maximum allowed baud rates, refer to Section 3.6.2.4, “SPI Timing" in this data sheet.

Baud rate generation consists of a series of divider stages. Six bits in the SPI baud rate register (SPPR2, SPPR1, SPPR0, SPR2, SPR1, and SPR0) determine the divisor to the SPI module clock which results in the SPI baud rate.

The SPI clock rate is determined by the product of the value in the baud rate preselection bits (SPPR2–SPPR0) and the value in the baud rate selection bits (SPR2–SPR0). The module clock divisor equation is shown in Equation 4.

$$\text{BaudRateDivisor} = (\text{SPPR} + 1) \bullet 2^{(\text{SPR} + 1)} \qquad \textit{Eqn. 4}$$

When all bits are clear (the default condition), the SPI module clock is divided by 2. When the selection bits (SPR2–SPR0) are 001 and the preselection bits (SPPR2–SPPR0) are 000, the module clock divisor becomes 4. When the selection bits are 010, the module clock divisor becomes 8, etc.