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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, I ² C, IEBus, SIO, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	45
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30840sgp-u5

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin ⁽¹⁾
97		P24					AN24	A4(/D4)
98		P23					AN23	A3(/D3)
99		P22					AN22	A2(/D2)
100		P21					AN21	A1(/D1)
101		P20					AN20	A0(/D0)
102		P17	INT5					D15
103		P16	INT4					D14
104		P15	INT3					D13
105		P14						D12
106		P13						D11
107		P12						D10
108		P11						D9
109		P10						D8
110		P07					AN07	D7
111		P06					AN06	D6
112		P05					AN05	D5
113		P04					AN04	D4
114		P114						
115		P113				INPC13/OUTC13		
116		P112				INPC12/OUTC12/ISRxD1/BE1IN		
117		P111				INPC11/OUTC11/ISCLK1		
118		P110				INPC10/OUTC10/ISTxD1/BE1OUT		
119		P03					AN03	D3
120		P02					AN02	D2
121		P01					AN01	D1
122		P00					AN00	D0
123		P157					AN157	
124		P156					AN156	
125		P155					AN155	
126		P154					AN154	
127		P153					AN153	
128		P152				ISRxD0	AN152	
129		P151				ISCLK0	AN151	
130	VSS							
131		P150				ISTxD0	AN150	
132	VCC1							
133		P107	KI3				AN7	
134		P106	KI2				AN6	
135		P105	KI1				AN5	
136		P104	KI0				AN4	
137		P103					AN3	
138		P102					AN2	
139		P101					AN1	
140	AVSS							
141		P100					AN0	
142	VREF							
143	AVCC							
144		P97			RxD4/SCL4/STxD4		ADTRG	

NOTES:

1. Bus control pins in M32C/84T cannot be used.

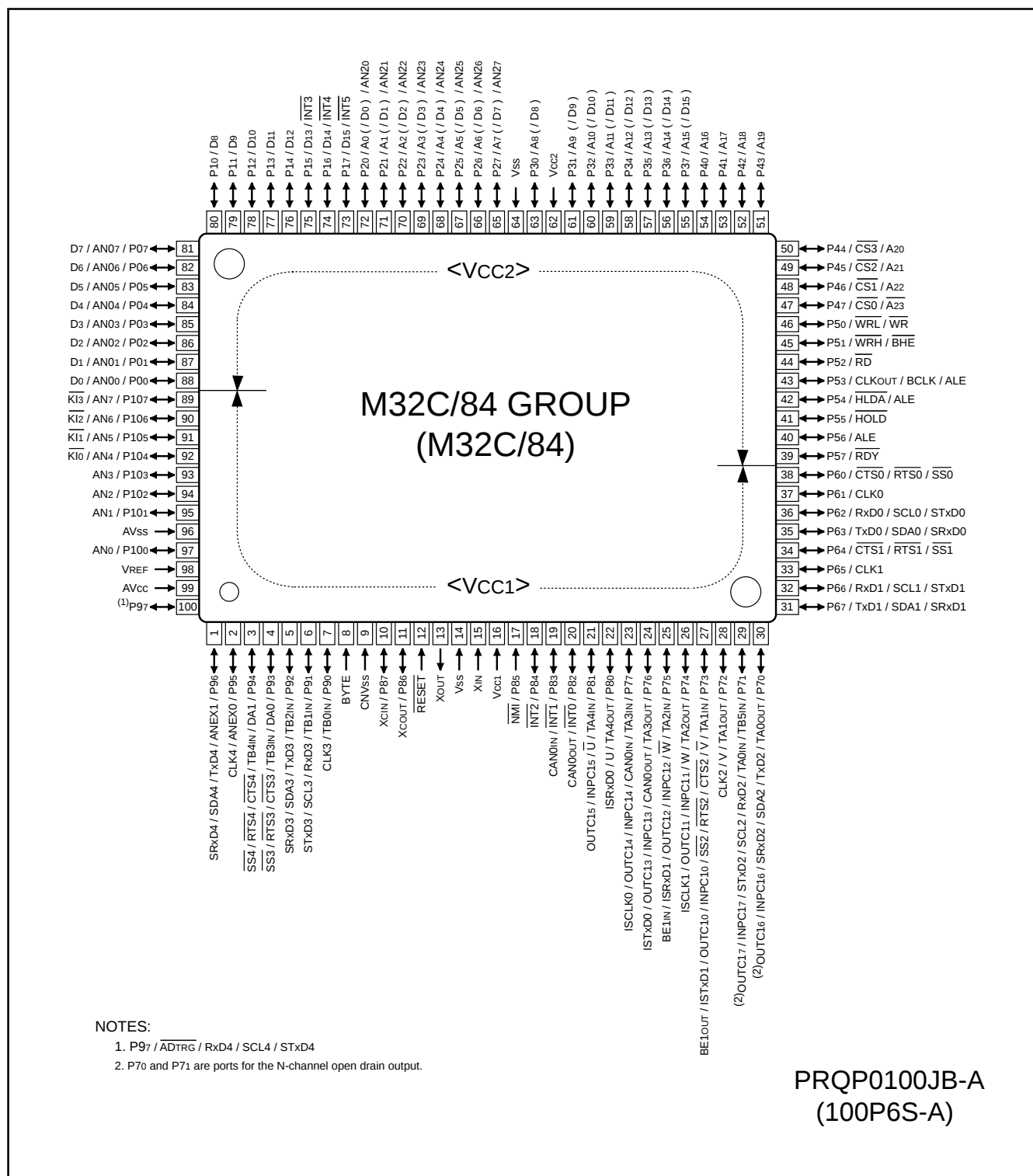


Figure 1.4 Pin Assignment for 100-Pin Package

Table 1.5 Pin Characteristics for 100-Pin Package (Continued)

Package Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
FP	GP								
51	49		P43						A19
52	50		P42						A18
53	51		P41						A17
54	52		P40						A16
55	53		P37						A15(/D15)
56	54		P36						A14(/D14)
57	55		P35						A13(/D13)
58	56		P34						A12(/D12)
59	57		P33						A11(/D11)
60	58		P32						A10(/D10)
61	59		P31						A9(/D9)
62	60	Vcc2							
63	61		P30						A8(/D8)
64	62	Vss							
65	63		P27					AN27	A7(/D7)
66	64		P26					AN26	A6(/D6)
67	65		P25					AN25	A5(/D5)
68	66		P24					AN24	A4(/D4)
69	67		P23					AN23	A3(/D3)
70	68		P22					AN22	A2(/D2)
71	69		P21					AN21	A1(/D1)
72	70		P20					AN20	A0(/D0)
73	71		P17	INT5					D15
74	72		P16	INT4					D14
75	73		P15	INT3					D13
76	74		P14						D12
77	75		P13						D11
78	76		P12						D10
79	77		P11						D9
80	78		P10						D8
81	79		P07					AN07	D7
82	80		P06					AN06	D6
83	81		P05					AN05	D5
84	82		P04					AN04	D4
85	83		P03					AN03	D3
86	84		P02					AN02	D2
87	85		P01					AN01	D1
88	86		P00					AN00	D0
89	87		P107	KI3				AN7	
90	88		P106	KI2				AN6	
91	89		P105	KI1				AN5	
92	90		P104	KI0				AN4	
93	91		P103					AN3	
94	92		P102					AN2	
95	93		P101					AN1	
96	94	AVss							
97	95		P100					AN0	
98	96	VREF							
99	97	AVcc							
100	98		P97			RxD4/SCL4/STxD4		ADTRG	

NOTES:

1. Bus control pins in M32C/84T cannot be used.

Address	Register	Symbol	Value after RESET
0090 ₁₆	UART0 Transmit /NACK Interrupt Control Register	S0TIC	XXXX X000 ₂
0091 ₁₆	UART1/UART4 Bus Conflict Detect Interrupt Control Register	BCN1IC/BCN4IC	XXXX X000 ₂
0092 ₁₆	UART1 Transmit/NACK Interrupt Control Register	S1TIC	XXXX X000 ₂
0093 ₁₆	Key Input Interrupt Control Register	KUPIC	XXXX X000 ₂
0094 ₁₆	Timer B0 Interrupt Control Register	TB0IC	XXXX X000 ₂
0095 ₁₆	Intelligent I/O Interrupt Control Register 1	IIO1IC	XXXX X000 ₂
0096 ₁₆	Timer B2 Interrupt Control Register	TB2IC	XXXX X000 ₂
0097 ₁₆	Intelligent I/O Interrupt Control Register 3	IIO3IC	XXXX X000 ₂
0098 ₁₆	Timer B4 Interrupt Control Register	TB4IC	XXXX X000 ₂
0099 ₁₆			
009A ₁₆	INT4 Interrupt Control Register	INT4IC	XX00 X000 ₂
009B ₁₆			
009C ₁₆	INT2 Interrupt Control Register	INT2IC	XX00 X000 ₂
009D ₁₆	Intelligent I/O Interrupt Control Register 9/ CAN Interrupt 0 Control Register	IIO9IC CAN0IC	XXXX X000 ₂
009E ₁₆	INT0 Interrupt Control Register	INT0IC	XX00 X000 ₂
009F ₁₆	Exit Priority Control Register	RLVL	XXXX 0000 ₂
00A0 ₁₆	Interrupt Request Register 0	IIO0IR	0000 000X ₂
00A1 ₁₆	Interrupt Request Register 1	IIO1IR	0000 000X ₂
00A2 ₁₆	Interrupt Request Register 2	IIO2IR	0000 000X ₂
00A3 ₁₆	Interrupt Request Register 3	IIO3IR	0000 000X ₂
00A4 ₁₆	Interrupt Request Register 4	IIO4IR	0000 000X ₂
00A5 ₁₆			
00A6 ₁₆			
00A7 ₁₆			
00A8 ₁₆	Interrupt Request Register 8	IIO8IR	0000 000X ₂
00A9 ₁₆	Interrupt Request Register 9	IIO9IR	0000 000X ₂
00AA ₁₆	Interrupt Request Register 10	IIO10IR	0000 000X ₂
00AB ₁₆	Interrupt Request Register 11	IIO11IR	0000 000X ₂
00AC ₁₆			
00AD ₁₆			
00AE ₁₆			
00AF ₁₆			
00B0 ₁₆	Interrupt Enable Register 0	IIO0IE	00 ₁₆
00B1 ₁₆	Interrupt Enable Register 1	IIO1IE	00 ₁₆
00B2 ₁₆	Interrupt Enable Register 2	IIO2IE	00 ₁₆
00B3 ₁₆	Interrupt Enable Register 3	IIO3IE	00 ₁₆
00B4 ₁₆	Interrupt Enable Register 4	IIO4IE	00 ₁₆
00B5 ₁₆			
00B6 ₁₆			
00B7 ₁₆			
00B8 ₁₆	Interrupt Enable Register 8	IIO8IE	00 ₁₆
00B9 ₁₆	Interrupt Enable Register 9	IIO9IE	00 ₁₆
00BA ₁₆	Interrupt Enable Register 10	IIO10IE	00 ₁₆
00BB ₁₆	Interrupt Enable Register 11	IIO11IE	00 ₁₆
00BC ₁₆			
00BD ₁₆			
00BE ₁₆			
00BF ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00C0 ₁₆			
00C1 ₁₆			
00C2 ₁₆			
00C3 ₁₆			
00C4 ₁₆			
00C5 ₁₆			
00C6 ₁₆			
00C7 ₁₆			
00C8 ₁₆			
00C9 ₁₆			
00CA ₁₆			
00CB ₁₆			
00CC ₁₆			
00CD ₁₆			
00CE ₁₆			
00CF ₁₆			
00D0 ₁₆			
00D1 ₁₆			
00D2 ₁₆			
00D3 ₁₆			
00D4 ₁₆			
00D5 ₁₆			
00D6 ₁₆			
00D7 ₁₆			
00D8 ₁₆			
00D9 ₁₆			
00DA ₁₆			
00DB ₁₆			
00DC ₁₆			
00DD ₁₆			
00DE ₁₆			
00DF ₁₆			
00E0 ₁₆			
00E1 ₁₆			
00E2 ₁₆			
00E3 ₁₆			
00E4 ₁₆			
00E5 ₁₆			
00E6 ₁₆			
00E7 ₁₆			
00E8 ₁₆ 00E9 ₁₆	SI/O Receive Buffer Register 0	G0RB	XXXX XXXX ₂ X000 XXXX ₂
00EA ₁₆ 00EB ₁₆	Transmit Buffer/Receive Data Register 0	G0TB/G0DR	XX ₁₆
00EC ₁₆	Receive Input Register 0	G0RI	XX ₁₆
00ED ₁₆	SI/O Communication Mode Register 0	G0MR	00 ₁₆
00EE ₁₆	Transmit Output Register 0	G0TO	XX ₁₆
00EF ₁₆	SI/O Communication Control Register 0	G0CR	0000 X011 ₂

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
01E0 ₁₆	CAN0 Message Slot Buffer 0 Standard ID0	C0SLOT0_0	XX ₁₆
01E1 ₁₆	CAN0 Message Slot Buffer 0 Standard ID1	C0SLOT0_1	XX ₁₆
01E2 ₁₆	CAN0 Message Slot Buffer 0 Extended ID0	C0SLOT0_2	XX ₁₆
01E3 ₁₆	CAN0 Message Slot Buffer 0 Extended ID1	C0SLOT0_3	XX ₁₆
01E4 ₁₆	CAN0 Message Slot Buffer 0 Extended ID2	C0SLOT0_4	XX ₁₆
01E5 ₁₆	CAN0 Message Slot Buffer 0 Data Length Code	C0SLOT0_5	XX ₁₆
01E6 ₁₆	CAN0 Message Slot Buffer 0 Data 0	C0SLOT0_6	XX ₁₆
01E7 ₁₆	CAN0 Message Slot Buffer 0 Data 1	C0SLOT0_7	XX ₁₆
01E8 ₁₆	CAN0 Message Slot Buffer 0 Data 2	C0SLOT0_8	XX ₁₆
01E9 ₁₆	CAN0 Message Slot Buffer 0 Data 3	C0SLOT0_9	XX ₁₆
01EA ₁₆	CAN0 Message Slot Buffer 0 Data 4	C0SLOT0_10	XX ₁₆
01EB ₁₆	CAN0 Message Slot Buffer 0 Data 5	C0SLOT0_11	XX ₁₆
01EC ₁₆	CAN0 Message Slot Buffer 0 Data 6	C0SLOT0_12	XX ₁₆
01ED ₁₆	CAN0 Message Slot Buffer 0 Data 7	C0SLOT0_13	XX ₁₆
01EE ₁₆	CAN0 Message Slot Buffer 0 Time Stamp High-Order	C0SLOT0_14	XX ₁₆
01EF ₁₆	CAN0 Message Slot Buffer 0 Time Stamp Low-Order	C0SLOT0_15	XX ₁₆
01F0 ₁₆	CAN0 Message Slot Buffer 1 Standard ID0	C0SLOT1_0	XX ₁₆
01F1 ₁₆	CAN0 Message Slot Buffer 1 Standard ID1	C0SLOT1_1	XX ₁₆
01F2 ₁₆	CAN0 Message Slot Buffer 1 Extended ID0	C0SLOT1_2	XX ₁₆
01F3 ₁₆	CAN0 Message Slot Buffer 1 Extended ID1	C0SLOT1_3	XX ₁₆
01F4 ₁₆	CAN0 Message Slot Buffer 1 Extended ID2	C0SLOT1_4	XX ₁₆
01F5 ₁₆	CAN0 Message Slot Buffer 1 Data Length Code	C0SLOT1_5	XX ₁₆
01F6 ₁₆	CAN0 Message Slot Buffer 1 Data 0	C0SLOT1_6	XX ₁₆
01F7 ₁₆	CAN0 Message Slot Buffer 1 Data 1	C0SLOT1_7	XX ₁₆
01F8 ₁₆	CAN0 Message Slot Buffer 1 Data 2	C0SLOT1_8	XX ₁₆
01F9 ₁₆	CAN0 Message Slot Buffer 1 Data 3	C0SLOT1_9	XX ₁₆
01FA ₁₆	CAN0 Message Slot Buffer 1 Data 4	C0SLOT1_10	XX ₁₆
01FB ₁₆	CAN0 Message Slot Buffer 1 Data 5	C0SLOT1_11	XX ₁₆
01FC ₁₆	CAN0 Message Slot Buffer 1 Data 6	C0SLOT1_12	XX ₁₆
01FD ₁₆	CAN0 Message Slot Buffer 1 Data 7	C0SLOT1_13	XX ₁₆
01FE ₁₆	CAN0 Message Slot Buffer 1 Time Stamp High-Order	C0SLOT1_14	XX ₁₆
01FF ₁₆	CAN0 Message Slot Buffer 1 Time Stamp Low-Order	C0SLOT1_15	XX ₁₆
0200 ₁₆ 0201 ₁₆	CAN0 Control Register 0	C0CTRL0	XX01 0X01 ₂ ⁽¹⁾ XXXX 0000 ₂ ⁽¹⁾
0202 ₁₆ 0203 ₁₆	CAN0 Status Register	C0STR	0000 0000 ₂ ⁽¹⁾ X000 0X01 ₂ ⁽¹⁾
0204 ₁₆ 0205 ₁₆	CAN0 Extended ID Register	C0IDR	00 ₁₆ ⁽¹⁾ 00 ₁₆ ⁽¹⁾
0206 ₁₆ 0207 ₁₆	CAN0 Configuration Register	C0CONR	0000 XXXX ₂ ⁽¹⁾ 0000 0000 ₂ ⁽¹⁾
0208 ₁₆ 0209 ₁₆	CAN0 Time Stamp Register	C0TSR	00 ₁₆ ⁽¹⁾ 00 ₁₆ ⁽¹⁾
020A ₁₆	CAN0 Transmit Error Count Register	C0TEC	00 ₁₆ ⁽¹⁾
020B ₁₆	CAN0 Receive Error Count Register	C0REC	00 ₁₆ ⁽¹⁾
020C ₁₆ 020D ₁₆	CAN0 Slot Interrupt Status Register	C0SISTR	00 ₁₆ ⁽¹⁾ 00 ₁₆ ⁽¹⁾
020E ₁₆			
020F ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and supplying the clock to the CAN module.

Address	Register	Symbol	Value after RESET
0210 ₁₆	CAN0 Slot Interrupt Mask Register	C0SIMKR	00 ₁₆ ⁽²⁾
0211 ₁₆			00 ₁₆ ⁽²⁾
0212 ₁₆			
0213 ₁₆			
0214 ₁₆	CAN0 Error Interrupt Mask Register	C0EIMKR	XXXX X000 ₂ ⁽²⁾
0215 ₁₆	CAN0 Error Interrupt Status Register	C0EISTR	XXXX X000 ₂ ⁽²⁾
0216 ₁₆	CAN0 Error Cause Register	C0EFR	00 ₁₆ ⁽²⁾
0217 ₁₆	CAN0 Baud Rate Prescaler	C0BRP	0000 0001 ₂ ⁽²⁾
0218 ₁₆			
0219 ₁₆	CAN0 Mode Register	C0MDR	XXXX XX00 ₂ ⁽²⁾
021A ₁₆			
021B ₁₆			
021C ₁₆			
021D ₁₆			
021E ₁₆			
021F ₁₆			
0220 ₁₆	CAN0 Single-Shot Control Register	C0SSCTLR	00 ₁₆ ⁽²⁾
0221 ₁₆			00 ₁₆ ⁽²⁾
0222 ₁₆			
0223 ₁₆			
0224 ₁₆	CAN0 Single-Shot Status Register	C0SSSTR	00 ₁₆ ⁽²⁾
0225 ₁₆			00 ₁₆ ⁽²⁾
0226 ₁₆			
0227 ₁₆			
0228 ₁₆	CAN0 Global Mask Register Standard ID0	C0GMR0	XXX0 0000 ₂ ⁽²⁾
0229 ₁₆	CAN0 Global Mask Register Standard ID1	C0GMR1	XX00 0000 ₂ ⁽²⁾
022A ₁₆	CAN0 Global Mask Register Extended ID0	C0GMR2	XXXX 0000 ₂ ⁽²⁾
022B ₁₆	CAN0 Global Mask Register Extended ID1	C0GMR3	00 ₁₆ ⁽²⁾
022C ₁₆	CAN0 Global Mask Register Extended ID2	C0GMR4	XX00 0000 ₂ ⁽²⁾
022D ₁₆			
022E ₁₆			
022F ₁₆			
0230 ₁₆	CAN0 Message Slot 0 Control Register / CAN0 Local Mask Register A Standard ID0	C0MCTL0/ C0LMAR0	0000 0000 ₂ ⁽²⁾ XXX0 0000 ₂ ⁽²⁾
0231 ₁₆	CAN0 Message Slot 1 Control Register / CAN0 Local Mask Register A Standard ID1	C0MCTL1/ C0LMAR1	0000 0000 ₂ ⁽²⁾ XX00 0000 ₂ ⁽²⁾
0232 ₁₆	CAN0 Message Slot 2 Control Register / CAN0 Local Mask Register A Extended ID0	C0MCTL2/ C0LMAR2	0000 0000 ₂ ⁽²⁾ XXXX 0000 ₂ ⁽²⁾
0233 ₁₆	CAN0 Message Slot 3 Control Register / CAN0 local Mask Register A Extended ID1	C0MCTL3/ C0LMAR3	00 ₁₆ ⁽²⁾ 00 ₁₆ ⁽²⁾
0234 ₁₆	CAN0 Message Slot 4 Control Register / CAN0 Local Mask Register A Extended ID2	C0MCTL4/ C0LMAR4	0000 0000 ₂ ⁽²⁾ XX00 0000 ₂ ⁽²⁾
0235 ₁₆	CAN0 Message Slot 5 Control Register	C0MCTL5	00 ₁₆ ⁽²⁾
0236 ₁₆	CAN0 Message Slot 6 Control Register	C0MCTL6	00 ₁₆ ⁽²⁾
0237 ₁₆	CAN0 Message Slot 7 Control Register	C0MCTL7	00 ₁₆ ⁽²⁾
0238 ₁₆	CAN0 Message Slot 8 Control Register / CAN0 Local Mask Register B Standard ID0	C0MCTL8/ C0LMBR0	0000 0000 ₂ ⁽²⁾ XXX0 0000 ₂ ⁽²⁾

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 0220₁₆ to 023F₁₆.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and supplying the clock to the CAN module.

Address	Register	Symbol	Value after RESET
0320 ₁₆			
0321 ₁₆			
0322 ₁₆			
0323 ₁₆			
0324 ₁₆	UART3 Special Mode Register 4	U3SMR4	00 ₁₆
0325 ₁₆	UART3 Special Mode Register 3	U3SMR3	00 ₁₆
0326 ₁₆	UART3 Special Mode Register 2	U3SMR2	00 ₁₆
0327 ₁₆	UART3 Special Mode Register	U3SMR	00 ₁₆
0328 ₁₆	UART3 Transmit/Receive Mode Register	U3MR	00 ₁₆
0329 ₁₆	UART3 Bit Rate Register	U3BRG	XX ₁₆
032A ₁₆	UART3 Transmit Buffer Register	U3TB	XX ₁₆
032B ₁₆			XX ₁₆
032C ₁₆	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000 ₂
032D ₁₆	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010 ₂
032E ₁₆	UART3 Receive Buffer Register	U3RB	XX ₁₆
032F ₁₆			XX ₁₆
0330 ₁₆			
0331 ₁₆			
0332 ₁₆			
0333 ₁₆			
0334 ₁₆	UART2 Special Mode Register 4	U2SMR4	00 ₁₆
0335 ₁₆	UART2 Special Mode Register 3	U2SMR3	00 ₁₆
0336 ₁₆	UART2 Special Mode Register 2	U2SMR2	00 ₁₆
0337 ₁₆	UART2 Special Mode Register	U2SMR	00 ₁₆
0338 ₁₆	UART2 Transmit/Receive Mode Register	U2MR	00 ₁₆
0339 ₁₆	UART2 Bit Rate Register	U2BRG	XX ₁₆
033A ₁₆	UART2 Transmit Buffer Register	U2TB	XX ₁₆
033B ₁₆			XX ₁₆
033C ₁₆	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000 ₂
033D ₁₆	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010 ₂
033E ₁₆	UART2 Receive Buffer Register	U2RB	XX ₁₆
033F ₁₆			XX ₁₆
0340 ₁₆	Count Start Flag	TABSR	00 ₁₆
0341 ₁₆	Clock Prescaler Reset Flag	CPSRF	0XXX XXXX ₂
0342 ₁₆	One-Shot Start Flag	ONSF	00 ₁₆
0343 ₁₆	Trigger Select Register	TRGSR	00 ₁₆
0344 ₁₆	Up/Down Flag	UDF	00 ₁₆
0345 ₁₆			
0346 ₁₆	Timer A0 Register	TA0	XX ₁₆
0347 ₁₆			XX ₁₆
0348 ₁₆	Timer A1 Register	TA1	XX ₁₆
0349 ₁₆			XX ₁₆
034A ₁₆	Timer A2 Register	TA2	XX ₁₆
034B ₁₆			XX ₁₆
034C ₁₆	Timer A3 Register	TA3	XX ₁₆
034D ₁₆			XX ₁₆
034E ₁₆	Timer A4 Register	TA4	XX ₁₆
034F ₁₆			XX ₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

$$V_{CC1}=V_{CC2}=5V$$

**Table 5.6 Flash Memory Version Electrical Characteristics (V_{CC1}=4.5 to 5.5V, 3.3 to 3.6V at
T_{opr}=0 to 60°C unless otherwise specified)**

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
-	Program and Erase Endurance ⁽²⁾		100			cycles
-	Word Program Time (V _{CC1} =5.0V, T _{opr} =25° C)			25	200	μs
-	Lock Bit Program Time			25	200	μs
-	Block Erase Time (V _{CC1} =5.0V, T _{opr} =25° C)	4-Kbyte Block		0.3	4	s
		8-Kbyte Block		0.3	4	s
		32-Kbyte Block		0.5	4	s
		64-Kbyte Block		0.8	4	s
-	All-Unlocked-Block Erase Time ⁽¹⁾				4 x <i>n</i>	s
t _{PS}	Wait Time to Stabilize Flash Memory Circuit				15	μs
-	Data Hold Time (T _{opr} =-40 to 85 ° C)		10			years

NOTES:

1. *n* denotes the number of block to be erased.

2. Number of program-erase cycles per block.

If Program and Erase Endurance is *n* cycle (*n*≠100), each block can be erased and programmed *n* cycles.
For example, if a 4-Kbyte block A is erased after programming a word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data can not be programmed to the same address more than once without erasing the block. (rewrite prohibited).

$$V_{CC1}=V_{CC2}=5V$$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr}=-20$ to $85^{\circ}C$ unless otherwise specified)

Table 5.9 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External Clock Input Cycle Time	31.25		ns
$t_{w(H)}$	External Clock Input High ("H") Width	13.75		ns
$t_{w(L)}$	External Clock Input Low ("L") Width	13.75		ns
t_r	External Clock Rise Time		5	ns
t_f	External Clock Fall Time		5	ns

Table 5.10 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data Input Access Time (RD standard)		(Note 1)	ns
$t_{ac1(AD-DB)}$	Data Input Access Time (AD standard, CS standard)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (RD standard, when accessing a space with the multiplexrd bus)		(Note 1)	ns
$t_{ac2(AD-DB)}$	Data Input Access Time (AD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{su(DB-BCLK)}$	Data Input Setup Time	26		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ Input Setup Time	26		ns
$t_{su(HOLD-BCLK)}$	$\overline{HOLD}$ Input Setup Time	30		ns
$t_{h(RD-DB)}$	Data Input Hold Time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ Input Hold Time	0		ns
$t_{h(BCLK-HOLD)}$	$\overline{HOLD}$ Input Hold Time	0		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ Output Delay Time		25	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles. Insert a wait state or lower the operation frequency, $f_{(BCLK)}$, if the calculated value is negative.

$$t_{ac1(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, m=(bx2)+1)$$

$$t_{ac1(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)}} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, n=a+b)$$

$$t_{ac2(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, m=(bx2)-1)$$

$$t_{ac2(AD-DB)} = \frac{10^9 \times p}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, p=\{(a+b-1) \times 2\}+1)$$

$$V_{CC1}=V_{CC2}=3.3V$$

Switching Characteristics

($V_{CC1}=V_{CC2}=3.0$ to $3.6V$, $V_{SS} = 0V$ at $T_{opr} = -20$ to $85^{\circ}C$ unless otherwise specified)

Table 5.40 Memory Expansion Mode and Microprocessor Mode
(when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 5.2		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard) ⁽³⁾		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard) ⁽³⁾		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-Select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-Select Signal Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-CS)}$	Chip-Select Signal Output Hold Time (RD standard) ⁽³⁾		0		ns
$t_{h(WR-CS)}$	Chip-Select Signal Output Hold Time (WR standard) ⁽³⁾		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-3		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		0		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 2)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard) ⁽³⁾		(Note 1)		ns
$t_{w(WR)}$	WR Output Width		(Note 2)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 20 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

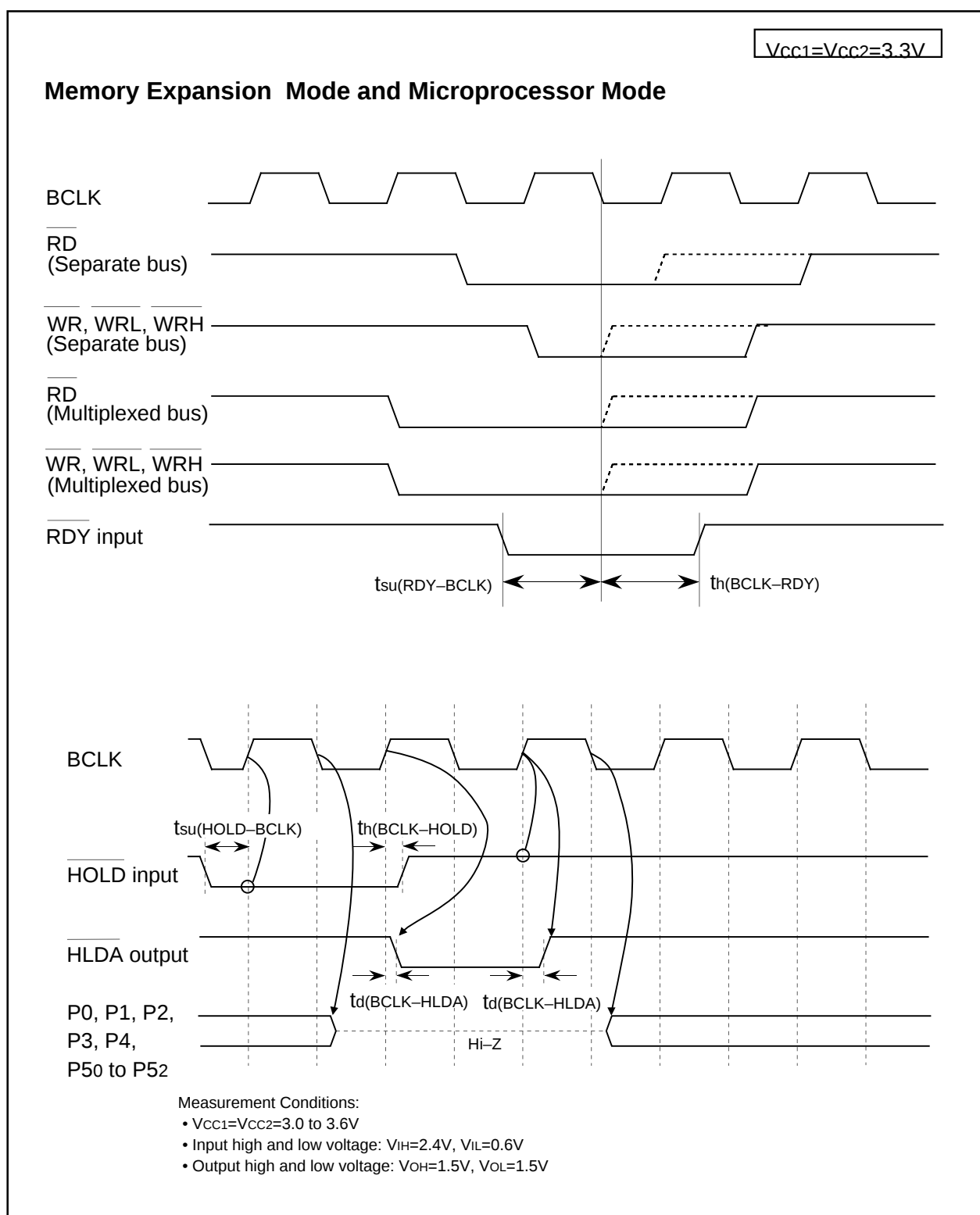
$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles.

$$t_{w(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, n=(b \times 2)-1)$$

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)}} - 20 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, m=b)$$

3. t_{cns} is added when recovery cycle is inserted.

Figure 5.10 $V_{CC1}=V_{CC2}=3.3V$ Timing Diagram (4)

5.2 Electrical Characteristics (M32C/84T)

Table 5.42 Absolute Maximum Ratings

Symbol	Parameter		Condition	Value	Unit
V _{CC1} , V _{CC2}	Supply Voltage		V _{CC1} =V _{CC2} =AV _{CC}	-0.3 to 6.0	V
AV _{CC}	Analog Supply Voltage		V _{CC1} =V _{CC2} =AV _{CC}	-0.3 to 6.0	V
V _I	Input Voltage	RESET, CNV _{SS} , BYTE, P60-P67, P72-P77, P80-P87, P90-P97, P100-P107, P140-P146, P150-P157 ⁽¹⁾ , V _{REF} , X _{IN}		-0.3 to V _{CC1} +0.3	V
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137 ⁽¹⁾		-0.3 to V _{CC2} +0.3	
		P70, P71		-0.3 to 6.0	
V _O	Output Voltage	P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P140-P146, P150-P157 ⁽¹⁾ , X _{OUT}		-0.3 to V _{CC1} +0.3	V
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137 ⁽¹⁾		-0.3 to V _{CC2} +0.3	
		P70, P71		-0.3 to 6.0	
P _d	Power Dissipation		T _{opr} =25° C	500	mW
T _{opr}	Operating Ambient Temperature	during CPU operation	T version	-40 to 85	° C
		during flash memory program and erase operation		0 to 60	
T _{stg}	Storage Temperature			-65 to 150	° C

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

$$V_{CC1}=V_{CC2}=5V$$

Table 5.44 Electrical Characteristics

($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr} = -40$ to $85^{\circ}C$ (T version),
 $f(BCLK)=32MHz$ unless otherwise specified)

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V _{OH}	Output High ("H") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137	I _{OH} =-5mA	V _{CC2} -2.0		V _{CC2}	V
		P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P140-P146, P150-P157 ⁽¹⁾	I _{OH} =-5mA	V _{CC1} -2.0		V _{CC1}	
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137	I _{OH} =-200μA	V _{CC2} -0.3		V _{CC2}	V
		P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P140-P146, P150-P157 ⁽¹⁾	I _{OH} =-200μA	V _{CC1} -0.3		V _{CC1}	
		X _{OUT}	I _{OH} =-1mA	3.0			V
		X _{COUT}	High Power	No load applied	2.5		V
			Low Power	No load applied	1.6		
V _{OL}	Output Low ("L") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OL} =5mA			2.0	V
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OL} =200μA			0.45	V
		X _{OUT}	I _{OL} =1mA			2.0	V
		X _{COUT}	High Power	No load applied	0		V
			Low Power	No load applied	0		
V _{T+} -V _{T-}	Hysteresis	HOLD, RDY, TA0IN-TA4IN, TB0IN-TB5IN, INT0-INT5, ADTRG, CTS0-CTS4, CLK0-CLK4, TA0OUT-TA4OUT, NMI, K10-K13, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		RESET		0.2		1.8	V
I _{IH}	Input High ("H") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾ , X _{IN} , RESET, CNVSS, BYTE	V _I =5V			5.0	μA
I _{IL}	Input Low ("L") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾ , X _{IN} , RESET, CNVSS, BYTE	V _I =0V			-5.0	μA
R _{PULLUP}	Pull-up Resistance	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	V _I =0V Flash Memory	30	50	167	kΩ
R _{fXIN}	Feedback Resistance	X _{IN}			1.5		MΩ
R _{fXCIN}	Feedback Resistance	X _{CIN}			10		MΩ
V _{RAM}	RAM Standby Voltage	In stop mode		2.0			V

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

$$V_{CC1}=V_{CC2}=5V$$

Table 5.45 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr}= -40$ to $85^{\circ}C$ (T version), $f(BCLK)=32MHz$ unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution	$V_{REF}=V_{CC1}$			10	Bits
INL	Integral Nonlinearity Error	$V_{REF}=V_{CC1}=V_{CC2}=5V$			± 3	LSB
						LSB
		External op-amp connection mode			± 7	LSB
DNL	Differential Nonlinearity Error				± 1	LSB
-	Offset Error				± 3	LSB
-	Gain Error				± 3	LSB
RLADDER	Resistor Ladder	$V_{REF}=V_{CC1}$	8		40	k Ω
t _{CONV}	10-bit Conversion Time ^(1, 2)		2.06			μs
t _{CONV}	8-bit Conversion Time ^(1, 2)		1.75			μs
t _{SAMP}	Sampling Time ⁽¹⁾		0.188			μs
V _{REF}	Reference Voltage		2		V_{CC1}	V
V _{IA}	Analog Input Voltage		0		V_{REF}	V

NOTES:

1. Divide $f(X_{IN})$, if exceeding 16 MHz, to keep ϕ_{AD} frequency at 16 MHz or less.
2. With using the sample and hold function.

Table 5.46 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr}= -40$ to $85^{\circ}C$ (T version), $f(BCLK)=32MHz$ unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t _{SU}	Setup Time				3	μs
R _O	Output Resistance		4	10	20	k Ω
I _{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTES:

1. Measurement when using one D/A converter. The DA_i register (i=0, 1) of the D/A converter, not being used, is set to "00₁₆". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

$$V_{CC1}=V_{CC2}=5V$$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr}= -40$ to $85^{\circ}C$ (T version) unless otherwise specified)

Table 5.50 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	100		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	40		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	40		ns

Table 5.51 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	400		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	200		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	200		ns

Table 5.52 Timer A Input (External Trigger Input in One-Shot Timer Mode)

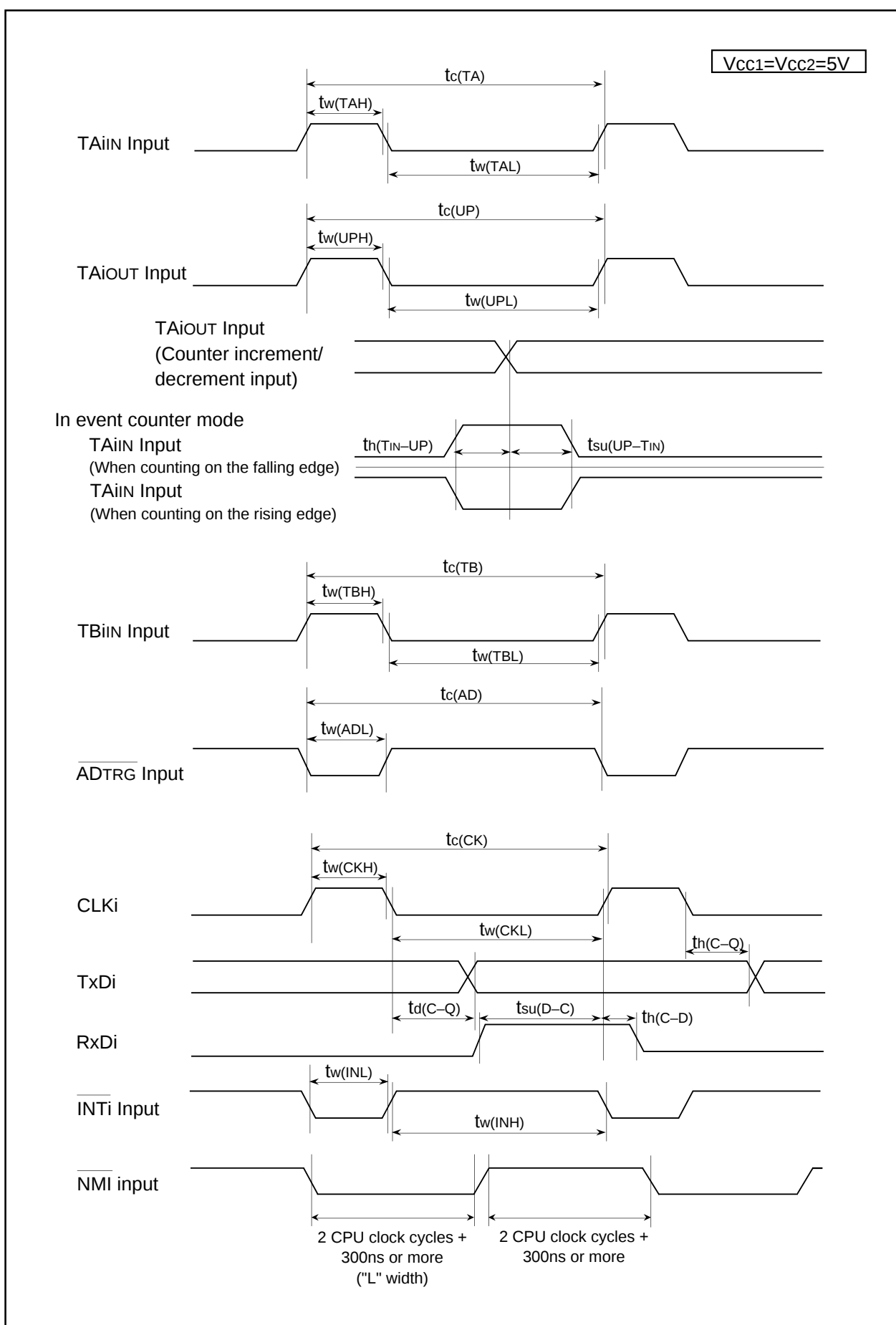
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	200		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 5.53 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 5.54 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAiOUT Input High ("H") Width	1000		ns
$t_{w(UPL)}$	TAiOUT Input Low ("L") Width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAiOUT Input Hold Time	400		ns

Figure 5.13 $V_{CC1}=V_{CC2}=5V$ Timing Diagram

REVISION HISTORY	M32C/84 Group (M32C/84, M32C/84T) Datasheet
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Rev.	Date	Description	
		Page	Summary
0.40	Sep. 30, 2003	—	New Document
0.50	Feb. 05, 2004	2, 3	Overview • Table 1.1 and Table 1.2 M32C/84 Group Performance Values for Shortest Instruction Execution Time and Power Consumption” modified
		5	• Figure 1.2 ROM/RAM Capacity Products added
		6	• Table 1.3 M32C/84 Group Products added
		6	• Figure 1.3 Product Numbering System 128-Kbytes added to ROM capacity Memory
0.50	Feb. 05, 2004	23	• Figure 3.1 Memory Map Diagram modified; products added
		24	SFR • “Values after RESET” for the PM1, PM2, D4INT, G0IRF, G1IRF, IDB0 to IDB1, TA0MR to TA4MR, TCSPR, DM0SL to DM3SL registers revised • The IPSA register added to address 0179 ₁₆ • NOTES added to the PM0 and TCSPR register
		44	Electrical Characteristics • Newly added
0.51	Feb. 09, 2004		Electrical Characteristics
		50	• Table 5.6 Flash Memory Version Electrical Characteristics Note 4 revised
		57	• Figure 5.2 Vcc1=Vcc2=5V Timing Diagram (1) Notes 1 and 2 revised
		68	• Figure 5.3 Vcc1=Vcc2=5V Timing Diagram (2) Notes 1, 2, and 3 revised
		68	• Figure 5.6 Vcc1=Vcc2=3.3V Timing Diagram (1) Notes 1, 2, and 3 revised
0.51	Feb. 09, 2004	69	• Figure 5.7 Vcc1=Vcc2=3.3V Timing Diagram (2) Notes 1 and 2 revised
0.52	Mar.12, 2004		Overview
		2, 3	• Table 1.1 and 1.2 M32C/84 Group Performance Values for Power Consumption modified
		48	Electrical Characteristics • Table 5.3 Electrical Characteristics Maximum values for Power Supply Current modified
		50	• Table 5.6 Flash Memory Version Electrical Characteristics Note 1. 100-cycle Products (D3, D5, U3, U5) deleted; Note 4 modified
0.52	Mar.12, 2004		• Table 5.7 Flash Memory Version Program and Erase Voltage and Read Operation Voltage Characteristics (at Topr=0 to 60°C) deleted
		61	• Table 5.22 Electrical Characteristics Maximum values for Power Supply Consumption modified and standard values when “Topr=85°C while clock is stopped” deleted

REVISION HISTORY	M32C/84 Group (M32C/84, M32C/84T) Datasheet
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Rev.	Date	Description	
		Page	Summary
1.00	Jun.01, 2004	-	M32C/84T (High-reliability version) added
		All Pages	Words standardized: On-chip oscillator, A/D converter and D/A converter
			Overview
		1	• 1.1 Applications Automobiles added
		2, 3	• Table 1.1 and Table 1.2 M32C/84 Group (M32C/84, M32C/84T) Performance M32C/84T added; note 3 added
		4	• Figure 1.1 M32C/84 Group (M32C/84, M32C/84T) Block Diagram Note 3 added
		5	• 1.4 Product Information Description modified
		6	• Figure 1.2 ROM/RAM Capacity figure modified
		6	• Table 1.3 M32C/84 Group M32C/84T added
		6	• Figure 1.3 Product Numbering System M32C/84T added
		7	• Figure 1.4 Pin Assignment for 144-Pin Package Note 3 added
		12	• Figure 1.6 Pin Assignment for 100-Pin Package Note 5 added
		8 to 10	• Table 1.5 Pin Characteristics for 144-Pin Package Note 1 added
		13, 14	• Table 1.6 Pin Characteristics for 100-Pin Package Note 1 added
		15 to 18	• Table 1.7 Pin Description Notes added
			Memory
		22	• Figure 3.1 Memory Map Tables of internal ROM/internal RAM modified; note 2 modified; notes 4 and 5 added
			SFR
		23	• Note 2 added
		24	• PWCR0 and PWCR1 registers deleted
			• “Values after RESET” of the masked ROM version added to the FMR0 register
			• Note 1 added
			Electrical Characteristics
		44	• Table 5.2 Recommended Operating Conditions f_{ripple} , $V_{p-p(\text{ripple})}$, V_{CC} , SV_{CC} and note 1 deleted
		47	• Table 5.3 Electrical Characteristics R_{PULLUP} value for the masked ROM version added
		48	• Table 5.4 A/D Conversion Characteristics t_{SMP} value modified; note 1 added
		50	• Table 5.7 Low Voltage Detect Circuit Electrical Characteristics added
			• Table 5.8 Power Supply Timing added
			• Figure 5.1 Power Supply Timing Diagram added
		55	• Table 5.23 Memory Expansion Mode and Microprocessor Mode $t_{h(BCLK-ALE)}$ value modified
		61	• Table 5.24 Electrical Characteristics R_{PULLUP} value for the masked ROM version added
		62	• Table 5.25 A/D Conversion Characteristics t_{CONV} value modified

