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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	85
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30843fhfp-u3

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Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Classsfication	Symbol	I/O Type	Supply Voltage	Function
Main Clock Input	XIN	I	VCC1	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, apply it to XIN and leave XOUT open
Main Clock Output	XOUT	O	VCC1	
Sub Clock Input	XCIN	I	VCC1	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT. To apply external clock, apply it to XCIN and leave XCOUT open
Sub Clock Output	XCOUT	O	VCC1	
BCLK Output(1)	BCLK	O	VCC2	Outputs BCLK signal
Clock Output	CLKOUT	O	VCC2	Outputs the clock having the same frequency as fC, f8 or f32
$\overline{INT}$ Interrupt Input	$\overline{INT0}$ to $\overline{INT2}$	I	VCC1	Input pins for the $\overline{INT}$ interrupt
	$\overline{INT3}$ to $\overline{INT5}$	I	VCC2	
$\overline{NMI}$ Interrupt Input	$\overline{NMI}$	I	VCC1	Input pin for the $\overline{NMI}$ interrupt
Key Input Interrupt	$\overline{KI0}$ to $\overline{KI3}$	I	VCC1	Input pins for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	VCC1	I/O pins for the timer A0 to A4 (TA0OUT is a pin for the N-channel open drain output.)
	TA0IN to TA4IN	I	VCC1	Input pins for the timer A0 to A4
Timer B	TB0IN to TB5IN	I	VCC1	Input pins for the timer B0 to B5
Three-phase Motor Control Timer Output	U, $\overline{U}$, V, $\overline{V}$, W, $\overline{W}$	O	VCC1	Output pins for the three-phase motor control timer
Serial I/O	$\overline{CTS0}$ to $\overline{CTS4}$	I	VCC1	Iutput pins for data transmission control
	$\overline{RTS0}$ to $\overline{RTS4}$	O	VCC1	Output pins for data reception control
	CLK0 to CLK4	I/O	VCC1	Inputs and outputs the transfer clock
	RxD0 to RxD4	I	VCC1	Inputs serial data
	TxD0 to TxD4	O	VCC1	Outputs serial data (TxD2 is a pin for the N-channel open drain output.)
I^2C Mode	SDA0 to SDA4	I/O	VCC1	Inputs and outputs serial data (SDA2 is a pin for the N-channel open drain output.)
	SCL0 to SCL4	I/O	VCC1	Inputs and outputs the transfer clock (SCL2 is a pin for the N-channel open drain output.)
Serial I/O Special Function	STxD0 to STxD4	O	VCC1	Outputs serial data when slave mode is selected (STxD2 is a pin for the N-channel open drain output.)
	SRxD0 to SRxD4	I	VCC1	Inputs serial data when slave mode is selected
	$\overline{SS0}$ to $\overline{SS4}$	I	VCC1	Input pins to control serial I/O special function

I : Input O : Output I/O : Input and output

NOTES:

1. Bus control pins in M32C/84T cannot be used.

Table 1.6 Pin Description (144-Pin Package only) (Continued)

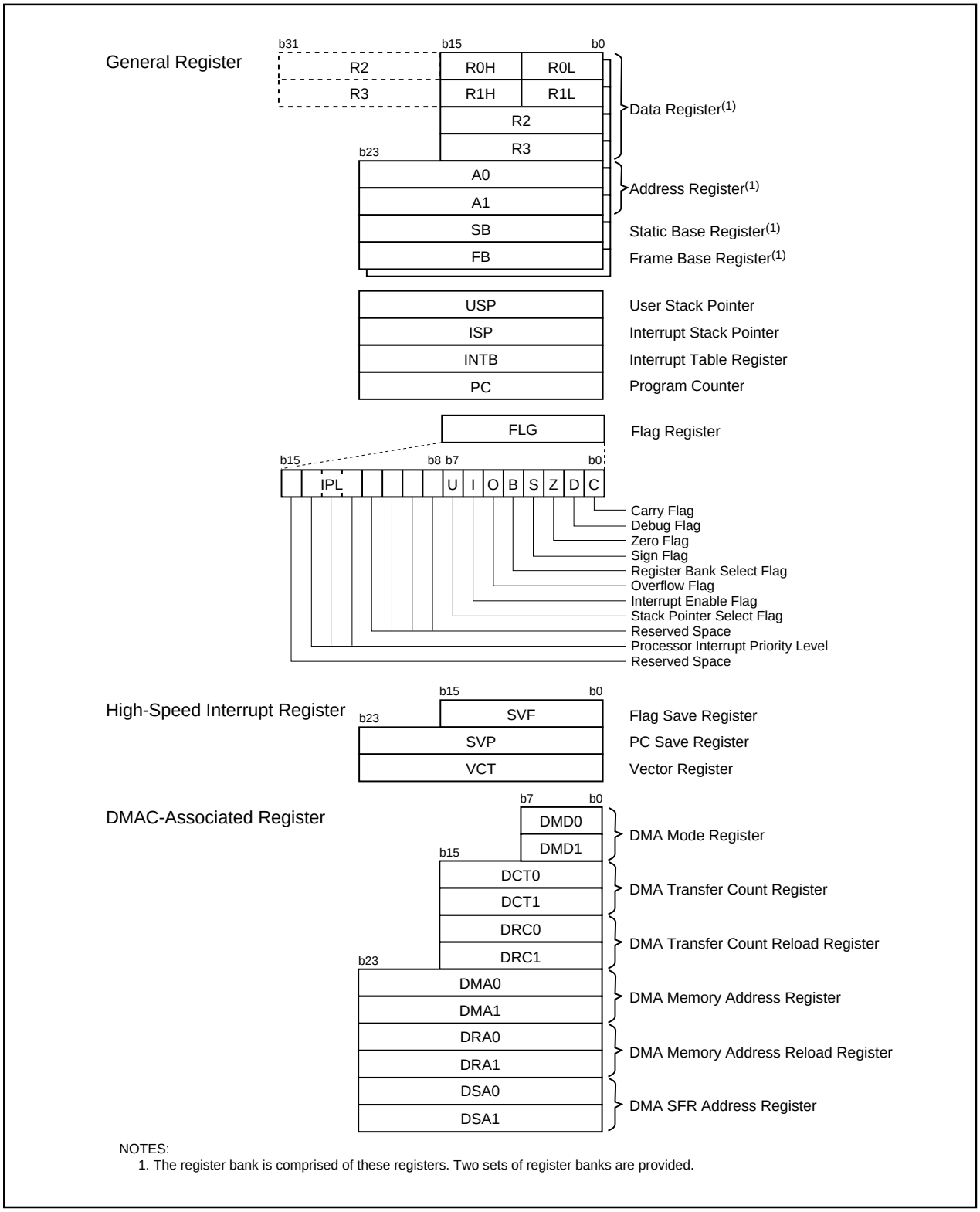
Classsfication	Symbol	I/O Type	Supply Voltage	Function
A/D Converter	$AN15_0$ to $AN15_7$	I	V_{CC1}	Analog input pins for the A/D converter
I/O Ports	$P11_0$ to $P11_4$ $P12_0$ to $P12_7$ $P13_0$ to $P13_7$	I/O	V_{CC2}	I/O ports having equivalent functions to P0
	$P14_0$ to $P14_6$ $P15_0$ to $P15_7$	I/O	V_{CC1}	I/O ports having equivalent functions to P0

I : Input O : Output I/O : Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.

The register bank is comprised of 8 registers (R0, R1, R2, R3, A0, A1, SB and FB) out of 28 CPU registers. Two sets of register banks are provided.



NOTES:
1. The register bank is comprised of these registers. Two sets of register banks are provided.

Figure 2.1 CPU Register

2.1 General Registers

2.1.1 Data Registers (R0, R1, R2 and R3)

R0, R1, R2 and R3 are 16-bit registers for transfer, arithmetic and logic operations. R0 and R1 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R0 can be combined with R2 to be used as a 32-bit data register (R2R0). The same applies to R1 and R3.

2.1.2 Address Registers (A0 and A1)

A0 and A1 are 24-bit registers for A0-/A1-indirect addressing, A0-/A1-relative addressing, transfer, arithmetic and logic operations.

2.1.3 Static Base Register (SB)

SB is a 24-bit register for SB-relative addressing.

2.1.4 Frame Base Register (FB)

FB is a 24-bit register for FB-relative addressing.

2.1.5 Program Counter (PC)

PC, 24 bits wide, indicates the address of an instruction to be executed.

2.1.6 Interrupt Table Register (INTB)

INTB is a 24-bit register indicating the starting address of an relocatable interrupt vector table.

2.1.7 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are 24 bits wide each. The U flag is used to switch between USP and ISP. Refer to **2.1.8 Flag Register (FLG)** for details on the U flag. Set USP and ISP to even addresses to execute an interrupt sequence efficiently.

2.1.8 Flag Register (FLG)

FLG is a 16-bit register indicating a CPU state.

2.1.8.1 Carry Flag (C)

The C flag indicates whether carry or borrow has occurred after executing an instruction.

2.1.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

2.1.8.3 Zero Flag (Z)

The Z flag is set to "1" when the value of zero is obtained from an arithmetic operation; otherwise "0".

2.1.8.4 Sign Flag (S)

The S flag is set to "1" when a negative value is obtained from an arithmetic operation; otherwise "0".

4. Special Function Registers (SFR)

Address	Register	Symbol	Value after RESET
000016			
000116			
000216			
000316			
000416	Processor Mode Register 0(1)	PM0	1000 00002(CNVss pin ="L") 0000 00112(CNVss pin ="H")
000516	Processor Mode Register 1	PM1	0016
000616	System Clock Control Register 0	CM0	0000 10002
000716	System Clock Control Register 1	CM1	0010 00002
000816			
000916	Address Match Interrupt Enable Register	AIER	0016
000A16	Protect Register	PRCR	XXXX 00002
000B16	External Data Bus Width Control Register(2)	DS	XXXX 10002(BYTE pin ="L") XXXX 00002(BYTE pin ="H")
000C16	Main Clock Division Register	MCD	XXX0 10002
000D16	Oscillation Stop Detection Register	CM2	0016
000E16	Watchdog Timer Start Register	WDTS	XX16
000F16	Watchdog Timer Control Register	WDC	000X XXXX2
001016 001116 001216	Address Match Interrupt Register 0	RMAD0	00000016
001316	Processor Mode Register 2	PM2	0016
001416 001516 001616	Address Match Interrupt Register 1	RMAD1	00000016
001716	Voltage Detection Register 2(2)	VCR2	0016
001816 001916 001A16	Address Match Interrupt Register 2	RMAD2	00000016
001B16	Voltage Detection Register 1(2)	VCR1	0000 10002
001C16 001D16 001E16	Address Match Interrupt Register 3	RMAD3	00000016
001F16			
002016			
002116			
002216			
002316			
002416			
002516			
002616	PLL Control Register 0	PLC0	0001 X0102
002716	PLL Control Register 1	PLC1	000X 00002
002816 002916 002A16	Address Match Interrupt Register 4	RMAD4	00000016
002B16			
002C16 002D16 002E16	Address Match Interrupt Register 5	RMAD5	00000016
002F16	Voltage Down Detection Interrupt Register(2)	D4INT	0016

X: Indeterminate
Blank spaces are reserved. No access is allowed.
NOTES:
1. The PM01 and PM00 bits in the PM1 register maintain values set before reset even if software reset or watchdog timer reset is performed.
2. These registers in M32C/84T cannot be used.

Address	Register	Symbol	Value after RESET
0030₁₆			
0031₁₆			
0032₁₆			
0033₁₆			
0034₁₆			
0035₁₆			
0036₁₆			
0037₁₆			
0038₁₆ 0039₁₆ 003A₁₆	Address Match Interrupt Register 6	RMAD6	000000₁₆
003B₁₆			
003C₁₆ 003D₁₆ 003E₁₆	Address Match Interrupt Register 7	RMAD7	000000₁₆
003F₁₆			
0040₁₆			
0041₁₆			
0042₁₆			
0043₁₆			
0044₁₆			
0045₁₆			
0046₁₆			
0047₁₆			
0048₁₆	External Space Wait Control Register 0(1)	EWCR0	X0X0 0011₂
0049₁₆	External Space Wait Control Register 1(1)	EWCR1	X0X0 0011₂
004A₁₆	External Space Wait Control Register 2(1)	EWCR2	X0X0 0011₂
004B₁₆	External Space Wait Control Register 3(1)	EWCR3	X0X0 0011₂
004C₁₆	Page Mode Wait Control Register 0(2)	PWCR0	0001 0001₂
004D₁₆	Page Mode Wait Control Register 1(2)	PWCR1	0001 0001₂
004E₁₆			
004F₁₆			
0050₁₆			
0051₁₆			
0052₁₆			
0053₁₆			
0054₁₆			
0055₁₆	Flash Memory Control Register 1	FMR1	0000 0101₂
0056₁₆			
0057₁₆	Flash Memory Control Register 0	FMR0	0000 0001₂(Flash memory version) XXXX XXX0₂(Masked ROM version)
0058₁₆			
0059₁₆			
005A₁₆			
005B₁₆			
005C₁₆			
005D₁₆			
005E₁₆			
005F₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. These registers in M32C/84T cannot be used.
2. These registers can be used only in the ROMless version.

Address	Register	Symbol	Value after RESET
00C0₁₆			
00C1₁₆			
00C2₁₆			
00C3₁₆			
00C4₁₆			
00C5₁₆			
00C6₁₆			
00C7₁₆			
00C8₁₆			
00C9₁₆			
00CA₁₆			
00CB₁₆			
00CC₁₆			
00CD₁₆			
00CE₁₆			
00CF₁₆			
00D0₁₆			
00D1₁₆			
00D2₁₆			
00D3₁₆			
00D4₁₆			
00D5₁₆			
00D6₁₆			
00D7₁₆			
00D8₁₆			
00D9₁₆			
00DA₁₆			
00DB₁₆			
00DC₁₆			
00DD₁₆			
00DE₁₆			
00DF₁₆			
00E0₁₆			
00E1₁₆			
00E2₁₆			
00E3₁₆			
00E4₁₆			
00E5₁₆			
00E6₁₆			
00E7₁₆			
00E8₁₆ 00E9₁₆	SI/O Receive Buffer Register 0	G0RB	XXXX XXXX₂ X000 XXXX₂
00EA₁₆	Transmit Buffer/Receive Data Register 0	G0TB/G0DR	XX₁₆
00EB₁₆			
00EC₁₆	Receive Input Register 0	G0RI	XX₁₆
00ED₁₆	SI/O Communication Mode Register 0	G0MR	00₁₆
00EE₁₆	Transmit Output Register 0	G0TO	XX₁₆
00EF₁₆	SI/O Communication Control Register 0	G0CR	0000 X011₂

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00F0$_{16}$	Data Compare Register 00	G0CMP0	XX$_{16}$
00F1$_{16}$	Data Compare Register 01	G0CMP1	XX$_{16}$
00F2$_{16}$	Data Compare Register 02	G0CMP2	XX$_{16}$
00F3$_{16}$	Data Compare Register 03	G0CMP3	XX$_{16}$
00F4$_{16}$	Data Mask Register 00	G0MSK0	XX$_{16}$
00F5$_{16}$	Data Mask Register 01	G0MSK1	XX$_{16}$
00F6$_{16}$	Communication Clock Select Register	CCS	XXXX 0000$_2$
00F7$_{16}$			
00F8$_{16}$ 00F9$_{16}$	Receive CRC Code Register 0	G0RCRC	XX$_{16}$ XX$_{16}$
00FA$_{16}$ 00FB$_{16}$	Transmit CRC Code Register 0	G0TCRC	00$_{16}$ 00$_{16}$
00FC$_{16}$	SI/O Extended Mode Register 0	G0EMR	00$_{16}$
00FD$_{16}$	SI/O Extended Receive Control Register 0	G0ERC	00$_{16}$
00FE$_{16}$	SI/O Special Communication Interrupt Detect Register 0	G0IRF	00$_{16}$
00FF$_{16}$	SI/O Extended Transmit Control Register 0	G0ETC	0000 0XXX$_2$
0100$_{16}$ 0101$_{16}$	Time Measurement/Waveform Generating Register 10	G1TM0/G1PO0	XX$_{16}$ XX$_{16}$
0102$_{16}$ 0103$_{16}$	Time Measurement/Waveform Generating Register 11	G1TM1/G1PO1	XX$_{16}$ XX$_{16}$
0104$_{16}$ 0105$_{16}$	Time Measurement/Waveform Generating Register 12	G1TM2/G1PO2	XX$_{16}$ XX$_{16}$
0106$_{16}$ 0107$_{16}$	Time Measurement/Waveform Generating Register 13	G1TM3/G1PO3	XX$_{16}$ XX$_{16}$
0108$_{16}$ 0109$_{16}$	Time Measurement/Waveform Generating Register 14	G1TM4/G1PO4	XX$_{16}$ XX$_{16}$
010A$_{16}$ 010B$_{16}$	Time Measurement/Waveform Generating Register 15	G1TM5/G1PO5	XX$_{16}$ XX$_{16}$
010C$_{16}$ 010D$_{16}$	Time Measurement/Waveform Generating Register 16	G1TM6/G1PO6	XX$_{16}$ XX$_{16}$
010E$_{16}$ 010F$_{16}$	Time Measurement/Waveform Generating Register 17	G1TM7/G1PO7	XX$_{16}$ XX$_{16}$
0110$_{16}$	Waveform Generating Control Register 10	G1POCR0	0000 X000$_2$
0111$_{16}$	Waveform Generating Control Register 11	G1POCR1	0X00 X000$_2$
0112$_{16}$	Waveform Generating Control Register 12	G1POCR2	0X00 X000$_2$
0113$_{16}$	Waveform Generating Control Register 13	G1POCR3	0X00 X000$_2$
0114$_{16}$	Waveform Generating Control Register 14	G1POCR4	0X00 X000$_2$
0115$_{16}$	Waveform Generating Control Register 15	G1POCR5	0X00 X000$_2$
0116$_{16}$	Waveform Generating Control Register 16	G1POCR6	0X00 X000$_2$
0117$_{16}$	Waveform Generating Control Register 17	G1POCR7	0X00 X000$_2$
0118$_{16}$	Time Measurement Control Register 10	G1TMCR0	00$_{16}$
0119$_{16}$	Time Measurement Control Register 11	G1TMCR1	00$_{16}$
011A$_{16}$	Time Measurement Control Register 12	G1TMCR2	00$_{16}$
011B$_{16}$	Time Measurement Control Register 13	G1TMCR3	00$_{16}$
011C$_{16}$	Time Measurement Control Register 14	G1TMCR4	00$_{16}$
011D$_{16}$	Time Measurement Control Register 15	G1TMCR5	00$_{16}$
011E$_{16}$	Time Measurement Control Register 16	G1TMCR6	00$_{16}$
011F$_{16}$	Time Measurement Control Register 17	G1TMCR7	00$_{16}$

X: Indeterminate

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Address	Register	Symbol	Value after RESET
0150₁₆			
0151₁₆			
0152₁₆			
0153₁₆			
0154₁₆			
0155₁₆			
0156₁₆			
0157₁₆			
0158₁₆			
0159₁₆			
015A₁₆			
015B₁₆			
015C₁₆			
015D₁₆			
015E₁₆			
015F₁₆			
0160₁₆			
0161₁₆			
0162₁₆			
0163₁₆			
0164₁₆			
0165₁₆			
0166₁₆			
0167₁₆			
0168₁₆			
0169₁₆			
016A₁₆			
016B₁₆			
016C₁₆			
016D₁₆			
016E₁₆			
016F₁₆			
0170₁₆			
0171₁₆			
0172₁₆			
0173₁₆			
0174₁₆			
0175₁₆			
0176₁₆			
0177₁₆			
0178₁₆	Input Function Select Register	IPS	00₁₆
0179₁₆	Input Function Select Register A	IPSA	00₁₆
017A₁₆			
017B₁₆			
017C₁₆			
017D₁₆ to 01DF₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
02F0₁₆			
02F1₁₆			
02F2₁₆			
02F3₁₆			
02F4₁₆	UART4 Special Mode Register 4	U4SMR4	00₁₆
02F5₁₆	UART4 Special Mode Register 3	U4SMR3	00₁₆
02F6₁₆	UART4 Special Mode Register 2	U4SMR2	00₁₆
02F7₁₆	UART4 Special Mode Register	U4SMR	00₁₆
02F8₁₆	UART4 Transmit/Receive Mode Register	U4MR	00₁₆
02F9₁₆	UART4 Bit Rate Register	U4BRG	XX₁₆
02FA₁₆	UART4 Transmit Buffer Register	U4TB	XX₁₆
02FB₁₆			XX₁₆
02FC₁₆	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000₂
02FD₁₆	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010₂
02FE₁₆	UART4 Receive Buffer Register	U4RB	XX₁₆
02FF₁₆			XX₁₆
0300₁₆	Timer B3, B4, B5 Count Start Flag	TBSR	000X XXXX₂
0301₁₆			
0302₁₆	Timer A1-1 Register	TA11	XX₁₆
0303₁₆			XX₁₆
0304₁₆	Timer A2-1 Register	TA21	XX₁₆
0305₁₆			XX₁₆
0306₁₆	Timer A4-1 Register	TA41	XX₁₆
0307₁₆			XX₁₆
0308₁₆	Three-Phase PWM Control Register 0	INVC0	00₁₆
0309₁₆	Three-Phase PWM Control Register 1	INVC1	00₁₆
030A₁₆	Three-Phase Output Buffer Register 0	IDB0	XX11 1111₂
030B₁₆	Three-Phase Output Buffer Register 1	IDB1	XX11 1111₂
030C₁₆	Dead Time Timer	DTT	XX₁₆
030D₁₆	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XX₁₆
030E₁₆			
030F₁₆			
0310₁₆	Timer B3 Register	TB3	XX₁₆
0311₁₆			XX₁₆
0312₁₆	Timer B4 Register	TB4	XX₁₆
0313₁₆			XX₁₆
0314₁₆	Timer B5 Register	TB5	XX₁₆
0315₁₆			XX₁₆
0316₁₆			
0317₁₆			
0318₁₆			
0319₁₆			
031A₁₆			
031B₁₆	Timer B3 Mode Register	TB3MR	00XX 0000₂
031C₁₆	Timer B4 Mode Register	TB4MR	00XX 0000₂
031D₁₆	Timer B5 Mode Register	TB5MR	00XX 0000₂
031E₁₆			
031F₁₆	External Interrupt Cause Select Register	IFSR	00₁₆

X: Indeterminate

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Address	Register	Symbol	Value after RESET
0320₁₆			
0321₁₆			
0322₁₆			
0323₁₆			
0324₁₆	UART3 Special Mode Register 4	U3SMR4	00₁₆
0325₁₆	UART3 Special Mode Register 3	U3SMR3	00₁₆
0326₁₆	UART3 Special Mode Register 2	U3SMR2	00₁₆
0327₁₆	UART3 Special Mode Register	U3SMR	00₁₆
0328₁₆	UART3 Transmit/Receive Mode Register	U3MR	00₁₆
0329₁₆	UART3 Bit Rate Register	U3BRG	XX₁₆
032A₁₆ 032B₁₆	UART3 Transmit Buffer Register	U3TB	XX₁₆ XX₁₆
032C₁₆	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000₂
032D₁₆	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010₂
032E₁₆ 032F₁₆	UART3 Receive Buffer Register	U3RB	XX₁₆ XX₁₆
0330₁₆			
0331₁₆			
0332₁₆			
0333₁₆			
0334₁₆	UART2 Special Mode Register 4	U2SMR4	00₁₆
0335₁₆	UART2 Special Mode Register 3	U2SMR3	00₁₆
0336₁₆	UART2 Special Mode Register 2	U2SMR2	00₁₆
0337₁₆	UART2 Special Mode Register	U2SMR	00₁₆
0338₁₆	UART2 Transmit/Receive Mode Register	U2MR	00₁₆
0339₁₆	UART2 Bit Rate Register	U2BRG	XX₁₆
033A₁₆ 033B₁₆	UART2 Transmit Buffer Register	U2TB	XX₁₆ XX₁₆
033C₁₆	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000₂
033D₁₆	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010₂
033E₁₆ 033F₁₆	UART2 Receive Buffer Register	U2RB	XX₁₆ XX₁₆
0340₁₆	Count Start Flag	TABSR	00₁₆
0341₁₆	Clock Prescaler Reset Flag	CPSRF	0XXX XXXX₂
0342₁₆	One-Shot Start Flag	ONSF	00₁₆
0343₁₆	Trigger Select Register	TRGSR	00₁₆
0344₁₆	Up/Down Flag	UDF	00₁₆
0345₁₆			
0346₁₆ 0347₁₆	Timer A0 Register	TA0	XX₁₆ XX₁₆
0348₁₆ 0349₁₆	Timer A1 Register	TA1	XX₁₆ XX₁₆
034A₁₆ 034B₁₆	Timer A2 Register	TA2	XX₁₆ XX₁₆
034C₁₆ 034D₁₆	Timer A3 Register	TA3	XX₁₆ XX₁₆
034E₁₆ 034F₁₆	Timer A4 Register	TA4	XX₁₆ XX₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
035016 035116	Timer B0 Register	TB0	XX16 XX16
035216 035316	Timer B1 Register	TB1	XX16 XX16
035416 035516	Timer B2 Register	TB2	XX16 XX16
035616	Timer A0 Mode Register	TA0MR	0016
035716	Timer A1 Mode Register	TA1MR	0016
035816	Timer A2 Mode Register	TA2MR	0016
035916	Timer A3 Mode Register	TA3MR	0016
035A16	Timer A4 Mode Register	TA4MR	0016
035B16	Timer B0 Mode Register	TB0MR	00XX 00002
035C16	Timer B1 Mode Register	TB1MR	00XX 00002
035D16	Timer B2 Mode Register	TB2MR	00XX 00002
035E16	Timer B2 Special Mode Register	TB2SC	XXXX XXX02
035F16	Count Source Prescaler Register(1)	TCSPR	0XXX 00002
036016			
036116			
036216			
036316			
036416	UART0 Special Mode Register 4	U0SMR4	0016
036516	UART0 Special Mode Register 3	U0SMR3	0016
036616	UART0 Special Mode Register 2	U0SMR2	0016
036716	UART0 Special Mode Register	U0SMR	0016
036816	UART0 Transmit/Receive Mode Register	U0MR	0016
036916	UART0 Bit Rate Register	U0BRG	XX16
036A16 036B16	UART0 Transmit Buffer Register	U0TB	XX16 XX16
036C16	UART0 Transmit/Receive Control Register 0	U0C0	0000 10002
036D16	UART0 Transmit/Receive Control Register 1	U0C1	0000 00102
036E16 036F16	UART0 Receive Buffer Register	U0RB	XX16 XX16
037016			
037116			
037216			
037316			
037416			
037516			
037616			
037716			
037816	DMA0 Request Source Select Register	DM0SL	0X00 00002
037916	DMA1 Request Source Select Register	DM1SL	0X00 00002
037A16	DMA2 Request Source Select Register	DM2SL	0X00 00002
037B16	DMA3 Request Source Select Register	DM3SL	0X00 00002
037C16 037D16	CRC Data Register	CRCD	XX16 XX16
037E16	CRC Input Register	CRCIN	XX16
037F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The TCSPR register maintains values set before reset, even after software reset or watchdog timer reset has been performed.

Address	Register	Symbol	Value after RESET
038016 038116	A/D0 Register 0	AD00	XXXX XXXX2 0000 00002
038216 038316	A/D0 Register 1	AD01	XX16 XX16
038416 038516	A/D0 Register 2	AD02	XX16 XX16
038616 038716	A/D0 Register 3	AD03	XX16 XX16
038816 038916	A/D0 Register 4	AD04	XX16 XX16
038A16 038B16	A/D0 Register 5	AD05	XX16 XX16
038C16 038D16	A/D0 Register 6	AD06	XX16 XX16
038E16 038F16	A/D0 Register 7	AD07	XX16 XX16
039016			
039116			
039216	A/D0 Control Register 4	AD0CON4	XXXX 00XX2
039316			
039416	A/D0 Control Register 2	AD0CON2	XX0X X0002
039516	A/D0 Control Register 3	AD0CON3	XXXX X0002
039616	A/D0 Control Register 0	AD0CON0	0016
039716	A/D0 Control Register 1	AD0CON1	0016
039816	D/A Register 0	DA0	XX16
039916			
039A16	D/A Register 1	DA1	XX16
039B16			
039C16	D/A Control Register	DACON	XXXX XX002
039D16			
039E16			
039F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

$V_{CC1}=V_{CC2}=5V$

Switching Characteristics

(V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.23 Memory Expansion Mode and Microprocessor Mode

(when accessing an external memory space with the multiplexed bus)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address Output Delay Time	See Figure 5.2		18	ns
th(BCLK-AD)	Address Output Hold Time (BCLK standard)		-3		ns
th(RD-AD)	Address Output Hold Time (RD standard)(5)		(Note 1)		ns
th(WR-AD)	Address Output Hold Time (WR standard)(5)		(Note 1)		ns
td(BCLK-CS)	Chip-Select Signal Output Delay Time			18	ns
th(BCLK-CS)	Chip-Select Signal Output Hold Time (BCLK standard)		-3		ns
th(RD-CS)	Chip-Select Signal Output Hold Time (RD standard)(5)		(Note 1)		ns
th(WR-CS)	Chip-Select Signal Output Hold Time (WR standard)(5)		(Note 1)		ns
td(BCLK-RD)	RD Signal Output Delay Time			18	ns
th(BCLK-RD)	RD Signal Output Hold Time		-5		ns
td(BCLK-WR)	WR Signal Output Delay Time			18	ns
th(BCLK-WR)	WR Signal Output Hold Time		-5		ns
td(DB-WR)	Data Output Delay Time (WR standard)		(Note 2)		ns
th(WR-DB)	Data Output Hold Time (WR standard)(5)		(Note 1)		ns
td(BCLK-ALE)	ALE Signal Output Delay Time (BCLK standard)			18	ns
th(BCLK-ALE)	ALE Signal Output Hold Time (BCLK standard)		-2		ns
td(AD-ALE)	ALE Signal Output Delay Time (address standard)		(Note 3)		ns
th(ALE-AD)	ALE Signal Output Hold Time (address standard)		(Note 4)		ns
tdz(RD-AD)	Address Output Float Start Time			8	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$th(RD-AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR-AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(RD-CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR-CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR-DB) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycle.

$$td(DB-WR) = \frac{10^9 \times m}{f(BCLK) \times 2} - 25 \quad [ns]$$ (if external bus cycle is aϕ + bϕ, m= (bx2)-1)

3. Values can be obtained from the following equations, according to BCLK frequency and external bus cycle.

$$td(AD-ALE) = \frac{10^9 \times n}{f(BCLK) \times 2} - 20 \quad [ns]$$ (if external bus cycle is aϕ + bϕ, n= a)

4. Values can be obtained from the following equations, according to BCLK frequency and external bus cycle.

$$th(ALE-AD) = \frac{10^9 \times n}{f(BCLK) \times 2} - 10 \quad [ns]$$ (if external bus cycle is aϕ + bϕ, n= a)

5. *tc* ns is added when recovery cycle is inserted.

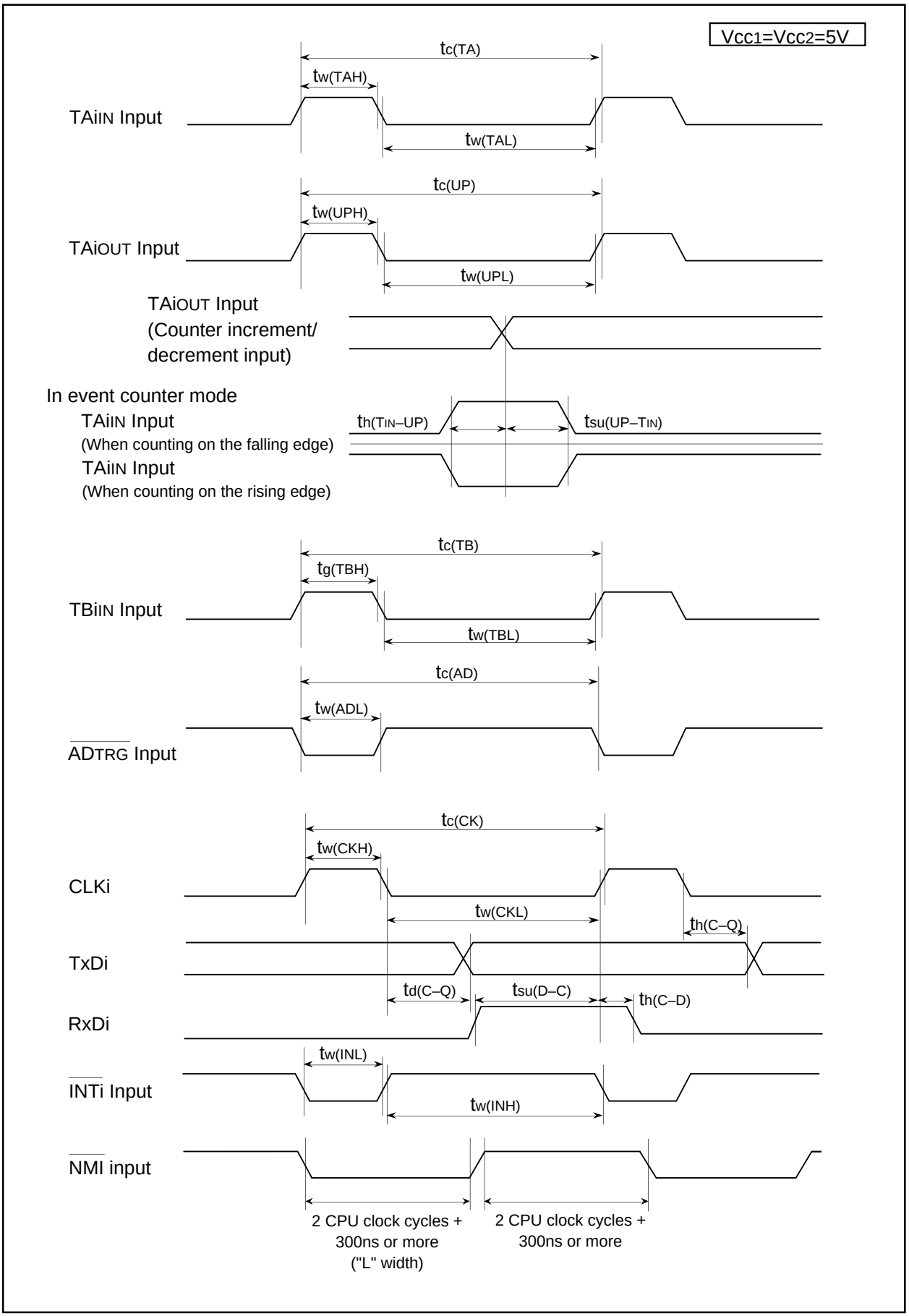

Figure 5.5 Vcc1=Vcc2=5V Timing Diagram (3)

$V_{CC1}=V_{CC2}=3.3V$

Table 5.25 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=AV_{CC}=V_{REF}$= 3.0 to 3.6V, $V_{SS}=AV_{SS}$=0V at Topr = –20 to 85°C, f(BCLK) = 24MHz unless otherwise specified)

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min.	Typ.	Max.	
-	Resolution		$V_{REF}=V_{CC1}$			10	Bits
INL	Integral Nonlinearity Error	No S&H (8-bit)	$V_{CC1}=V_{CC2}=V_{REF}$=3.3V			±2	LSB
DNL	Differential Nonlinearity Error	No S&H (8-bit)				±1	LSB
-	Offset Error	No S&H (8-bit)				±2	LSB
-	Gain Error	No S&H (8-bit)				±2	LSB
R_{LADDER}	Resistor Ladder		$V_{REF}=V_{CC1}$	8		40	kΩ
t_{CONV}	8-bit Conversion Time(1, 2)			6.1			µs
V_{REF}	Reference Voltage			3		V_{CC1}	V
V_{IA}	Analog Input Voltage			0		V_{REF}	V

S&H: Sample and Hold

NOTES:
1. Divide f(X_{IN}), if exceeding 10 MHz, to keep ϕAD frequency at 10 MHz or less.
2. S&H not available.

Table 5.26 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=V_{REF}$=3.0 to 3.6V, $V_{SS}=AV_{SS}$=0V at Topr = –20 to 85°C, f(BCLK) = 24MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.0	mA

NOTES:
1. Measurement results when using one D/A converter. The DAi register (i=0, 1) of the D/A converter, not being used, is set to "00_{16}". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

$V_{CC1}=V_{CC2}=5V$

Table 5.44 Electrical Characteristics (Continued)
($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr = -40 to 85°C (T version), f(BCLK)=32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power Supply Current	In single-chip mode, output pins are left open and other pins are connected to V_{SS}.	f(BCLK)=32 MHz, Square wave, No division		28	50	mA
			f(BCLK)=32 kHz, In low-power consumption mode, Program running on ROM		430		µA
			f(BCLK)=32 kHz, In low-power consumption mode, Program running on RAM(1)		25		µA
			f(BCLK)=32 kHz, In wait mode, Topr=25° C		10		µA
			While clock stops, Topr=25° C		0.8	5	µA
			While clock stops, Topr=85° C			50	µA

NOTES:
1. Value is obtained when setting the FMSTP bit in the FMR0 register to "1" (flash memory stopped).

$V_{CC1}=V_{CC2}=5V$

Table 5.45 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr= -40 to 85°C (T version), f(BCLK)=32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
-	Resolution	$V_{REF}=V_{CC1}$				10	Bits
INL	Integral Nonlinearity Error	$V_{REF}=V_{CC1}=V_{CC2}=5V$	AN_0 to AN_7, $AN0_0$ to $AN0_7$, $AN2_0$ to $AN2_7$, $AN15_0$ to $AN15_7$, ANEX0, ANEX1			±3	LSB
							LSB
			External op-amp connection mode			±7	LSB
							LSB
DNL	Differential Nonlinearity Error					±1	LSB
-	Offset Error					±3	LSB
-	Gain Error					±3	LSB
R_{LADDER}	Resistor Ladder	$V_{REF}=V_{CC1}$		8		40	kΩ
t_{CONV}	10-bit Conversion Time(1, 2)			2.06			µs
t_{CONV}	8-bit Conversion Time(1, 2)			1.75			µs
t_{SAMP}	Sampling Time(1)			0.188			µs
V_{REF}	Reference Voltage			2		V_{CC1}	V
V_{IA}	Analog Input Voltage			0		V_{REF}	V

NOTES:
1. Divide f(X_{IN}), if exceeding 16 MHz, to keep ϕAD frequency at 16 MHz or less.
2. With using the sample and hold function.

Table 5.46 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr= -40 to 85°C (T version), f(BCLK)=32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTES:
1. Measurement when using one D/A converter. The DAi register (i=0, 1) of the D/A converter, not being used, is set to "00_{16}". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

Rev.	Date	Description	
		Page	Summary
		57	• **Figure 5.3 V_{CC1}=V_{CC2}=5V Timing Diagram (1)** *tw(ER)* expression on Note 3 modified; *tcyc* expression added
		58	• **Figure 5.4 V_{CC1}=V_{CC2}=5V Timing Diagram (2)** *tac2(AD-DB)* expression on Note 1 modified; *th(ALE-AD)* expressions on Notes 1 and 2 modified; *tcyc* expression added
		63	• **Table 5.28 Memory Expansion Mode and Microprocessor Mode** *tac1(RD-DB)* expression on Note 1 modified; *tac2(RD-DB)* expression on Note 1 added
		68	• **Figure 5.7 V_{CC1}=V_{CC2}=3.3V Timing Diagram (1)** *tw(ER)* expression on Note 3 modified; *tcyc* expression added
		69	• **Figure 5.8 V_{CC1}=V_{CC2}=3.3V Timing Diagram (2)** *tac2(RD-DB)* expression on Note 1 modified; *th(ALE-AD)* expressions on Notes 1 and 2 modified; *th(WR-CS)* expression on Note 2 modified; *tcyc* expression added
		74	• **Table 5.43 Electrical Characteristics** Parameter f(BCLK) and its values added
		78	• **Table 5.47 Flash Memory Version Electrical Characteristics** Mesurement condition changed