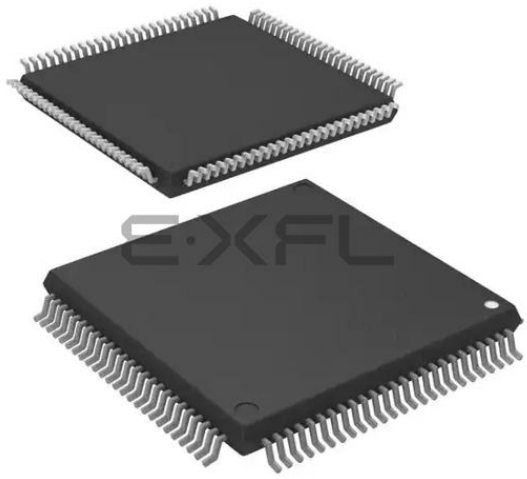
Renesas Electronics America Inc - M30843FJGP#U3 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	85
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30843fjgp-u3

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Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
49		P13$_6$						
50		P13$_5$						
51		P13$_4$						
52		P5$_7$						$\overline{\text{RDY}}$
53		P5$_6$						ALE
54		P5$_5$						$\overline{\text{HOLD}}$
55		P5$_4$						$\overline{\text{HLDA}}$/ALE
56		P13$_3$						
57	V_{SS}							
58		P13$_2$						
59	V_{CC2}							
60		P13$_1$						
61		P13$_0$						
62		P5$_3$						CLK$_{OUT}$/BCLK/ALE
63		P5$_2$						$\overline{\text{RD}}$
64		P5$_1$						$\overline{\text{WRH}}$/$\overline{\text{BHE}}$
65		P5$_0$						$\overline{\text{WRL}}$/$\overline{\text{WR}}$
66		P12$_7$						
67		P12$_6$						
68		P12$_5$						
69		P4$_7$						$\overline{\text{CS0}}$/A$_{23}$
70		P4$_6$						$\overline{\text{CS1}}$/A$_{22}$
71		P4$_5$						$\overline{\text{CS2}}$/A$_{21}$
72		P4$_4$						$\overline{\text{CS3}}$/A$_{20}$
73		P4$_3$						A$_{19}$
74	V_{CC2}							
75		P4$_2$						A$_{18}$
76	V_{SS}							
77		P4$_1$						A$_{17}$
78		P4$_0$						A$_{16}$
79		P3$_7$						A$_{15}$(/D$_{15}$)
80		P3$_6$						A$_{14}$(/D$_{14}$)
81		P3$_5$						A$_{13}$(/D$_{13}$)
82		P3$_4$						A$_{12}$(/D$_{12}$)
83		P3$_3$						A$_{11}$(/D$_{11}$)
84		P3$_2$						A$_{10}$(/D$_{10}$)
85		P3$_1$						A$_9$(/D$_9$)
86		P12$_4$						
87		P12$_3$						
88		P12$_2$						
89		P12$_1$						
90		P12$_0$						
91	V_{CC2}							
92		P3$_0$						A$_8$(/D$_8$)
93	V_{SS}							
94		P2$_7$					AN2$_7$	A$_7$(/D$_7$)
95		P2$_6$					AN2$_6$	A$_6$(/D$_6$)
96		P2$_5$					AN2$_5$	A$_5$(/D$_5$)

NOTES:
1. Bus control pins in M32C/84T cannot be used.

Table 1.5 Pin Characteristics for 100-Pin Package

Package Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin(1)
FP	GP								
1	99		P9$_6$			TxD4/SDA4/SRxD4		ANEX1	
2	100		P9$_5$			CLK4		ANEX0	
3	1		P9$_4$		TB4$_{IN}$	$\overline{CTS4}$/$\overline{RTS4}$/$\overline{SS4}$		DA1	
4	2		P9$_3$		TB3$_{IN}$	$\overline{CTS3}$/$\overline{RTS3}$/$\overline{SS3}$		DA0	
5	3		P9$_2$		TB2$_{IN}$	TxD3/SDA3/SRxD3			
6	4		P9$_1$		TB1$_{IN}$	RxD3/SCL3/STxD3			
7	5		P9$_0$		TB0$_{IN}$	CLK3			
8	6	BYTE							
9	7	CNV$_{SS}$							
10	8	X$_{CIN}$	P8$_7$						
11	9	X$_{COUT}$	P8$_6$						
12	10	$\overline{RESET}$							
13	11	X$_{OUT}$							
14	12	V$_{SS}$							
15	13	X$_{IN}$							
16	14	V$_{CC1}$							
17	15		P8$_5$	$\overline{NMI}$					
18	16		P8$_4$	$\overline{INT2}$					
19	17		P8$_3$	$\overline{INT1}$		CAN0$_{IN}$			
20	18		P8$_2$	$\overline{INT0}$		CAN0$_{OUT}$			
21	19		P8$_1$		TA4$_{IN}$/$\overline{U}$		INPC1$_5$/OUTC1$_5$		
22	20		P8$_0$		TA4$_{OUT}$/U		ISRxD0		
23	21		P7$_7$		TA3$_{IN}$	CAN0$_{IN}$	INPC1$_4$/OUTC1$_4$/ISCLK0		
24	22		P7$_6$		TA3$_{OUT}$	CAN0$_{OUT}$	INPC1$_3$/OUTC1$_3$/ISTxD0		
25	23		P7$_5$		TA2$_{IN}$/$\overline{W}$		INPC1$_2$/OUTC1$_2$/ISRxD1/BE1$_{IN}$		
26	24		P7$_4$		TA2$_{OUT}$/W		INPC1$_1$/OUTC1$_1$/ISCLK1		
27	25		P7$_3$		TA1$_{IN}$/$\overline{V}$	$\overline{CTS2}$/$\overline{RTS2}$/$\overline{SS2}$	INPC1$_0$/OUTC1$_0$/ISTxD1/BE1$_{OUT}$		
28	26		P7$_2$		TA1$_{OUT}$/V	CLK2			
29	27		P7$_1$		TB5$_{IN}$/TA0$_{IN}$	RxD2/SCL2/STxD2	INPC1$_7$/OUTC1$_7$		
30	28		P7$_0$		TA0$_{OUT}$	TxD2/SDA2/SRxD2	INPC1$_6$/OUTC1$_6$		
31	29		P6$_7$			TxD1/SDA1/SRxD1			
32	30		P6$_6$			RxD1/SCL1/STxD1			
33	31		P6$_5$			CLK1			
34	32		P6$_4$			$\overline{CTS1}$/$\overline{RTS1}$/$\overline{SS1}$			
35	33		P6$_3$			TxD0/SDA0/SRxD0			
36	34		P6$_2$			RxD0/SCL0/STxD0			
37	35		P6$_1$			CLK0			
38	36		P6$_0$			$\overline{CTS0}$/$\overline{RTS0}$/$\overline{SS0}$			
39	37		P5$_7$						$\overline{RDY}$
40	38		P5$_6$						ALE
41	39		P5$_5$						$\overline{HOLD}$
42	40		P5$_4$						$\overline{HLDA}$/ALE
43	41		P5$_3$						CLK$_{OUT}$/BCLK/ALE
44	42		P5$_2$						$\overline{RD}$
45	43		P5$_1$						$\overline{WRH}$/$\overline{BHE}$
46	44		P5$_0$						$\overline{WRL}$/$\overline{WR}$
47	45		P4$_7$						$\overline{CS0}$/A$_{23}$
48	46		P4$_6$						$\overline{CS1}$/A$_{22}$
49	47		P4$_5$						$\overline{CS2}$/A$_{21}$
50	48		P4$_4$						$\overline{CS3}$/A$_{20}$

NOTES:
1. Bus control pins in M32C/84T cannot be used.

1.6 Pin Description

Table 1.6 Pin Description (100-Pin and 144-Pin Packages)

Classsfication	Symbol	I/O Type	Supply Voltage	Function
Power Supply	V_{CC1}, V_{CC2} V_{SS}	I	–	Apply 3.0 to 5.5V to both V_{CC1} and V_{CC2} pins. Apply 0V to the V_{SS} pin. $V_{CC1} \geq V_{CC2}$(1, 2)
Analog Power Supply	AVCC AVSS	I	V_{CC1}	Supplies power to the A/D converter. Connect the AVCC pin to V_{CC1} and the AVSS pin to V_{SS}
Reset Input	$\overline{RESET}$	I	V_{CC1}	The microcomputer is in a reset state when "L" is applied to the $\overline{RESET}$ pin
CNVSS	CNVSS	I	V_{CC1}	Switches processor mode. Connect the CNVSS pin to V_{SS} to start up in single-chip mode or to V_{CC1} to start up in microprocessor mode
Input to Switch External Data Bus Width(3)	BYTE	I	V_{CC1}	Switches data bus width in external memory space 3. The data bus is 16 bits wide when the BYTE pin is held "L" and 8 bits wide when it is held "H". Set to either. Connect the BYTE pin to V_{SS} to use the microcomputer in single-chip mode
Bus Control Pins(3)	D_0 to D_7	I/O	V_{CC2}	Inputs and outputs data (D_0 to D_7) while accessing an external memory space with separate bus
	D_8 to D_{15}	I/O	V_{CC2}	Inputs and outputs data (D_8 to D_{15}) while accessing an external memory space with 16-bit separate bus
	A_0 to A_{22}	O	V_{CC2}	Outputs address bits A_0 to A_{22}
	$\overline{A_{23}}$	O	V_{CC2}	Outputs inversed address bit A_{23}
	A_0/D_0 to A_7/D_7	I/O	V_{CC2}	Inputs and outputs data (D_0 to D_7) and outputs 8 low-order address bits (A_0 to A_7) by time-sharing while accessing an external memory space with multiplexed bus
	A_8/D_8 to A_{15}/D_{15}	I/O	V_{CC2}	Inputs and outputs data (D_8 to D_{15}) and outputs 8 middle-order address bits (A_8 to A_{15}) by time-sharing while accessing an external memory space with 16-bit multiplexed bus
	$\overline{CS0}$ to $\overline{CS3}$	O	V_{CC2}	Outputs $\overline{CS0}$ to $\overline{CS3}$ that are chip-select signals specifying an external space
	$\overline{WRL}$ / $\overline{WR}$ $\overline{WRH}$ / $\overline{BHE}$ $\overline{RD}$	O	V_{CC2}	Outputs $\overline{WRL}$, $\overline{WRH}$, ($\overline{WR}$, $\overline{BHE}$) and $\overline{RD}$ signals. $\overline{WRL}$ and $\overline{WRH}$ can be switched with $\overline{WR}$ and $\overline{BHE}$ by program ■ $\overline{WRL}$, $\overline{WRH}$ and $\overline{RD}$ selected: If external data bus is 16 bits wide, data is written to an even address in external memory space when $\overline{WRL}$ is held "L". Data is written to an odd address when $\overline{WRH}$ is held "L". Data is read when $\overline{RD}$ is held "L". ■ $\overline{WR}$, $\overline{BHE}$ and $\overline{RD}$ selected: Data is written to external memory space when $\overline{WR}$ is held "L". Data in an external memory space is read when $\overline{RD}$ is held "L". An odd address is accessed when $\overline{BHE}$ is held "L". Select $\overline{WR}$, $\overline{BHE}$ and $\overline{RD}$ for external 8-bit data bus.
	ALE	O	V_{CC2}	ALE is a signal latching the address
	$\overline{HOLD}$	I	V_{CC2}	The microcomputer is placed in a hold state while the $\overline{HOLD}$ pin is held "L"
	$\overline{HLDA}$	O	V_{CC2}	Outputs an "L" signal while the microcomputer is placed in a hold state
	$\overline{RDY}$	I	V_{CC2}	Bus is placed in a wait state while the $\overline{RDY}$ pin is held "L"

I : Input O : Output I/O : Input and output

NOTES:
1. V_{CC1} is hereinafter referred to as V_{CC} unless otherwise noted.
2. Apply 4.2 to 5.5V to the V_{CC1} and V_{CC2} pins when using M32C/84T. V_{CC1}=V_{CC2}.
3. Bus cotrol pins in M32C/84T cannot be used.

4. Special Function Registers (SFR)

Address	Register	Symbol	Value after RESET
000016			
000116			
000216			
000316			
000416	Processor Mode Register 0(1)	PM0	1000 00002(CNVss pin ="L") 0000 00112(CNVss pin ="H")
000516	Processor Mode Register 1	PM1	0016
000616	System Clock Control Register 0	CM0	0000 10002
000716	System Clock Control Register 1	CM1	0010 00002
000816			
000916	Address Match Interrupt Enable Register	AIER	0016
000A16	Protect Register	PRCR	XXXX 00002
000B16	External Data Bus Width Control Register(2)	DS	XXXX 10002(BYTE pin ="L") XXXX 00002(BYTE pin ="H")
000C16	Main Clock Division Register	MCD	XXX0 10002
000D16	Oscillation Stop Detection Register	CM2	0016
000E16	Watchdog Timer Start Register	WDTS	XX16
000F16	Watchdog Timer Control Register	WDC	000X XXXX2
001016 001116 001216	Address Match Interrupt Register 0	RMAD0	00000016
001316	Processor Mode Register 2	PM2	0016
001416 001516 001616	Address Match Interrupt Register 1	RMAD1	00000016
001716	Voltage Detection Register 2(2)	VCR2	0016
001816 001916 001A16	Address Match Interrupt Register 2	RMAD2	00000016
001B16	Voltage Detection Register 1(2)	VCR1	0000 10002
001C16 001D16 001E16	Address Match Interrupt Register 3	RMAD3	00000016
001F16			
002016			
002116			
002216			
002316			
002416			
002516			
002616	PLL Control Register 0	PLC0	0001 X0102
002716	PLL Control Register 1	PLC1	000X 00002
002816 002916 002A16	Address Match Interrupt Register 4	RMAD4	00000016
002B16			
002C16 002D16 002E16	Address Match Interrupt Register 5	RMAD5	00000016
002F16	Voltage Down Detection Interrupt Register(2)	D4INT	0016

X: Indeterminate
Blank spaces are reserved. No access is allowed.
NOTES:
1. The PM01 and PM00 bits in the PM1 register maintain values set before reset even if software reset or watchdog timer reset is performed.
2. These registers in M32C/84T cannot be used.

Address	Register	Symbol	Value after RESET
00C0₁₆			
00C1₁₆			
00C2₁₆			
00C3₁₆			
00C4₁₆			
00C5₁₆			
00C6₁₆			
00C7₁₆			
00C8₁₆			
00C9₁₆			
00CA₁₆			
00CB₁₆			
00CC₁₆			
00CD₁₆			
00CE₁₆			
00CF₁₆			
00D0₁₆			
00D1₁₆			
00D2₁₆			
00D3₁₆			
00D4₁₆			
00D5₁₆			
00D6₁₆			
00D7₁₆			
00D8₁₆			
00D9₁₆			
00DA₁₆			
00DB₁₆			
00DC₁₆			
00DD₁₆			
00DE₁₆			
00DF₁₆			
00E0₁₆			
00E1₁₆			
00E2₁₆			
00E3₁₆			
00E4₁₆			
00E5₁₆			
00E6₁₆			
00E7₁₆			
00E8₁₆ 00E9₁₆	SI/O Receive Buffer Register 0	G0RB	XXXX XXXX₂ X000 XXXX₂
00EA₁₆	Transmit Buffer/Receive Data Register 0	G0TB/G0DR	XX₁₆
00EB₁₆			
00EC₁₆	Receive Input Register 0	G0RI	XX₁₆
00ED₁₆	SI/O Communication Mode Register 0	G0MR	00₁₆
00EE₁₆	Transmit Output Register 0	G0TO	XX₁₆
00EF₁₆	SI/O Communication Control Register 0	G0CR	0000 X011₂

X: Indeterminate

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Address	Register	Symbol	Value after RESET
00F0$_{16}$	Data Compare Register 00	G0CMP0	XX$_{16}$
00F1$_{16}$	Data Compare Register 01	G0CMP1	XX$_{16}$
00F2$_{16}$	Data Compare Register 02	G0CMP2	XX$_{16}$
00F3$_{16}$	Data Compare Register 03	G0CMP3	XX$_{16}$
00F4$_{16}$	Data Mask Register 00	G0MSK0	XX$_{16}$
00F5$_{16}$	Data Mask Register 01	G0MSK1	XX$_{16}$
00F6$_{16}$	Communication Clock Select Register	CCS	XXXX 0000$_2$
00F7$_{16}$			
00F8$_{16}$ 00F9$_{16}$	Receive CRC Code Register 0	G0RCRC	XX$_{16}$ XX$_{16}$
00FA$_{16}$ 00FB$_{16}$	Transmit CRC Code Register 0	G0TCRC	00$_{16}$ 00$_{16}$
00FC$_{16}$	SI/O Extended Mode Register 0	G0EMR	00$_{16}$
00FD$_{16}$	SI/O Extended Receive Control Register 0	G0ERC	00$_{16}$
00FE$_{16}$	SI/O Special Communication Interrupt Detect Register 0	G0IRF	00$_{16}$
00FF$_{16}$	SI/O Extended Transmit Control Register 0	G0ETC	0000 0XXX$_2$
0100$_{16}$ 0101$_{16}$	Time Measurement/Waveform Generating Register 10	G1TM0/G1PO0	XX$_{16}$ XX$_{16}$
0102$_{16}$ 0103$_{16}$	Time Measurement/Waveform Generating Register 11	G1TM1/G1PO1	XX$_{16}$ XX$_{16}$
0104$_{16}$ 0105$_{16}$	Time Measurement/Waveform Generating Register 12	G1TM2/G1PO2	XX$_{16}$ XX$_{16}$
0106$_{16}$ 0107$_{16}$	Time Measurement/Waveform Generating Register 13	G1TM3/G1PO3	XX$_{16}$ XX$_{16}$
0108$_{16}$ 0109$_{16}$	Time Measurement/Waveform Generating Register 14	G1TM4/G1PO4	XX$_{16}$ XX$_{16}$
010A$_{16}$ 010B$_{16}$	Time Measurement/Waveform Generating Register 15	G1TM5/G1PO5	XX$_{16}$ XX$_{16}$
010C$_{16}$ 010D$_{16}$	Time Measurement/Waveform Generating Register 16	G1TM6/G1PO6	XX$_{16}$ XX$_{16}$
010E$_{16}$ 010F$_{16}$	Time Measurement/Waveform Generating Register 17	G1TM7/G1PO7	XX$_{16}$ XX$_{16}$
0110$_{16}$	Waveform Generating Control Register 10	G1POCR0	0000 X000$_2$
0111$_{16}$	Waveform Generating Control Register 11	G1POCR1	0X00 X000$_2$
0112$_{16}$	Waveform Generating Control Register 12	G1POCR2	0X00 X000$_2$
0113$_{16}$	Waveform Generating Control Register 13	G1POCR3	0X00 X000$_2$
0114$_{16}$	Waveform Generating Control Register 14	G1POCR4	0X00 X000$_2$
0115$_{16}$	Waveform Generating Control Register 15	G1POCR5	0X00 X000$_2$
0116$_{16}$	Waveform Generating Control Register 16	G1POCR6	0X00 X000$_2$
0117$_{16}$	Waveform Generating Control Register 17	G1POCR7	0X00 X000$_2$
0118$_{16}$	Time Measurement Control Register 10	G1TMCR0	00$_{16}$
0119$_{16}$	Time Measurement Control Register 11	G1TMCR1	00$_{16}$
011A$_{16}$	Time Measurement Control Register 12	G1TMCR2	00$_{16}$
011B$_{16}$	Time Measurement Control Register 13	G1TMCR3	00$_{16}$
011C$_{16}$	Time Measurement Control Register 14	G1TMCR4	00$_{16}$
011D$_{16}$	Time Measurement Control Register 15	G1TMCR5	00$_{16}$
011E$_{16}$	Time Measurement Control Register 16	G1TMCR6	00$_{16}$
011F$_{16}$	Time Measurement Control Register 17	G1TMCR7	00$_{16}$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0320₁₆			
0321₁₆			
0322₁₆			
0323₁₆			
0324₁₆	UART3 Special Mode Register 4	U3SMR4	00₁₆
0325₁₆	UART3 Special Mode Register 3	U3SMR3	00₁₆
0326₁₆	UART3 Special Mode Register 2	U3SMR2	00₁₆
0327₁₆	UART3 Special Mode Register	U3SMR	00₁₆
0328₁₆	UART3 Transmit/Receive Mode Register	U3MR	00₁₆
0329₁₆	UART3 Bit Rate Register	U3BRG	XX₁₆
032A₁₆ 032B₁₆	UART3 Transmit Buffer Register	U3TB	XX₁₆ XX₁₆
032C₁₆	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000₂
032D₁₆	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010₂
032E₁₆ 032F₁₆	UART3 Receive Buffer Register	U3RB	XX₁₆ XX₁₆
0330₁₆			
0331₁₆			
0332₁₆			
0333₁₆			
0334₁₆	UART2 Special Mode Register 4	U2SMR4	00₁₆
0335₁₆	UART2 Special Mode Register 3	U2SMR3	00₁₆
0336₁₆	UART2 Special Mode Register 2	U2SMR2	00₁₆
0337₁₆	UART2 Special Mode Register	U2SMR	00₁₆
0338₁₆	UART2 Transmit/Receive Mode Register	U2MR	00₁₆
0339₁₆	UART2 Bit Rate Register	U2BRG	XX₁₆
033A₁₆ 033B₁₆	UART2 Transmit Buffer Register	U2TB	XX₁₆ XX₁₆
033C₁₆	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000₂
033D₁₆	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010₂
033E₁₆ 033F₁₆	UART2 Receive Buffer Register	U2RB	XX₁₆ XX₁₆
0340₁₆	Count Start Flag	TABSR	00₁₆
0341₁₆	Clock Prescaler Reset Flag	CPSRF	0XXX XXXX₂
0342₁₆	One-Shot Start Flag	ONSF	00₁₆
0343₁₆	Trigger Select Register	TRGSR	00₁₆
0344₁₆	Up/Down Flag	UDF	00₁₆
0345₁₆			
0346₁₆ 0347₁₆	Timer A0 Register	TA0	XX₁₆ XX₁₆
0348₁₆ 0349₁₆	Timer A1 Register	TA1	XX₁₆ XX₁₆
034A₁₆ 034B₁₆	Timer A2 Register	TA2	XX₁₆ XX₁₆
034C₁₆ 034D₁₆	Timer A3 Register	TA3	XX₁₆ XX₁₆
034E₁₆ 034F₁₆	Timer A4 Register	TA4	XX₁₆ XX₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<100-pin Package>

Address	Register	Symbol	Value after RESET
03A0$_{16}$			
03A1$_{16}$			
03A2$_{16}$			
03A3$_{16}$			
03A4$_{16}$			
03A5$_{16}$			
03A6$_{16}$			
03A7$_{16}$	Function Select Register D1	PSD1	X0XX XX00$_2$
03A8$_{16}$			
03A9$_{16}$			
03AA$_{16}$			
03AB$_{16}$			
03AC$_{16}$	Function Select Register C2	PSC2	XXXX X00X$_2$
03AD$_{16}$	Function Select Register C3	PSC3	X0XX XXXX$_2$
03AE$_{16}$			
03AF$_{16}$	Function Select Register C	PSC	00X0 0000$_2$
03B0$_{16}$	Function Select Register A0	PS0	00$_{16}$
03B1$_{16}$	Function Select Register A1	PS1	00$_{16}$
03B2$_{16}$	Function Select Register B0	PSL0	00$_{16}$
03B3$_{16}$	Function Select Register B1	PSL1	00$_{16}$
03B4$_{16}$	Function Select Register A2	PS2	00X0 0000$_2$
03B5$_{16}$	Function Select Register A3	PS3	00$_{16}$
03B6$_{16}$	Function Select Register B2	PSL2	00X0 0000$_2$
03B7$_{16}$	Function Select Register B3	PSL3	00$_{16}$
03B8$_{16}$			
03B9$_{16}$			
03BA$_{16}$			
03BB$_{16}$			
03BC$_{16}$			
03BD$_{16}$			
03BE$_{16}$			
03BF$_{16}$			
03C0$_{16}$	Port P6 Register	P6	XX$_{16}$
03C1$_{16}$	Port P7 Register	P7	XX$_{16}$
03C2$_{16}$	Port P6 Direction Register	PD6	00$_{16}$
03C3$_{16}$	Port P7 Direction Register	PD7	00$_{16}$
03C4$_{16}$	Port P8 Register	P8	XX$_{16}$
03C5$_{16}$	Port P9 Register	P9	XX$_{16}$
03C6$_{16}$	Port P8 Direction Register	PD8	00X0 0000$_2$
03C7$_{16}$	Port P9 Direction Register	PD9	00$_{16}$
03C8$_{16}$	Port P10 Register	P10	XX$_{16}$
03C9$_{16}$			
03CA$_{16}$	Port P10 Direction Register	PD10	00$_{16}$
03CB$_{16}$	Set default value to "FF$_{16}$"		
03CC$_{16}$			
03CD$_{16}$			
03CE$_{16}$	Set default value to "FF$_{16}$"		
03CF$_{16}$	Set default value to "FF$_{16}$"		

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Table 5.2 Recommended Operating Conditions

(V_{CC1}= V_{CC2}=3.0V to 5.5V at Topr=– 20 to 85°C unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V_{CC1}, V_{CC2}	Supply Voltage (V_{CC1}≥ V_{CC2})		3.0	5.0	5.5	V
AVCC	Analog Supply Voltage			V_{CC1}		V
VSS	Supply Voltage			0		V
AVSS	Analog Supply Voltage			0		V
V_{IH}	Input High ("H") Voltage	$P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$(4)	0.8V_{CC2}		V_{CC2}	V
		$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	0.8V_{CC1}		V_{CC1}	
		$P7_0$, $P7_1$	0.8V_{CC1}		6.0	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in single-chip mode)	0.8V_{CC2}		V_{CC2}	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in memory expansion mode and microprocesor mode)	0.5V_{CC2}		V_{CC2}	
V_{IL}	Input Low ("L") Voltage	$P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$(4)	0		0.2V_{CC2}	V
		$P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	0		0.2V_{CC1}	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in single-chip mode)	0		0.2V_{CC2}	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in memory expansion mode and microprocesor mode)	0		0.16V_{CC2}	
$I_{OH(peak)}$	Peak Output High ("H") Current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			-10.0	mA
$I_{OH(avg)}$	Average Output High ("H") Current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			-5.0	mA
$I_{OL(peak)}$	Peak Output Low ("L") Current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			10.0	mA
$I_{OL(avg)}$	Average Output Low ("L") Current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			5.0	mA

NOTES:

1. Typical values when average output current is 100ms.
2. Total $I_{OL(peak)}$ for P0, P1, P2, $P8_6$, $P8_7$, P9, P10, P11, P14 and P15 must be 80mA or less.
   Total $I_{OL(peak)}$ for P3, P4, P5, P6, P7, $P8_0$ to $P8_4$, P12 and P13 must be 80mA or less.
   Total $I_{OH(peak)}$ for P0, P1, P2, and P11 must be -40mA or less.
   Total $I_{OH(peak)}$ for $P8_6$, $P8_7$, P9, P10, P14 and P15 must be -40mA or less.
   Total $I_{OH(peak)}$ for P3, P4, P5, P12 and P13 must be -40mA or less.
   Total $I_{OH(peak)}$ for P6, P7, and $P8_0$ to $P8_4$ must be -40mA or less.
3. V_{IH} and V_{IL} reference for $P8_7$ applies when $P8_7$ is used as a programmable input port.
   It does not apply when $P8_7$ is used as X_{CIN}.
4. P11 to P15 are provided in the 144-pin package only.

$V_{CC1}=V_{CC2}=5V$

Table 5.6 Flash Memory Version Electrical Characteristics (V_{CC1}=4.5 to 5.5V, 3.3 to 3.6V at Topr=0 to 60°C unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
-	Program and Erase Endurance(2)		100			cycles
-	Word Program Time (V_{CC1}=5.0V, Topr=25° C)			25	200	µs
-	Lock Bit Program Time			25	200	µs
-	Block Erase Time (V_{CC1}=5.0V, Topr=25° C)	4-Kbyte Block		0.3	4	s
		8-Kbyte Block		0.3	4	s
		32-Kbyte Block		0.5	4	s
		64-Kbyte Block		0.8	4	s
-	All-Unlocked-Block Erase Time(1)				4 x *n*	s
t_{PS}	Wait Time to Stabilize Flash Memory Circuit				15	µs
-	Data Hold Time (Topr=-40 to 85 ° C)		10			years

NOTES:
1. *n* denotes the number of block to be erased.
2. Number of program-erase cycles per block.
   If Program and Erase Endurance is *n* cycle (*n*=100), each block can be erased and programmed *n* cycles. For example, if a 4-Kbyte block A is erased after programming a word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data can not be programmed to the same address more than once without erasing the block. (rewrite prohibited).

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr=–20 to 85°C unless otherwise specified)

Table 5.9 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External Clock Input Cycle Time	31.25		ns
$t_{W(H)}$	External Clock Input High ("H") Width	13.75		ns
$t_{W(L)}$	External Clock Input Low ("L") Width	13.75		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

Table 5.10 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{AC1(RD-DB)}$	Data Input Access Time (RD standard)		(Note 1)	ns
$t_{AC1(AD-DB)}$	Data Input Access Time (AD standard, CS standard)		(Note 1)	ns
$t_{AC2(RD-DB)}$	Data Input Access Time (RD standard, when accessing a space with the multiplexrd bus)		(Note 1)	ns
$t_{AC2(AD-DB)}$	Data Input Access Time (AD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{SU(DB-BCLK)}$	Data Input Setup Time	26		ns
$t_{SU(RDY-BCLK)}$	$\overline{RDY}$ Input Setup Time	26		ns
$t_{SU(HOLD-BCLK)}$	$\overline{HOLD}$ Input Setup Time	30		ns
$t_{H(RD-DB)}$	Data Input Hold Time	0		ns
$t_{H(BCLK-RDY)}$	$\overline{RDY}$ Input Hold Time	0		ns
$t_{H(BCLK-HOLD)}$	$\overline{HOLD}$ Input Hold Time	0		ns
$t_{D(BCLK-HLDA)}$	$\overline{HLDA}$ Output Delay Time		25	ns

NOTES:
1. Values can be obtained from the following equations, according to BCLK frequecncy and external bus cycles. Insert a wait state or lower the operation frequency, $f_{(BCLK)}$, if the calculated value is negative.

$$t_{AC1(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, m=(bx2)+1)

$$t_{AC1(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)}} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, n=a+b)

$$t_{AC2(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, m=(bx2)-1)

$$t_{AC2(AD-DB)} = \frac{10^9 \times p}{f_{(BCLK)} \times 2} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, p={(a+b-1)x2}+1)

$V_{CC1}=V_{CC2}=3.3V$

Timing Requirements

($V_{CC1}=V_{CC2}$= 3.0 to 3.6V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.34 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width (counted on both edges)	80		ns

Table 5.35 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Wdth	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width	200		ns

Table 5.36 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width	200		ns

Table 5.37 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{ADTRG}$ Input Cycle Time (required for trigger)	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ Input Low ("L") Width	125		ns

Table 5.38 Serial I/O

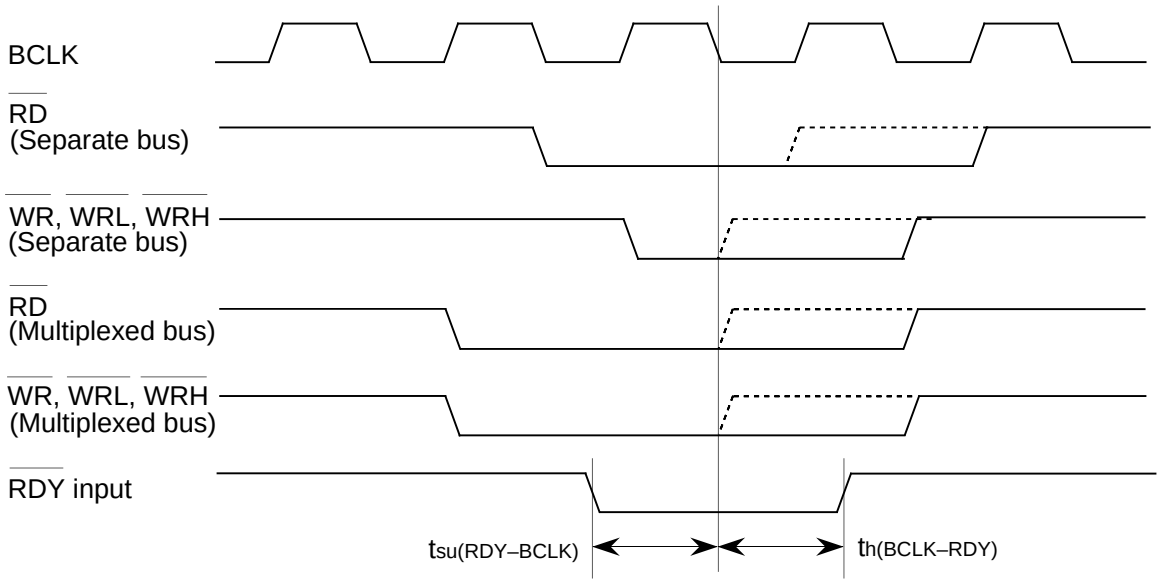
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Setup Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

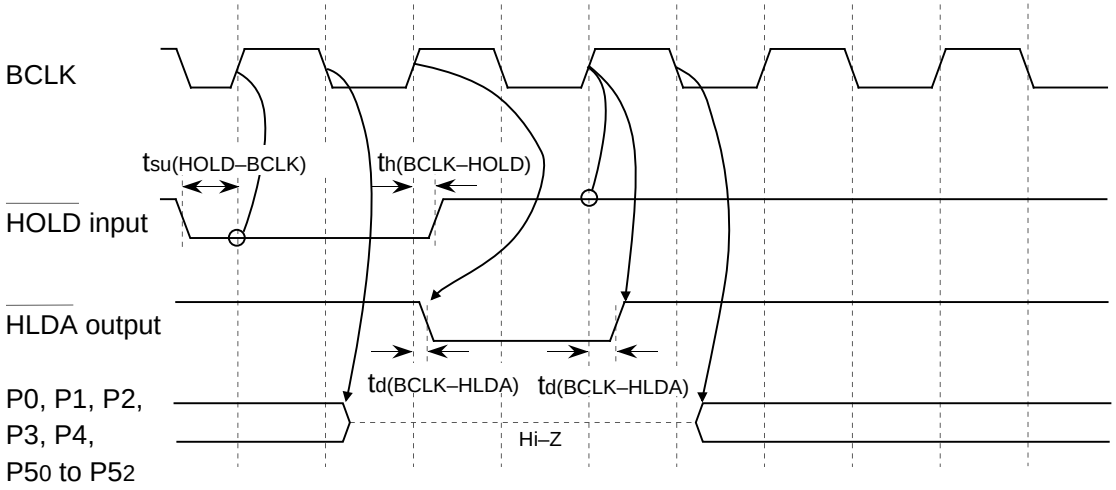
Table 5.39 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input High ("H") Width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ Input Low ("L") Width	250		ns

$V_{CC1}=V_{CC2}=3.3V$

Memory Expansion Mode and Microprocessor Mode





Measurement Conditions:
- $V_{CC1}=V_{CC2}=3.0$ to 3.6V
- Input high and low voltage: $V_{IH}=2.4V$, $V_{IL}=0.6V$
- Output high and low voltage: $V_{OH}=1.5V$, $V_{OL}=1.5V$

Figure 5.10 $V_{CC1}=V_{CC2}=3.3V$ Timing Diagram (4)

Table 5.43 Recommended Operating Conditions (Continued)

(V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS}=0V at Topr = -40 to 85°C (T version) unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$f(BCLK)$	CPU Input Frequency	V_{CC1}=4.2 to 5.5V	0		32	MHz
$f(X_{IN})$	Main Clock Input Frequency	V_{CC1}=4.2 to 5.5V	0		32	MHz
$f(X_{CIN})$	Sub Clock Frequency			32.768	50	kHz
$f(Ring)$	On-chip Oscillator Frequency (V_{CC1}=V_{CC2}=5.0V, Topr=25° C)		0.5	1	2	MHz
$f(PLL)$	PLL Clock Frequency	V_{CC1}=4.2 to 5.5V	10		32	MHz
$t_{SU(PLL)}$	Wait Time to Stabilize PLL Frequency Synthesizer	V_{CC1}=5.0V			5	ms

$V_{CC1}=V_{CC2}=5V$

Table 5.44 Electrical Characteristics

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr = -40 to 85°C (T version), f(BCLK)=32MHz unless otherwise specified)

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	Output High ("H") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$	I_{OH}=-5mA	V_{CC2}-2.0		V_{CC2}	V
		$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OH}=-5mA	V_{CC1}-2.0		V_{CC1}	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$	I_{OH}=-200µA	V_{CC2}-0.3		V_{CC2}	V
		$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$,$P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OH}=-200µA	V_{CC1}-0.3		V_{CC1}	
		X_{OUT}	I_{OH}=-1mA	3.0			V
		X_{COUT} High Power	No load applied		2.5		V
		X_{COUT} Low Power	No load applied		1.6		
V_{OL}	Output Low ("L") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OL}=5mA			2.0	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OL}=200µA			0.45	V
		X_{OUT}	I_{OL}=1mA			2.0	V
		X_{COUT} High Power	No load applied		0		V
		X_{COUT} Low Power	No load applied		0		
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, TA0IN-TA4IN, TB0IN-TB5IN, $\overline{INT0}$-$\overline{INT5}$, $\overline{ADTRG}$, $\overline{CTS0}$-$\overline{CTS4}$, CLK0-CLK4, TA0OUT-TA4OUT, $\overline{NMI}$, $\overline{KI0}$-$\overline{KI3}$, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		$\overline{RESET}$		0.2		1.8	V
I_{IH}	Input High ("H") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=5V			5.0	µA
I_{IL}	Input Low ("L") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=0V			-5.0	µA
R_{PULLUP}	Pull-up Resistance	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	V_I=0V Flash Memory	30	50	167	kΩ
Rf_{XIN}	Feedback Resistance	X_{IN}			1.5		MΩ
Rf_{XCIN}	Feedback Resistance	X_{CIN}			10		MΩ
V_{RAM}	RAM Standby Voltage	In stop mode		2.0			V

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

$V_{CC1}=V_{CC2}=5V$

Table 5.47 Flash Memory Version Electrical Characteristics

(V_{CC1}=4.5 to 5.5V, 3.3 to 3.6V at Topr= 0 to 60°C unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
-	Program and Erase Endurance(2)		100			cycles
-	Word Program Time (V_{CC1}=5.0V, Topr=25° C)			25	200	µs
-	Lock Bit Program Time			25	200	µs
-	Block Erase Time (V_{CC1}=5.0V, Topr=25° C)	4-Kbyte Block		0.3	4	s
		8-Kbyte Block		0.3	4	s
		32-Kbyte Block		0.5	4	s
		64-Kbyte Block		0.8	4	s
-	All-Unlocked-Block Erase Time(1)				4 x *n*	s
t_{PS}	Wait Time to Stabilize Flash Memory Circuit				15	µs
-	Data Hold Time (Topr=-40 to 85 ° C)		10			years

NOTES:
1. *n* denotes the number of block to be erased.
2. Number of program-erase cycles per block.
   If Program and Erase Endurance is *n* cycle (*n*=100), each block can be erased and programmed *n* cycles. For example, if a 4-Kbyte block A is erased after programming a word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data can not be programmed to the same address more than once without erasing the block. (rewrite prohibited).

Table 5.48 Power Supply Timing

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Wait Time to Stabilize Internal Supply Voltage when Power-on	V_{CC1}=3.0 to 5.5V			2	ms

$t_{d(P-R)}$
Wait Time to Stabilize Internal Supply Voltage when Power-on

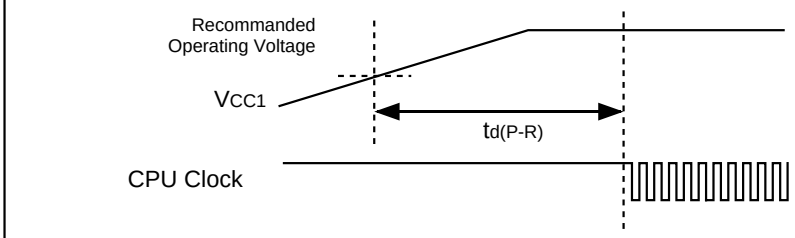


Figure 5.11 Power Supply Timing Diagram

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr= -40 to 85°C (T version) unless otherwise specified)

Table 5.55 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width (counted on both edges)	80		ns

Table 5.56 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width	200		ns

Table 5.57 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width	200		ns

Table 5.58 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max	
$t_{c(AD)}$	$\overline{ADTRG}$ Input Cycle Time (required for trigger)	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ Input Low ("L") Pulse Width	125		ns

Table 5.59 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Setup Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

Table 5.60 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input High ("H") Width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ Input Low ("L") Width	250		ns

REVISION HISTORY	M32C/84 Group (M32C/84, M32C/84T) Datasheet

Rev.	Date	Description	
		Page	Summary
0.40	Sep. 30, 2003	–	New Document
0.50	Feb. 05, 2004		**Overview**
		2, 3	• **Table 1.1** and **Table 1.2 M32C/84 Group Performance** Values for Shortest Instruction Execution Time and Power Consumption" modified
		5	• **Figure 1.2 ROM/RAM Capacity** Products added
			• **Table 1.3 M32C/84 Group** Products added
		6	• **Figure 1.3 Product Numbering System** 128-Kbytes added to ROM capacity Memory
		23	• **Figure 3.1 Memory Map** Diagram modified; products added
			SFR
		24	• "Values after RESET" for the PM1, PM2, D4INT, G0IRF, G1IRF, IDB0 to IDB1, TA0MR to TA4MR, TCSPR, DM0SL to DM3SL registers revised
			• The IPSA register added to address 0179_{16}
			• NOTES added to the PM0 and TCSPR register
			Electrical Characteristics
		44	• Newly added
0.51	Feb. 09, 2004		**Electrical Characteristics**
		50	• **Table 5.6 Flash Memory Version Electrical Characteristics** Note 4 revised
		57	• **Figure 5.2 V_{CC1}=V_{CC2}=5V Timing Diagram (1)** Notes 1 and 2 revised
		68	• **Figure 5.3 V_{CC1}=V_{CC2}=5V Timing Diagram (2)** Notes 1, 2, and 3 revised
		68	• **Figure 5.6 V_{CC1}=V_{CC2}=3.3V Timing Diagram (1)** Notes 1, 2, and 3 revised
		69	• **Figure 5.7 V_{CC1}=V_{CC2}=3.3V Timing Diagram (2)** Notes 1 and 2 revised
0.52	Mar.12, 2004		**Overview**
		2, 3	•**Table 1.1 and 1.2 M32C/84 Group Performance** Values for Power Consumption modified
			Electrical Characteristics
		48	• **Table 5.3 Electrical Characteristics** Maximum values for Power Supply Current modified
		50	• **Table 5.6 Flash Memory Version Electrical Characteristics** Note 1. 100-cycle Products (D3, D5, U3, U5) deleted; Note 4 modified
			• **Table 5.7 Flash Memory Version Program and Erase Voltage and Read Operation Voltage Characteristics (at Topr=0 to 60°C)** deleted
		61	• **Table 5.22 Electrical Characteristics** Maximum values for Power Supply Consumption modified and standard values when "Topr=85°C while clock is stopped" deleted

Rev.	Date	Description	
		Page	Summary
		57	• **Figure 5.3 V_{CC1}=V_{CC2}=5V Timing Diagram (1)** *tw(ER)* expression on Note 3 modified; *tcyc* expression added
		58	• **Figure 5.4 V_{CC1}=V_{CC2}=5V Timing Diagram (2)** *tac2(AD-DB)* expression on Note 1 modified; *th(ALE-AD)* expressions on Notes 1 and 2 modified; *tcyc* expression added
		63	• **Table 5.28 Memory Expansion Mode and Microprocessor Mode** *tac1(RD-DB)* expression on Note 1 modified; *tac2(RD-DB)* expression on Note 1 added
		68	• **Figure 5.7 V_{CC1}=V_{CC2}=3.3V Timing Diagram (1)** *tw(ER)* expression on Note 3 modified; *tcyc* expression added
		69	• **Figure 5.8 V_{CC1}=V_{CC2}=3.3V Timing Diagram (2)** *tac2(RD-DB)* expression on Note 1 modified; *th(ALE-AD)* expressions on Notes 1 and 2 modified; *th(WR-CS)* expression on Note 2 modified; *tcyc* expression added
		74	• **Table 5.43 Electrical Characteristics** Parameter f(BCLK) and its values added
		78	• **Table 5.47 Flash Memory Version Electrical Characteristics** Mesurement condition changed