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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, I ² C, IEBus, SIO, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	85
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30843fjgp-u5

Table 1.5 Pin Characteristics for 100-Pin Package

Package Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin ⁽¹⁾
FP	GP								
1	99		P96			TxD4/SDA4/SRxD4		ANEX1	
2	100		P95			CLK4		ANEX0	
3	1		P94		TB4IN	CTS4/RTS4/SS4		DA1	
4	2		P93		TB3IN	CTS3/RTS3/SS3		DA0	
5	3		P92		TB2IN	TxD3/SDA3/SRxD3			
6	4		P91		TB1IN	RxD3/SCL3/STxD3			
7	5		P90		TB0IN	CLK3			
8	6	BYTE							
9	7	CNVss							
10	8	XCIN	P87						
11	9	XCOUT	P86						
12	10	RESET							
13	11	XOUT							
14	12	Vss							
15	13	XIN							
16	14	VCC1							
17	15		P85	NMI					
18	16		P84	INT2					
19	17		P83	INT1		CAN0IN			
20	18		P82	INT0		CAN0OUT			
21	19		P81		TA4IN/ $\bar{U}$		INPC15/OUTC15		
22	20		P80		TA4OUT/ $\bar{U}$		ISRxD0		
23	21		P77		TA3IN	CAN0IN	INPC14/OUTC14/ISCLK0		
24	22		P76		TA3OUT	CAN0OUT	INPC13/OUTC13/ISTxD0		
25	23		P75		TA2IN/ $\bar{W}$		INPC12/OUTC12/ISRxD1/BE1IN		
26	24		P74		TA2OUT/ $\bar{W}$		INPC11/OUTC11/ISCLK1		
27	25		P73		TA1IN/ $\bar{V}$	CTS2/RTS2/SS2	INPC10/OUTC10/ISTxD1/BE1OUT		
28	26		P72		TA1OUT/ $\bar{V}$	CLK2			
29	27		P71		TB5IN/TA0IN	RxD2/SCL2/STxD2	INPC17/OUTC17		
30	28		P70		TA0OUT	TxD2/SDA2/SRxD2	INPC16/OUTC16		
31	29		P67			TxD1/SDA1/SRxD1			
32	30		P66			RxD1/SCL1/STxD1			
33	31		P65			CLK1			
34	32		P64			CTS1/RTS1/SS1			
35	33		P63			TxD0/SDA0/SRxD0			
36	34		P62			RxD0/SCL0/STxD0			
37	35		P61			CLK0			
38	36		P60			CTS0/RTS0/SS0			
39	37		P57						RDY
40	38		P56						ALE
41	39		P55						HOLD
42	40		P54						HLDA/ALE
43	41		P53						CLKout/BCLK/ALE
44	42		P52						RD
45	43		P51						WRH/BHE
46	44		P50						WRL/WR
47	45		P47						CS0/A23
48	46		P46						CS1/A22
49	47		P45						CS2/A21
50	48		P44						CS3/A20

NOTES:

1. Bus control pins in M32C/84T cannot be used.

Address	Register	Symbol	Value after RESET
0060 ₁₆			
0061 ₁₆			
0062 ₁₆			
0063 ₁₆			
0064 ₁₆			
0065 ₁₆			
0066 ₁₆			
0067 ₁₆			
0068 ₁₆	DMA0 Interrupt Control Register	DM0IC	XXXX X000 ₂
0069 ₁₆	Timer B5 Interrupt Control Register	TB5IC	XXXX X000 ₂
006A ₁₆	DMA2 Interrupt Control Register	DM2IC	XXXX X000 ₂
006B ₁₆	UART2 Receive /ACK Interrupt Control Register	S2RIC	XXXX X000 ₂
006C ₁₆	Timer A0 Interrupt Control Register	TA0IC	XXXX X000 ₂
006D ₁₆	UART3 Receive /ACK Interrupt Control Register	S3RIC	XXXX X000 ₂
006E ₁₆	Timer A2 Interrupt Control Register	TA2IC	XXXX X000 ₂
006F ₁₆	UART4 Receive /ACK Interrupt Control Register	S4RIC	XXXX X000 ₂
0070 ₁₆	Timer A4 Interrupt Control Register	TA4IC	XXXX X000 ₂
0071 ₁₆	UART0/UART3 Bus Conflict Detect Interrupt Control Register	BCN0IC/BCN3IC	XXXX X000 ₂
0072 ₁₆	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X000 ₂
0073 ₁₆	A/D0 Conversion Interrupt Control Register	AD0IC	XXXX X000 ₂
0074 ₁₆	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X000 ₂
0075 ₁₆	Intelligent I/O Interrupt Control Register 0	IIO0IC	XXXX X000 ₂
0076 ₁₆	Timer B1 Interrupt Control Register	TB1IC	XXXX X000 ₂
0077 ₁₆	Intelligent I/O Interrupt Control Register 2	IIO2IC	XXXX X000 ₂
0078 ₁₆	Timer B3 Interrupt Control Register	TB3IC	XXXX X000 ₂
0079 ₁₆	Intelligent I/O Interrupt Control Register 4	IIO4IC	XXXX X000 ₂
007A ₁₆	INT5 Interrupt Control Register	INT5IC	XX00 X000 ₂
007B ₁₆			
007C ₁₆	INT3 Interrupt Control Register	INT3IC	XX00 X000 ₂
007D ₁₆	Intelligent I/O Interrupt Control Register 8	IIO8IC	XXXX X000 ₂
007E ₁₆	INT1 Interrupt Control Register	INT1IC	XX00 X000 ₂
007F ₁₆	Intelligent I/O Interrupt Control Register 10/ CAN Interrupt 1 Control Register	IIO10IC CAN1IC	XXXX X000 ₂
0080 ₁₆			
0081 ₁₆	CAN Interrupt 2 Control Register	CAN2IC	XXXX X000 ₂
0082 ₁₆			
0083 ₁₆			
0084 ₁₆			
0085 ₁₆			
0086 ₁₆			
0087 ₁₆			
0088 ₁₆	DMA1 Interrupt Control Register	DM1IC	XXXX X000 ₂
0089 ₁₆	UART2 Transmit /NACK Interrupt Control Register	S2TIC	XXXX X000 ₂
008A ₁₆	DMA3 Interrupt Control Register	DM3IC	XXXX X000 ₂
008B ₁₆	UART3 Transmit /NACK Interrupt Control Register	S3TIC	XXXX X000 ₂
008C ₁₆	Timer A1 Interrupt Control Register	TA1IC	XXXX X000 ₂
008D ₁₆	UART4 Transmit /NACK Interrupt Control Register	S4TIC	XXXX X000 ₂
008E ₁₆	Timer A3 Interrupt Control Register	TA3IC	XXXX X000 ₂
008F ₁₆	UART2 Bus Conflict Detect Interrupt Control Register	BCN2IC	XXXX X000 ₂

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0090 ₁₆	UART0 Transmit /NACK Interrupt Control Register	S0TIC	XXXX X000 ₂
0091 ₁₆	UART1/UART4 Bus Conflict Detect Interrupt Control Register	BCN1IC/BCN4IC	XXXX X000 ₂
0092 ₁₆	UART1 Transmit/NACK Interrupt Control Register	S1TIC	XXXX X000 ₂
0093 ₁₆	Key Input Interrupt Control Register	KUPIC	XXXX X000 ₂
0094 ₁₆	Timer B0 Interrupt Control Register	TB0IC	XXXX X000 ₂
0095 ₁₆	Intelligent I/O Interrupt Control Register 1	IIO1IC	XXXX X000 ₂
0096 ₁₆	Timer B2 Interrupt Control Register	TB2IC	XXXX X000 ₂
0097 ₁₆	Intelligent I/O Interrupt Control Register 3	IIO3IC	XXXX X000 ₂
0098 ₁₆	Timer B4 Interrupt Control Register	TB4IC	XXXX X000 ₂
0099 ₁₆			
009A ₁₆	INT4 Interrupt Control Register	INT4IC	XX00 X000 ₂
009B ₁₆			
009C ₁₆	INT2 Interrupt Control Register	INT2IC	XX00 X000 ₂
009D ₁₆	Intelligent I/O Interrupt Control Register 9/ CAN Interrupt 0 Control Register	IIO9IC CAN0IC	XXXX X000 ₂
009E ₁₆	INT0 Interrupt Control Register	INT0IC	XX00 X000 ₂
009F ₁₆	Exit Priority Control Register	RLVL	XXXX 0000 ₂
00A0 ₁₆	Interrupt Request Register 0	IIO0IR	0000 000X ₂
00A1 ₁₆	Interrupt Request Register 1	IIO1IR	0000 000X ₂
00A2 ₁₆	Interrupt Request Register 2	IIO2IR	0000 000X ₂
00A3 ₁₆	Interrupt Request Register 3	IIO3IR	0000 000X ₂
00A4 ₁₆	Interrupt Request Register 4	IIO4IR	0000 000X ₂
00A5 ₁₆			
00A6 ₁₆			
00A7 ₁₆			
00A8 ₁₆	Interrupt Request Register 8	IIO8IR	0000 000X ₂
00A9 ₁₆	Interrupt Request Register 9	IIO9IR	0000 000X ₂
00AA ₁₆	Interrupt Request Register 10	IIO10IR	0000 000X ₂
00AB ₁₆	Interrupt Request Register 11	IIO11IR	0000 000X ₂
00AC ₁₆			
00AD ₁₆			
00AE ₁₆			
00AF ₁₆			
00B0 ₁₆	Interrupt Enable Register 0	IIO0IE	00 ₁₆
00B1 ₁₆	Interrupt Enable Register 1	IIO1IE	00 ₁₆
00B2 ₁₆	Interrupt Enable Register 2	IIO2IE	00 ₁₆
00B3 ₁₆	Interrupt Enable Register 3	IIO3IE	00 ₁₆
00B4 ₁₆	Interrupt Enable Register 4	IIO4IE	00 ₁₆
00B5 ₁₆			
00B6 ₁₆			
00B7 ₁₆			
00B8 ₁₆	Interrupt Enable Register 8	IIO8IE	00 ₁₆
00B9 ₁₆	Interrupt Enable Register 9	IIO9IE	00 ₁₆
00BA ₁₆	Interrupt Enable Register 10	IIO10IE	00 ₁₆
00BB ₁₆	Interrupt Enable Register 11	IIO11IE	00 ₁₆
00BC ₁₆			
00BD ₁₆			
00BE ₁₆			
00BF ₁₆			

X: Indeterminate

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Address	Register	Symbol	Value after RESET
00C0 ₁₆			
00C1 ₁₆			
00C2 ₁₆			
00C3 ₁₆			
00C4 ₁₆			
00C5 ₁₆			
00C6 ₁₆			
00C7 ₁₆			
00C8 ₁₆			
00C9 ₁₆			
00CA ₁₆			
00CB ₁₆			
00CC ₁₆			
00CD ₁₆			
00CE ₁₆			
00CF ₁₆			
00D0 ₁₆			
00D1 ₁₆			
00D2 ₁₆			
00D3 ₁₆			
00D4 ₁₆			
00D5 ₁₆			
00D6 ₁₆			
00D7 ₁₆			
00D8 ₁₆			
00D9 ₁₆			
00DA ₁₆			
00DB ₁₆			
00DC ₁₆			
00DD ₁₆			
00DE ₁₆			
00DF ₁₆			
00E0 ₁₆			
00E1 ₁₆			
00E2 ₁₆			
00E3 ₁₆			
00E4 ₁₆			
00E5 ₁₆			
00E6 ₁₆			
00E7 ₁₆			
00E8 ₁₆ 00E9 ₁₆	SI/O Receive Buffer Register 0	G0RB	XXXX XXXX ₂ X000 XXXX ₂
00EA ₁₆ 00EB ₁₆	Transmit Buffer/Receive Data Register 0	G0TB/G0DR	XX ₁₆
00EC ₁₆	Receive Input Register 0	G0RI	XX ₁₆
00ED ₁₆	SI/O Communication Mode Register 0	G0MR	00 ₁₆
00EE ₁₆	Transmit Output Register 0	G0TO	XX ₁₆
00EF ₁₆	SI/O Communication Control Register 0	G0CR	0000 X011 ₂

X: Indeterminate

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Address	Register	Symbol	Value after RESET
00F0 ₁₆	Data Compare Register 00	G0CMP0	XX ₁₆
00F1 ₁₆	Data Compare Register 01	G0CMP1	XX ₁₆
00F2 ₁₆	Data Compare Register 02	G0CMP2	XX ₁₆
00F3 ₁₆	Data Compare Register 03	G0CMP3	XX ₁₆
00F4 ₁₆	Data Mask Register 00	G0MSK0	XX ₁₆
00F5 ₁₆	Data Mask Register 01	G0MSK1	XX ₁₆
00F6 ₁₆	Communication Clock Select Register	CCS	XXXX 0000 ₂
00F7 ₁₆			
00F8 ₁₆	Receive CRC Code Register 0	G0RCRC	XX ₁₆
00F9 ₁₆			XX ₁₆
00FA ₁₆	Transmit CRC Code Register 0	G0TCRC	00 ₁₆
00FB ₁₆			00 ₁₆
00FC ₁₆	SI/O Extended Mode Register 0	G0EMR	00 ₁₆
00FD ₁₆	SI/O Extended Receive Control Register 0	G0ERC	00 ₁₆
00FE ₁₆	SI/O Special Communication Interrupt Detect Register 0	G0IRF	00 ₁₆
00FF ₁₆	SI/O Extended Transmit Control Register 0	G0ETC	0000 0XXX ₂
0100 ₁₆	Time Measurement/Waveform Generating Register 10	G1TM0/G1PO0	XX ₁₆
0101 ₁₆			XX ₁₆
0102 ₁₆	Time Measurement/Waveform Generating Register 11	G1TM1/G1PO1	XX ₁₆
0103 ₁₆			XX ₁₆
0104 ₁₆	Time Measurement/Waveform Generating Register 12	G1TM2/G1PO2	XX ₁₆
0105 ₁₆			XX ₁₆
0106 ₁₆	Time Measurement/Waveform Generating Register 13	G1TM3/G1PO3	XX ₁₆
0107 ₁₆			XX ₁₆
0108 ₁₆	Time Measurement/Waveform Generating Register 14	G1TM4/G1PO4	XX ₁₆
0109 ₁₆			XX ₁₆
010A ₁₆	Time Measurement/Waveform Generating Register 15	G1TM5/G1PO5	XX ₁₆
010B ₁₆			XX ₁₆
010C ₁₆	Time Measurement/Waveform Generating Register 16	G1TM6/G1PO6	XX ₁₆
010D ₁₆			XX ₁₆
010E ₁₆	Time Measurement/Waveform Generating Register 17	G1TM7/G1PO7	XX ₁₆
010F ₁₆			XX ₁₆
0110 ₁₆	Waveform Generating Control Register 10	G1POCR0	0000 X000 ₂
0111 ₁₆	Waveform Generating Control Register 11	G1POCR1	0X00 X000 ₂
0112 ₁₆	Waveform Generating Control Register 12	G1POCR2	0X00 X000 ₂
0113 ₁₆	Waveform Generating Control Register 13	G1POCR3	0X00 X000 ₂
0114 ₁₆	Waveform Generating Control Register 14	G1POCR4	0X00 X000 ₂
0115 ₁₆	Waveform Generating Control Register 15	G1POCR5	0X00 X000 ₂
0116 ₁₆	Waveform Generating Control Register 16	G1POCR6	0X00 X000 ₂
0117 ₁₆	Waveform Generating Control Register 17	G1POCR7	0X00 X000 ₂
0118 ₁₆	Time Measurement Control Register 10	G1TMCR0	00 ₁₆
0119 ₁₆	Time Measurement Control Register 11	G1TMCR1	00 ₁₆
011A ₁₆	Time Measurement Control Register 12	G1TMCR2	00 ₁₆
011B ₁₆	Time Measurement Control Register 13	G1TMCR3	00 ₁₆
011C ₁₆	Time Measurement Control Register 14	G1TMCR4	00 ₁₆
011D ₁₆	Time Measurement Control Register 15	G1TMCR5	00 ₁₆
011E ₁₆	Time Measurement Control Register 16	G1TMCR6	00 ₁₆
011F ₁₆	Time Measurement Control Register 17	G1TMCR7	00 ₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET	
0239 ₁₆	CAN0 Message Slot 9 Control Register / CAN0 Local Mask Register B Standard ID1	C0MCTL9/ C0LMBR1	0000 0000 ₂ ⁽²⁾ XX00 0000 ₂ ⁽²⁾	↑ (Note 1) ↓
023A ₁₆	CAN0 Message Slot 10 Control Register / CAN0 Local Mask Register B Extended ID0	C0MCTL10/ C0LMBR2	0000 0000 ₂ ⁽²⁾ XXXX 0000 ₂ ⁽²⁾	
023B ₁₆	CAN0 Message Slot 11 Control Register / CAN0 Local Mask Register B Extended ID1	C0MCTL11/ C0LMBR3	00 ₁₆ ⁽²⁾ 00 ₁₆ ⁽²⁾	
023C ₁₆	CAN0 Message Slot 12 Control Register / CAN0 Local Mask Register B Extended ID2	C0MCTL12/ C0LMBR4	0000 0000 ₂ ⁽²⁾ XX00 0000 ₂ ⁽²⁾	
023D ₁₆	CAN0 Message Slot 13 Control Register	C0MCTL13	00 ₁₆ ⁽²⁾	
023E ₁₆	CAN0 Message Slot 14 Control Register	C0MCTL14	00 ₁₆ ⁽²⁾	
023F ₁₆	CAN0 Message Slot 15 Control Register	C0MCTL15	00 ₁₆ ⁽²⁾	
0240 ₁₆	CAN0 Slot Buffer Select Register	C0SBS	00 ₁₆ ⁽²⁾	
0241 ₁₆	CAN0 Control Register 1	C0CTLR1	X000 00XX ₂ ⁽²⁾	
0242 ₁₆	CAN0 Sleep Control Register	C0SLPR	XXXX XXX0 ₂	
0243 ₁₆				
0244 ₁₆	CAN0 Acceptance Filter Support Register	C0AFS	00 ₁₆ ⁽²⁾	
0245 ₁₆			01 ₁₆ ⁽²⁾	
0246 ₁₆				
0247 ₁₆				
0248 ₁₆				
0249 ₁₆				
024A ₁₆				
024B ₁₆				
024C ₁₆				
024D ₁₆				
024E ₁₆				
024F ₁₆				
0250 ₁₆				
0251 ₁₆				
0252 ₁₆				
0253 ₁₆				
0254 ₁₆				
0255 ₁₆				
0256 ₁₆				
0257 ₁₆				
0258 ₁₆				
0259 ₁₆				
025A ₁₆				
025B ₁₆				
025C ₁₆				
025D ₁₆ to 02BF ₁₆				

X: Indeterminate

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NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 0220₁₆ to 023F₁₆.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and supplying the clock to the CAN module.

Address	Register	Symbol	Value after RESET
02C0 ₁₆ 02C1 ₁₆	X0 Register Y0 Register	X0R,Y0R	XX ₁₆ XX ₁₆
02C2 ₁₆ 02C3 ₁₆	X1 Register Y1 Register	X1R,Y1R	XX ₁₆ XX ₁₆
02C4 ₁₆ 02C5 ₁₆	X2 Register Y2 Register	X2R,Y2R	XX ₁₆ XX ₁₆
02C6 ₁₆ 02C7 ₁₆	X3 Register Y3 Register	X3R,Y3R	XX ₁₆ XX ₁₆
02C8 ₁₆ 02C9 ₁₆	X4 Register Y4 Register	X4R,Y4R	XX ₁₆ XX ₁₆
02CA ₁₆ 02CB ₁₆	X5 Register Y5 Register	X5R,Y5R	XX ₁₆ XX ₁₆
02CC ₁₆ 02CD ₁₆	X6 Register Y6 Register	X6R,Y6R	XX ₁₆ XX ₁₆
02CE ₁₆ 02CF ₁₆	X7 Register Y7 Register	X7R,Y7R	XX ₁₆ XX ₁₆
02D0 ₁₆ 02D1 ₁₆	X8 Register Y8 Register	X8R,Y8R	XX ₁₆ XX ₁₆
02D2 ₁₆ 02D3 ₁₆	X9 Register Y9 Register	X9R,Y9R	XX ₁₆ XX ₁₆
02D4 ₁₆ 02D5 ₁₆	X10 Register Y10 Register	X10R,Y10R	XX ₁₆ XX ₁₆
02D6 ₁₆ 02D7 ₁₆	X11 Register Y11 Register	X11R,Y11R	XX ₁₆ XX ₁₆
02D8 ₁₆ 02D9 ₁₆	X12 Register Y12 Register	X12R,Y12R	XX ₁₆ XX ₁₆
02DA ₁₆ 02DB ₁₆	X13 Register Y13 Register	X13R,Y13R	XX ₁₆ XX ₁₆
02DC ₁₆ 02DD ₁₆	X14 Register Y14 Register	X14R,Y14R	XX ₁₆ XX ₁₆
02DE ₁₆ 02DF ₁₆	X15 Register Y15 Register	X15R,Y15R	XX ₁₆ XX ₁₆
02E0 ₁₆	X/Y Control Register	XYC	XXXX XX00 ₂
02E1 ₁₆			
02E2 ₁₆			
02E3 ₁₆			
02E4 ₁₆	UART1 Special Mode Register 4	U1SMR4	00 ₁₆
02E5 ₁₆	UART1 Special Mode Register 3	U1SMR3	00 ₁₆
02E6 ₁₆	UART1 Special Mode Register 2	U1SMR2	00 ₁₆
02E7 ₁₆	UART1 Special Mode Register	U1SMR	00 ₁₆
02E8 ₁₆	UART1 Transmit/Receive Mode Register	U1MR	00 ₁₆
02E9 ₁₆	UART1 Bit Rate Register	U1BRG	XX ₁₆
02EA ₁₆ 02EB ₁₆	UART1 Transmit Buffer Register	U1TB	XX ₁₆ XX ₁₆
02EC ₁₆	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000 ₂
02ED ₁₆	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010 ₂
02EE ₁₆ 02EF ₁₆	UART1 Receive Buffer Register	U1RB	XX ₁₆ XX ₁₆

X: Indeterminate

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Address	Register	Symbol	Value after RESET
02F0 ₁₆			
02F1 ₁₆			
02F2 ₁₆			
02F3 ₁₆			
02F4 ₁₆	UART4 Special Mode Register 4	U4SMR4	00 ₁₆
02F5 ₁₆	UART4 Special Mode Register 3	U4SMR3	00 ₁₆
02F6 ₁₆	UART4 Special Mode Register 2	U4SMR2	00 ₁₆
02F7 ₁₆	UART4 Special Mode Register	U4SMR	00 ₁₆
02F8 ₁₆	UART4 Transmit/Receive Mode Register	U4MR	00 ₁₆
02F9 ₁₆	UART4 Bit Rate Register	U4BRG	XX ₁₆
02FA ₁₆	UART4 Transmit Buffer Register	U4TB	XX ₁₆
02FB ₁₆			XX ₁₆
02FC ₁₆	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000 ₂
02FD ₁₆	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010 ₂
02FE ₁₆	UART4 Receive Buffer Register	U4RB	XX ₁₆
02FF ₁₆			XX ₁₆
0300 ₁₆	Timer B3, B4, B5 Count Start Flag	TBSR	000X XXXX ₂
0301 ₁₆			
0302 ₁₆	Timer A1-1 Register	TA11	XX ₁₆
0303 ₁₆			XX ₁₆
0304 ₁₆	Timer A2-1 Register	TA21	XX ₁₆
0305 ₁₆			XX ₁₆
0306 ₁₆	Timer A4-1 Register	TA41	XX ₁₆
0307 ₁₆			XX ₁₆
0308 ₁₆	Three-Phase PWM Control Register 0	INVC0	00 ₁₆
0309 ₁₆	Three-Phase PWM Control Register 1	INVC1	00 ₁₆
030A ₁₆	Three-Phase Output Buffer Register 0	IDB0	XX11 1111 ₂
030B ₁₆	Three-Phase Output Buffer Register 1	IDB1	XX11 1111 ₂
030C ₁₆	Dead Time Timer	DTT	XX ₁₆
030D ₁₆	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XX ₁₆
030E ₁₆			
030F ₁₆			
0310 ₁₆	Timer B3 Register	TB3	XX ₁₆
0311 ₁₆			XX ₁₆
0312 ₁₆	Timer B4 Register	TB4	XX ₁₆
0313 ₁₆			XX ₁₆
0314 ₁₆	Timer B5 Register	TB5	XX ₁₆
0315 ₁₆			XX ₁₆
0316 ₁₆			
0317 ₁₆			
0318 ₁₆			
0319 ₁₆			
031A ₁₆			
031B ₁₆	Timer B3 Mode Register	TB3MR	00XX 0000 ₂
031C ₁₆	Timer B4 Mode Register	TB4MR	00XX 0000 ₂
031D ₁₆	Timer B5 Mode Register	TB5MR	00XX 0000 ₂
031E ₁₆			
031F ₁₆	External Interrupt Cause Select Register	IFSR	00 ₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0320 ₁₆			
0321 ₁₆			
0322 ₁₆			
0323 ₁₆			
0324 ₁₆	UART3 Special Mode Register 4	U3SMR4	00 ₁₆
0325 ₁₆	UART3 Special Mode Register 3	U3SMR3	00 ₁₆
0326 ₁₆	UART3 Special Mode Register 2	U3SMR2	00 ₁₆
0327 ₁₆	UART3 Special Mode Register	U3SMR	00 ₁₆
0328 ₁₆	UART3 Transmit/Receive Mode Register	U3MR	00 ₁₆
0329 ₁₆	UART3 Bit Rate Register	U3BRG	XX ₁₆
032A ₁₆	UART3 Transmit Buffer Register	U3TB	XX ₁₆
032B ₁₆			XX ₁₆
032C ₁₆	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000 ₂
032D ₁₆	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010 ₂
032E ₁₆	UART3 Receive Buffer Register	U3RB	XX ₁₆
032F ₁₆			XX ₁₆
0330 ₁₆			
0331 ₁₆			
0332 ₁₆			
0333 ₁₆			
0334 ₁₆	UART2 Special Mode Register 4	U2SMR4	00 ₁₆
0335 ₁₆	UART2 Special Mode Register 3	U2SMR3	00 ₁₆
0336 ₁₆	UART2 Special Mode Register 2	U2SMR2	00 ₁₆
0337 ₁₆	UART2 Special Mode Register	U2SMR	00 ₁₆
0338 ₁₆	UART2 Transmit/Receive Mode Register	U2MR	00 ₁₆
0339 ₁₆	UART2 Bit Rate Register	U2BRG	XX ₁₆
033A ₁₆	UART2 Transmit Buffer Register	U2TB	XX ₁₆
033B ₁₆			XX ₁₆
033C ₁₆	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000 ₂
033D ₁₆	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010 ₂
033E ₁₆	UART2 Receive Buffer Register	U2RB	XX ₁₆
033F ₁₆			XX ₁₆
0340 ₁₆	Count Start Flag	TABSR	00 ₁₆
0341 ₁₆	Clock Prescaler Reset Flag	CPSRF	0XXX XXXX ₂
0342 ₁₆	One-Shot Start Flag	ONSF	00 ₁₆
0343 ₁₆	Trigger Select Register	TRGSR	00 ₁₆
0344 ₁₆	Up/Down Flag	UDF	00 ₁₆
0345 ₁₆			
0346 ₁₆	Timer A0 Register	TA0	XX ₁₆
0347 ₁₆			XX ₁₆
0348 ₁₆	Timer A1 Register	TA1	XX ₁₆
0349 ₁₆			XX ₁₆
034A ₁₆	Timer A2 Register	TA2	XX ₁₆
034B ₁₆			XX ₁₆
034C ₁₆	Timer A3 Register	TA3	XX ₁₆
034D ₁₆			XX ₁₆
034E ₁₆	Timer A4 Register	TA4	XX ₁₆
034F ₁₆			XX ₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

$$V_{CC1}=V_{CC2}=5V$$

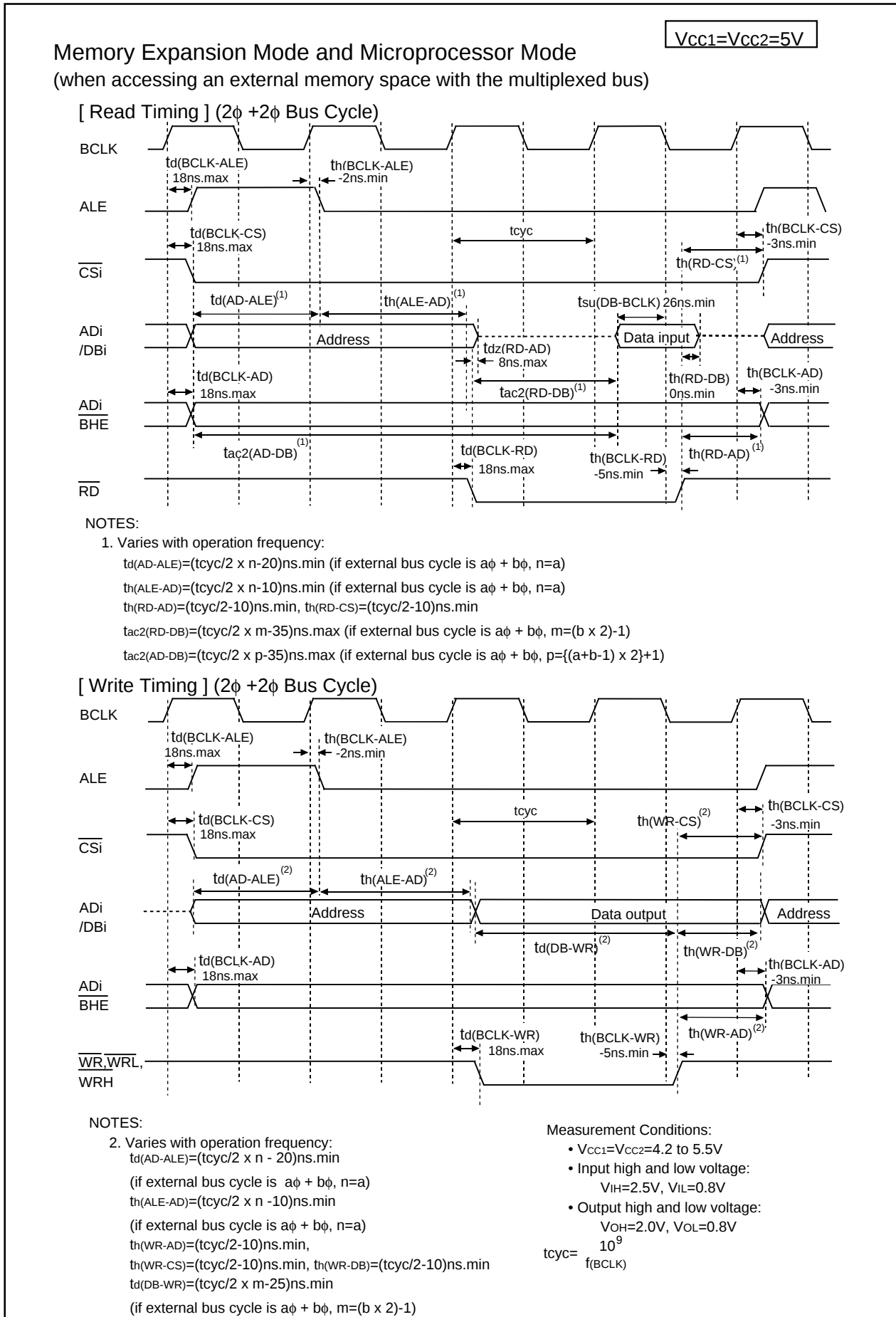
Table 5.3 Electrical Characteristics

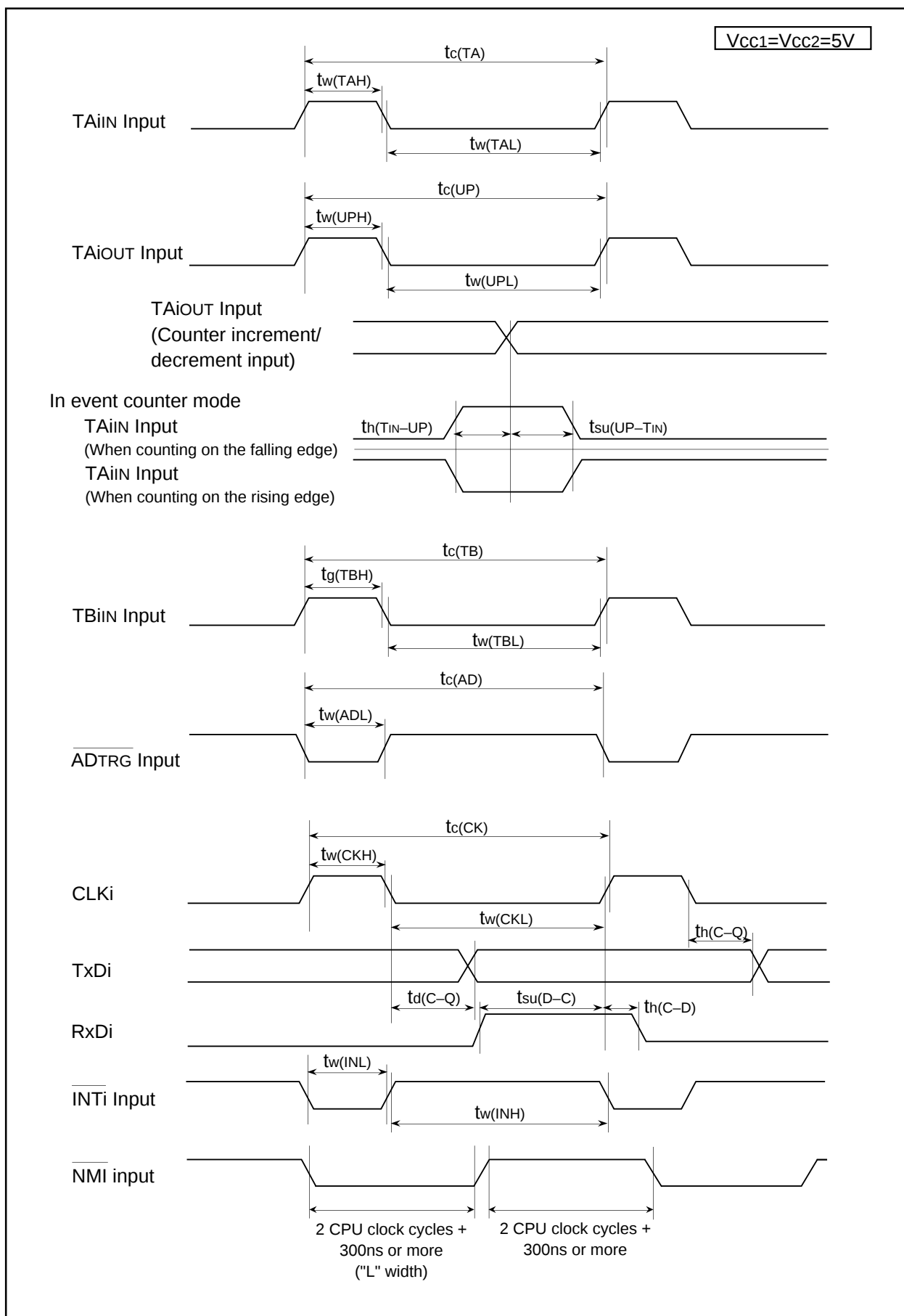
($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr}=-20$ to $85^{\circ}C$, $f(BCLK)=32MHz$ unless otherwise specified)

Symbol		Parameter	Condition	Standard			Unit	
				Min.	Typ.	Max.		
V _{OH}	Output High ("H") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137	I _{OH} =-5mA	V _{CC2} -2.0		V _{CC2}	V	
		P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P140-P146, P150-P157 ⁽¹⁾	I _{OH} =-5mA	V _{CC1} -2.0		V _{CC1}		
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137	I _{OH} =-200μA	V _{CC2} -0.3		V _{CC2}	V	
		P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107,P140-P146, P150-P157 ⁽¹⁾	I _{OH} =-200μA	V _{CC1} -0.3		V _{CC1}		
		X _{OUT}	I _{OH} =-1mA	3.0		V _{CC1}	V	
		X _{COUT}	High Power	No load applied		2.5		V
			Low Power	No load applied		1.6		
V _{OL}	Output Low ("L") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OL} =5mA			2.0	V	
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OL} =200μA			0.45	V	
		X _{OUT}	I _{OL} =1mA			2.0	V	
		X _{COUT}	High Power	No load applied		0		V
			Low Power	No load applied		0		
		V _{T+} -V _{T-}	Hysteresis	HOLD, RDY, TA0IN-TA4IN, TB0IN-TB5IN, INT0-INT5, ADTRG, CTS0-CTS4, CLK0-CLK4, TA0OUT-TA4OUT, NMI, KI0-KI3, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0
RESET				0.2		1.8	V	
I _{IH}	Input High ("H") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾ , X _{IN} , RESET, CNV _{SS} , BYTE	V _I =5V			5.0	μA	
I _{IL}	Input Low ("L") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾ , X _{IN} , RESET, CNV _{SS} , BYTE	V _I =0V			-5.0	μA	
R _{PULLUP}	Pull-up Resistance	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	V _I =0V	Flash Memory	30	50	167	kΩ
				Masked ROM	20	40	167	
R _{fXIN}	Feedback Resistance	X _{IN}				1.5		MΩ
R _{fXCIN}	Feedback Resistance	X _{CIN}				10		MΩ
V _{RAM}	RAM Standby Voltage	In stop mode		2.0				V

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

Figure 5.4 $V_{CC1}=V_{CC2}=5V$ Timing Diagram (2)

Figure 5.5 $V_{CC1}=V_{CC2}=5V$ Timing Diagram (3)

$$V_{CC1}=V_{CC2}=3.3V$$

Switching Characteristics

($V_{CC1}=V_{CC2}=3.0$ to $3.6V$, $V_{SS} = 0V$ at $T_{opr} = -20$ to $85^{\circ}C$ unless otherwise specified)

Table 5.40 Memory Expansion Mode and Microprocessor Mode
(when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 5.2		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard) ⁽³⁾		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard) ⁽³⁾		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-Select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-Select Signal Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-CS)}$	Chip-Select Signal Output Hold Time (RD standard) ⁽³⁾		0		ns
$t_{h(WR-CS)}$	Chip-Select Signal Output Hold Time (WR standard) ⁽³⁾		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-3		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		0		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 2)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard) ⁽³⁾		(Note 1)		ns
$t_{w(WR)}$	WR Output Width		(Note 2)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 20 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

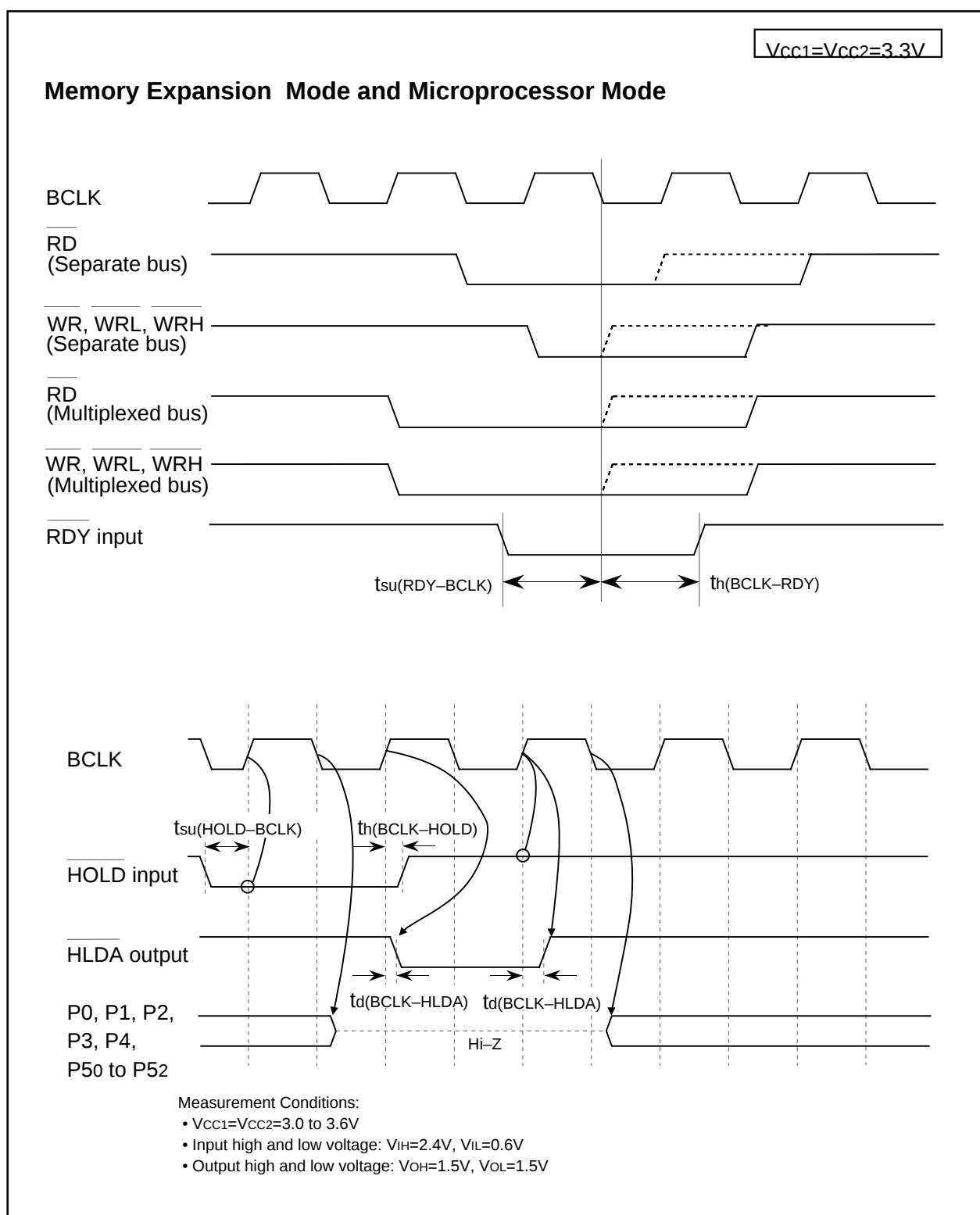
$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles.

$$t_{w(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, n=(b \times 2)-1)$$

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)}} - 20 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, m=b)$$

3. t_{cns} is added when recovery cycle is inserted.

Figure 5.10 $V_{CC1}=V_{CC2}=3.3V$ Timing Diagram (4)

$$V_{CC1}=V_{CC2}=5V$$

Table 5.45 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr}= -40$ to $85^{\circ}C$ (T version), $f(BCLK)=32MHz$ unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution	$V_{REF}=V_{CC1}$			10	Bits
INL	Integral Nonlinearity Error	$V_{REF}=V_{CC1}=V_{CC2}=5V$			± 3	LSB
						LSB
		External op-amp connection mode			± 7	LSB
DNL	Differential Nonlinearity Error				± 1	LSB
-	Offset Error				± 3	LSB
-	Gain Error				± 3	LSB
RLADDER	Resistor Ladder	$V_{REF}=V_{CC1}$	8		40	k Ω
t _{CONV}	10-bit Conversion Time ^(1, 2)		2.06			μs
t _{CONV}	8-bit Conversion Time ^(1, 2)		1.75			μs
t _{SAMP}	Sampling Time ⁽¹⁾		0.188			μs
V _{REF}	Reference Voltage		2		V_{CC1}	V
V _{IA}	Analog Input Voltage		0		V_{REF}	V

NOTES:

1. Divide $f(X_{IN})$, if exceeding 16 MHz, to keep ϕ_{AD} frequency at 16 MHz or less.
2. With using the sample and hold function.

Table 5.46 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr}= -40$ to $85^{\circ}C$ (T version), $f(BCLK)=32MHz$ unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t _{SU}	Setup Time				3	μs
R _O	Output Resistance		4	10	20	k Ω
I _{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTES:

1. Measurement when using one D/A converter. The DA_i register (i=0, 1) of the D/A converter, not being used, is set to "00₁₆". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

$$V_{CC1}=V_{CC2}=5V$$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr}= -40$ to $85^{\circ}C$ (T version) unless otherwise specified)

Table 5.50 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	100		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	40		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	40		ns

Table 5.51 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	400		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	200		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	200		ns

Table 5.52 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	200		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 5.53 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 5.54 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAiOUT Input High ("H") Width	1000		ns
$t_{w(UPL)}$	TAiOUT Input Low ("L") Width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAiOUT Input Hold Time	400		ns

$$V_{CC1}=V_{CC2}=5V$$

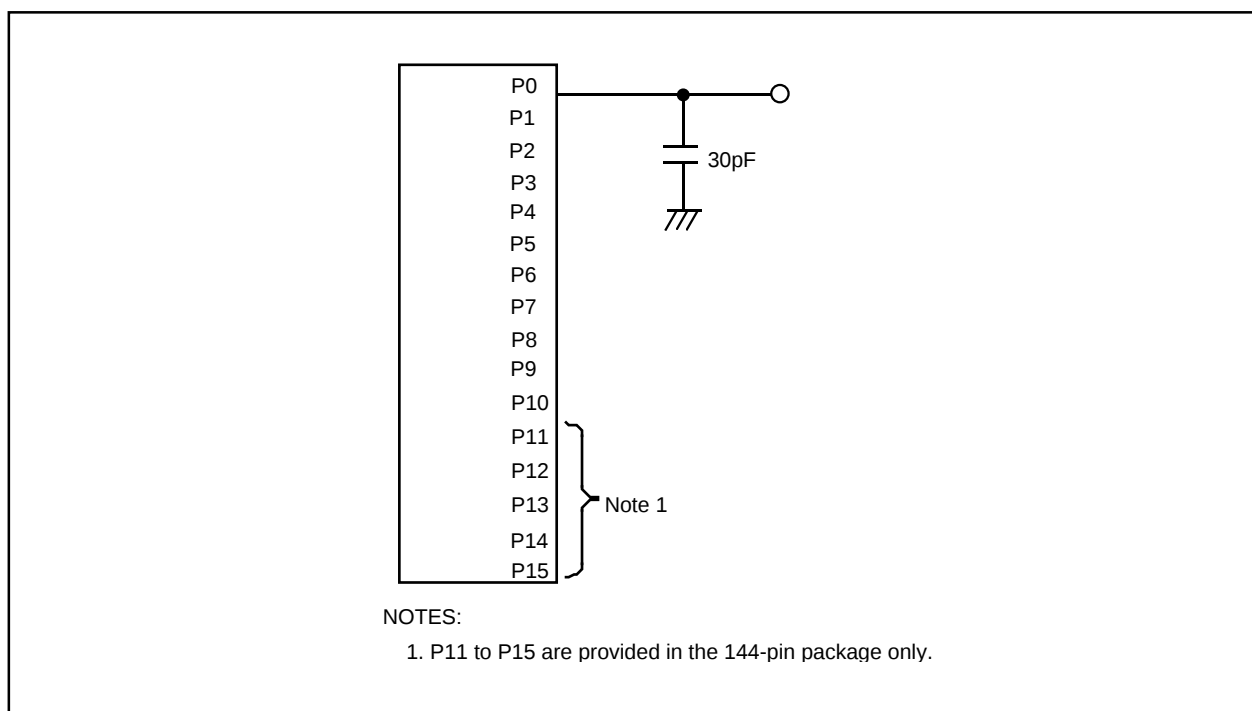


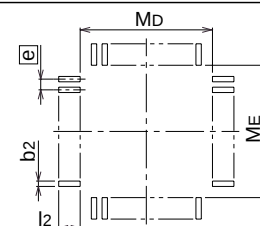
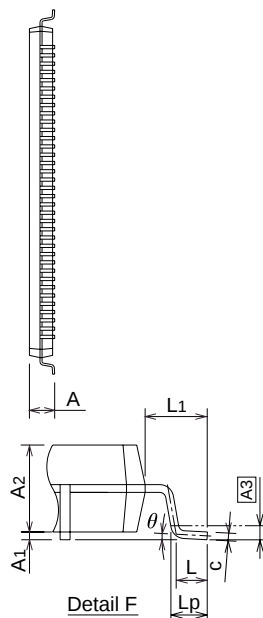
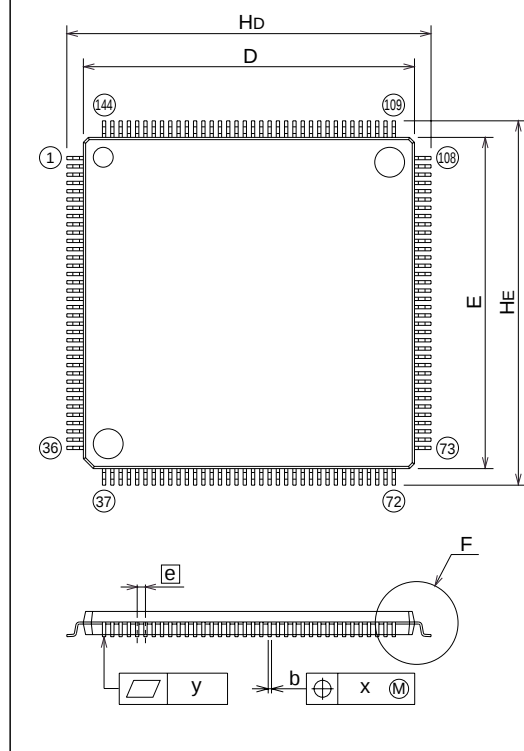
Figure 5.12 P0 to P15 Measurement Circuit

Package Dimensions

PLQP0144KA-A (144P6Q-A)

Plastic 144pin 20X20mm body LQFP

JEITA Package Code	RENESAS Code	Previous Code	Mass[Typ.]
P-LQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A	1.2g



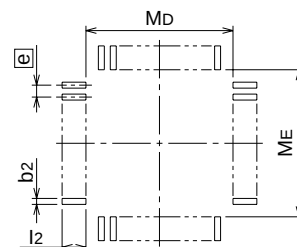
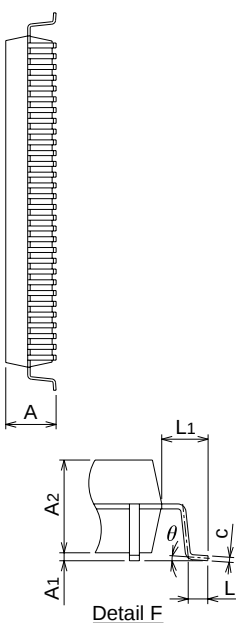
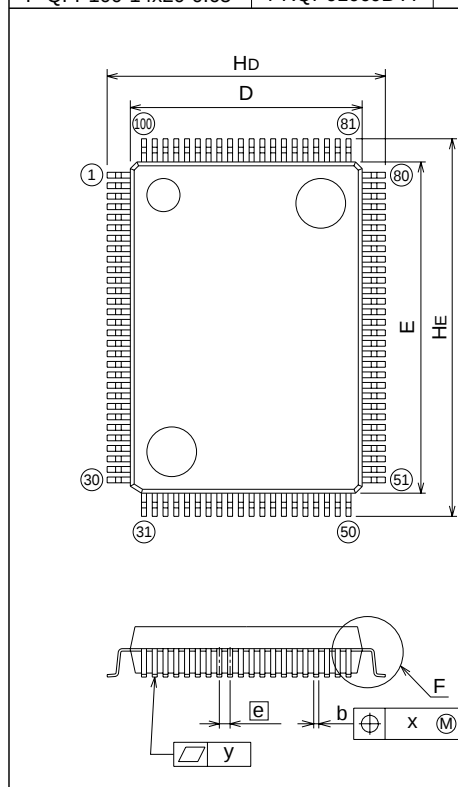
Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.7
A1	0.05	0.125	0.2
A2	—	1.4	—
b	0.17	0.22	0.27
c	0.105	0.125	0.175
D	19.9	20.0	20.1
E	19.9	20.0	20.1
e	—	0.5	—
Hd	21.8	22.0	22.2
HE	21.8	22.0	22.2
L	0.35	0.5	0.65
L1	—	1.0	—
Lp	0.45	0.6	0.75
A3	—	0.25	—
x	—	—	0.08
y	—	—	0.1
θ	0°	—	8°
b2	—	0.225	—
l2	0.95	—	—
MD	—	20.4	—
ME	—	20.4	—

PRQP0100JB-A (100P6S-A)

Plastic 100pin 14X20mm body QFP

JEITA Package Code	RENESAS Code	Previous Code	Mass[Typ.]
P-QFP100-14x20-0.65	PRQP0100JB-A	100P6S-A	1.6g



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	3.05
A1	0	0.1	0.2
A2	—	2.8	—
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	—	0.65	—
Hd	16.5	16.8	17.1
HE	22.5	22.8	23.1
L	0.4	0.6	0.8
L1	—	1.4	—
x	—	—	0.13
y	—	—	0.1
θ	0°	—	10°
b2	—	0.35	—
l2	1.3	—	—
Md	—	14.6	—
ME	—	20.6	—

REVISION HISTORY	M32C/84 Group (M32C/84, M32C/84T) Datasheet
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Rev.	Date	Description	
		Page	Summary
1.00	Jun.01, 2004	-	M32C/84T (High-reliability version) added
		All Pages	Words standardized: On-chip oscillator, A/D converter and D/A converter
			Overview
		1	• 1.1 Applications Automobiles added
		2, 3	• Table 1.1 and Table 1.2 M32C/84 Group (M32C/84, M32C/84T) Performance M32C/84T added; note 3 added
		4	• Figure 1.1 M32C/84 Group (M32C/84, M32C/84T) Block Diagram Note 3 added
		5	• 1.4 Product Information Description modified
		6	• Figure 1.2 ROM/RAM Capacity figure modified
		6	• Table 1.3 M32C/84 Group M32C/84T added
		6	• Figure 1.3 Product Numbering System M32C/84T added
		7	• Figure 1.4 Pin Assignment for 144-Pin Package Note 3 added
		12	• Figure 1.6 Pin Assignment for 100-Pin Package Note 5 added
		8 to 10	• Table 1.5 Pin Characteristics for 144-Pin Package Note 1 added
		13, 14	• Table 1.6 Pin Characteristics for 100-Pin Package Note 1 added
		15 to 18	• Table 1.7 Pin Description Notes added
			Memory
		22	• Figure 3.1 Memory Map Tables of internal ROM/internal RAM modified; note 2 modified; notes 4 and 5 added
			SFR
		23	• Note 2 added
		24	• PWCR0 and PWCR1 registers deleted
			• “Values after RESET” of the masked ROM version added to the FMR0 register
			• Note 1 added
			Electrical Characteristics
		44	• Table 5.2 Recommended Operating Conditions f_{ripple} , $V_{p-p(\text{ripple})}$, V_{CC} , SV_{CC} and note 1 deleted
		47	• Table 5.3 Electrical Characteristics R_{PULLUP} value for the masked ROM version added
		48	• Table 5.4 A/D Conversion Characteristics t_{SMP} value modified; note 1 added
		50	• Table 5.7 Low Voltage Detect Circuit Electrical Characteristics added
			• Table 5.8 Power Supply Timing added
			• Figure 5.1 Power Supply Timing Diagram added
		55	• Table 5.23 Memory Expansion Mode and Microprocessor Mode $t_{h(BCLK-ALE)}$ value modified
		61	• Table 5.24 Electrical Characteristics R_{PULLUP} value for the masked ROM version added
		62	• Table 5.25 A/D Conversion Characteristics t_{CONV} value modified

