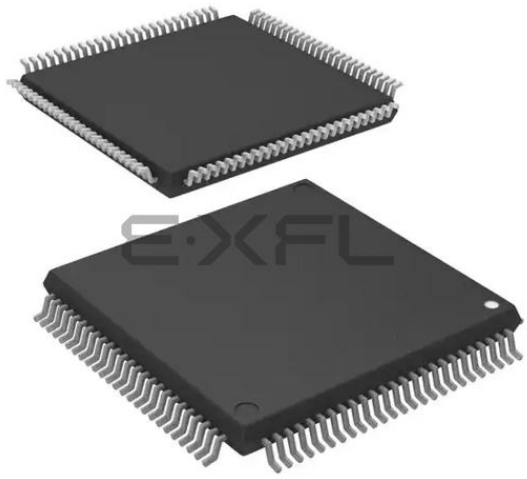
Renesas Electronics America Inc - M30843FWGP#U3 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	85
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30843fwgp-u3

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Rev.1.21
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1. Overview

The M32C/84 group (M32C/84, M32C/84T) microcomputer is a single-chip control unit that utilizes high-performance silicon gate CMOS technology with the M32C/80 series CPU core. The M32C/84 group (M32C/84, M32C/84T) is available in 144-pin and 100-pin plastic molded LQFP/QFP packages.

With a 16-Mbyte address space, this microcomputer combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.

It includes a multiplier and DMAC adequate for office automation, communication devices and industrial equipments, and other high-speed processing applications.

1.1 Applications

Automobiles, audio, cameras, office equipment, communications equipment, portable equipment, etc.

Table 1.2 M32C/84 Group (M32C/84, M32C/84T) Performance (100-Pin Package)

Characteristic		Performance	
		M32C/84	M32C/84T
CPU	Basic Instructions	108 instructions	
	Shortest Instruction Execution Time	31.3 ns (f(BCLK)=32 MHz, V_{CC1}=4.2 V to 5.5 V) 41.7 ns (f(BCLK)=24 MHz, V_{CC1}=3.0 V to 5.5 V)	31.3 ns (f(BCLK)=32 MHz, V_{CC1}=4.2 V to 5.5 V)
	Operation Mode	Single-chip mode, Memory expansion mode and Microprocessor mode	Single-chip mode
	Address Space	16 Mbytes	
	Memory Capacity	See Table 1.3	
Peripheral Function	I/O Port	87 I/O pins and 1 input pin	
	Multifunction Timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit	
	Intelligent I/O	Time measurement function or Waveform generating function: 16 bits x 8 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing)	
	Serial I/O	5 Channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus(1), I^2C bus(2)	
	CAN Module	1 channel Supporting CAN 2.0B specification	
	A/D Converter	10-bit A/D converter: 1 circuit, 26 channels	
	D/A Converter	8 bits x 2 channels	
	DMAC	4 channels	
	DMAC II	Can be activated by all peripheral function interrupt sources Immediate transfer, Calculation transfer and Chain transfer functions	
	CRC Calculation Circuit	CRC-CCITT	
	X/Y Converter	16 bits x 16 bits	
	Watchdog Timer	15 bits x 1 channel (with prescaler)	
	Interrupt	38 internal and 8 external sources, 5 software sources Interrupt priority level: 7	
	Clock Generation Circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally	
	Oscillation Stop Detect Function	Main clock oscillation stop detect function	
	Voltage Detection Circuit	Available (optional)	Not available(4)
Electrical Characteristics	Supply Voltage	V_{CC1}=4.2 V to 5.5 V, V_{CC2}=3.0 V to V_{CC1} (f(BCLK)=32 MHz) V_{CC1}=3.0 V to 5.5 V, V_{CC2}=3.0 V to V_{CC1} (f(BCLK)=24 MHz)	V_{CC1}=V_{CC2}=4.2 V to 5.5 V, (f(BCLK)=32 MHz)(3)
	Power Consumption	28 mA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 MHz) 22 mA (V_{CC1}=V_{CC2}=3.3 V, f(BCLK)=24 MHz) 10µA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 kHz, in wait mode)	28 mA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 MHz) 10µA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 kHz, in wait mode)
Flash Memory	Program/Erase Supply Voltage	3.3 V ± 0.3 V or 5.0 V ± 0.5 V	5.0 V ± 0.5 V
	Program and Erase Endurance	100 times (all space)	
Operating Ambient Temperature		–20 to 85°C –40 to 85°C (optional)	–40 to 85°C (T version)
Package		100-pin plastic molded LQFP/QFP	

NOTES:
1. IEBus is a trademark of NEC Electronics Corporation.
2. I^2C bus is a trademark of Koninklijke Philips Electronics N. V.
3. The supply voltage of M32C/84T (High-reliability version) must be V_{CC1}=V_{CC2}.
4. The cold start-up/warm start-up determine function is available only at the user's option.

All options are on a request basis.

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

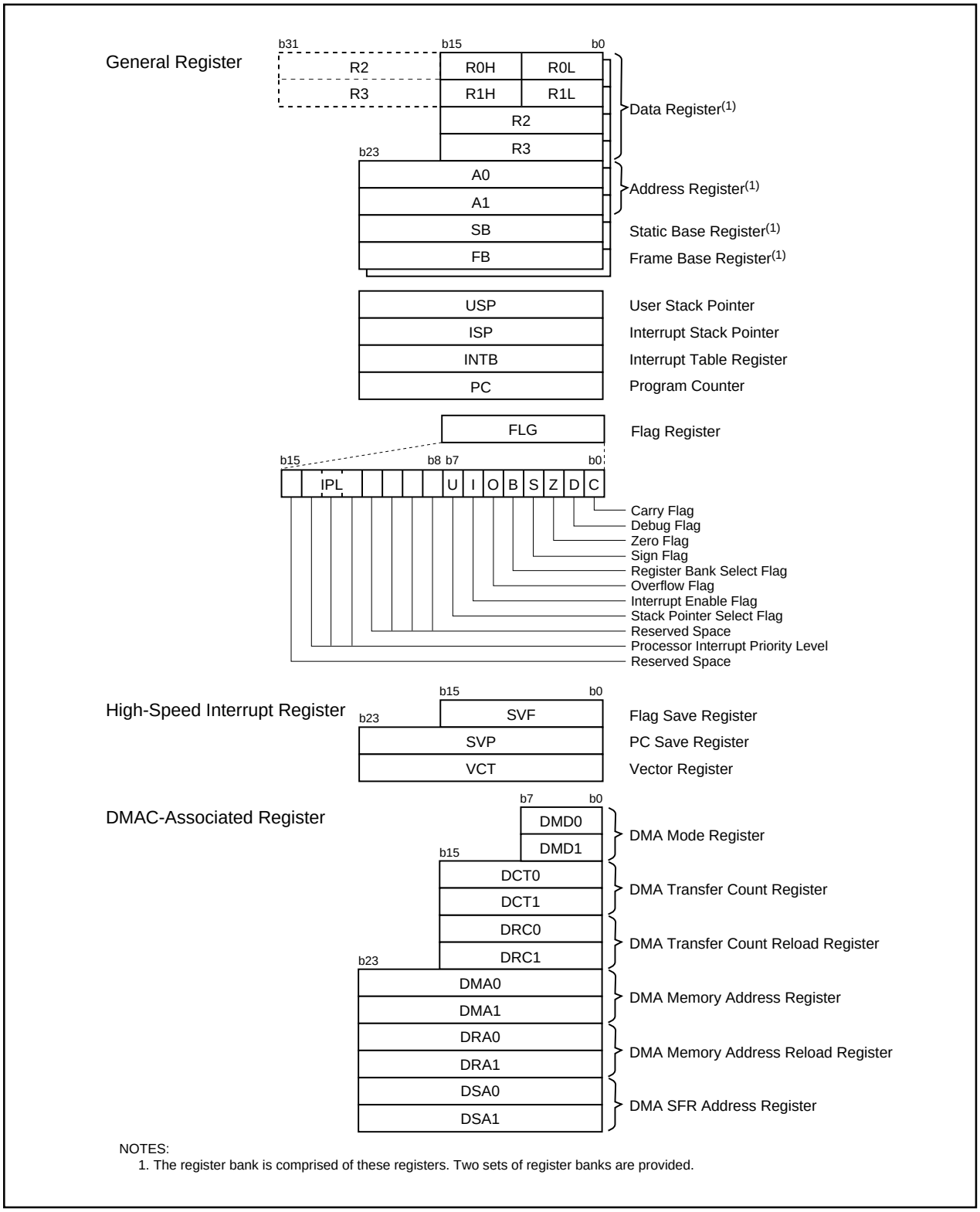
Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin(1)
97		P2$_4$					AN2$_4$	A$_4$(/D$_4$)
98		P2$_3$					AN2$_3$	A$_3$(/D$_3$)
99		P2$_2$					AN2$_2$	A$_2$(/D$_2$)
100		P2$_1$					AN2$_1$	A$_1$(/D$_1$)
101		P2$_0$					AN2$_0$	A$_0$(/D$_0$)
102		P1$_7$	$\overline{\text{INT5}}$					D$_{15}$
103		P1$_6$	$\overline{\text{INT4}}$					D$_{14}$
104		P1$_5$	$\overline{\text{INT3}}$					D$_{13}$
105		P1$_4$						D$_{12}$
106		P1$_3$						D$_{11}$
107		P1$_2$						D$_{10}$
108		P1$_1$						D$_9$
109		P1$_0$						D$_8$
110		P0$_7$					AN0$_7$	D$_7$
111		P0$_6$					AN0$_6$	D$_6$
112		P0$_5$					AN0$_5$	D$_5$
113		P0$_4$					AN0$_4$	D$_4$
114		P11$_4$						
115		P11$_3$				INPC1$_3$/OUTC1$_3$		
116		P11$_2$				INPC1$_2$/OUTC1$_2$/ISRxD1/BE1$_{IN}$		
117		P11$_1$				INPC1$_1$/OUTC1$_1$/ISCLK1		
118		P11$_0$				INPC1$_0$/OUTC1$_0$/ISTxD1/BE1$_{OUT}$		
119		P0$_3$					AN0$_3$	D$_3$
120		P0$_2$					AN0$_2$	D$_2$
121		P0$_1$					AN0$_1$	D$_1$
122		P0$_0$					AN0$_0$	D$_0$
123		P15$_7$					AN15$_7$	
124		P15$_6$					AN15$_6$	
125		P15$_5$					AN15$_5$	
126		P15$_4$					AN15$_4$	
127		P15$_3$					AN15$_3$	
128		P15$_2$				ISRxD0	AN15$_2$	
129		P15$_1$				ISCLK0	AN15$_1$	
130	V$_{SS}$							
131		P15$_0$				ISTxD0	AN15$_0$	
132	V$_{CC1}$							
133		P10$_7$	$\overline{\text{KI}_3}$				AN$_7$	
134		P10$_6$	$\overline{\text{KI}_2}$				AN$_6$	
135		P10$_5$	$\overline{\text{KI}_1}$				AN$_5$	
136		P10$_4$	$\overline{\text{KI}_0}$				AN$_4$	
137		P10$_3$					AN$_3$	
138		P10$_2$					AN$_2$	
139		P10$_1$					AN$_1$	
140	AV$_{SS}$							
141		P10$_0$					AN$_0$	
142	V$_{REF}$							
143	AV$_{CC}$							
144		P9$_7$			RxD4/SCL4/STxD4		$\overline{\text{AD}_{TRG}}$	

NOTES:
1. Bus control pins in M32C/84T cannot be used.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.

The register bank is comprised of 8 registers (R0, R1, R2, R3, A0, A1, SB and FB) out of 28 CPU registers. Two sets of register banks are provided.



NOTES:
1. The register bank is comprised of these registers. Two sets of register banks are provided.

Figure 2.1 CPU Register

Address	Register	Symbol	Value after RESET
009016	UART0 Transmit /NACK Interrupt Control Register	S0TIC	XXXX X0002
009116	UART1/UART4 Bus Conflict Detect Interrupt Control Register	BCN1IC/BCN4IC	XXXX X0002
009216	UART1 Transmit/NACK Interrupt Control Register	S1TIC	XXXX X0002
009316	Key Input Interrupt Control Register	KUPIC	XXXX X0002
009416	Timer B0 Interrupt Control Register	TB0IC	XXXX X0002
009516	Intelligent I/O Interrupt Control Register 1	IIO1IC	XXXX X0002
009616	Timer B2 Interrupt Control Register	TB2IC	XXXX X0002
009716	Intelligent I/O Interrupt Control Register 3	IIO3IC	XXXX X0002
009816	Timer B4 Interrupt Control Register	TB4IC	XXXX X0002
009916			
009A16	INT4 Interrupt Control Register	INT4IC	XX00 X0002
009B16			
009C16	INT2 Interrupt Control Register	INT2IC	XX00 X0002
009D16	Intelligent I/O Interrupt Control Register 9/ CAN Interrupt 0 Control Register	IIO9IC CAN0IC	XXXX X0002
009E16	INT0 Interrupt Control Register	INT0IC	XX00 X0002
009F16	Exit Priority Control Register	RLVL	XXXX 00002
00A016	Interrupt Request Register 0	IIO0IR	0000 000X2
00A116	Interrupt Request Register 1	IIO1IR	0000 000X2
00A216	Interrupt Request Register 2	IIO2IR	0000 000X2
00A316	Interrupt Request Register 3	IIO3IR	0000 000X2
00A416	Interrupt Request Register 4	IIO4IR	0000 000X2
00A516			
00A616			
00A716			
00A816	Interrupt Request Register 8	IIO8IR	0000 000X2
00A916	Interrupt Request Register 9	IIO9IR	0000 000X2
00AA16	Interrupt Request Register 10	IIO10IR	0000 000X2
00AB16	Interrupt Request Register 11	IIO11IR	0000 000X2
00AC16			
00AD16			
00AE16			
00AF16			
00B016	Interrupt Enable Register 0	IIO0IE	0016
00B116	Interrupt Enable Register 1	IIO1IE	0016
00B216	Interrupt Enable Register 2	IIO2IE	0016
00B316	Interrupt Enable Register 3	IIO3IE	0016
00B416	Interrupt Enable Register 4	IIO4IE	0016
00B516			
00B616			
00B716			
00B816	Interrupt Enable Register 8	IIO8IE	0016
00B916	Interrupt Enable Register 9	IIO9IE	0016
00BA16	Interrupt Enable Register 10	IIO10IE	0016
00BB16	Interrupt Enable Register 11	IIO11IE	0016
00BC16			
00BD16			
00BE16			
00BF16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00C0₁₆			
00C1₁₆			
00C2₁₆			
00C3₁₆			
00C4₁₆			
00C5₁₆			
00C6₁₆			
00C7₁₆			
00C8₁₆			
00C9₁₆			
00CA₁₆			
00CB₁₆			
00CC₁₆			
00CD₁₆			
00CE₁₆			
00CF₁₆			
00D0₁₆			
00D1₁₆			
00D2₁₆			
00D3₁₆			
00D4₁₆			
00D5₁₆			
00D6₁₆			
00D7₁₆			
00D8₁₆			
00D9₁₆			
00DA₁₆			
00DB₁₆			
00DC₁₆			
00DD₁₆			
00DE₁₆			
00DF₁₆			
00E0₁₆			
00E1₁₆			
00E2₁₆			
00E3₁₆			
00E4₁₆			
00E5₁₆			
00E6₁₆			
00E7₁₆			
00E8₁₆ 00E9₁₆	SI/O Receive Buffer Register 0	G0RB	XXXX XXXX₂ X000 XXXX₂
00EA₁₆	Transmit Buffer/Receive Data Register 0	G0TB/G0DR	XX₁₆
00EB₁₆			
00EC₁₆	Receive Input Register 0	G0RI	XX₁₆
00ED₁₆	SI/O Communication Mode Register 0	G0MR	00₁₆
00EE₁₆	Transmit Output Register 0	G0TO	XX₁₆
00EF₁₆	SI/O Communication Control Register 0	G0CR	0000 X011₂

X: Indeterminate

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Address	Register	Symbol	Value after RESET
012016	Base Timer Register 1	G1BT	XX16
012116			XX16
012216	Base Timer Control Register 10	G1BCR0	0016
012316	Base Timer Control Register 11	G1BCR1	X000 000X2
012416	Time Measurement Prescaler Register 16	G1TPR6	0016
012516	Time Measurement Prescaler Register 17	G1TPR7	0016
012616	Function Enable Register 1	G1FE	0016
012716	Function Select Register 1	G1FS	0016
012816	SI/O Receive Buffer Register 1	G1RB	XXXX XXXX2
012916			X000 XXXX2
012A16	Transmit Buffer/Receive Data Register 1	G1TB/G1DR	XX16
012B16			
012C16	Receive Input Register 1	G1RI	XX16
012D16	SI/O Communication Mode Register 1	G1MR	0016
012E16	Transmit Output Register 1	G1TO	XX16
012F16	SI/O Communication Control Register 1	G1CR	0000 X0112
013016	Data Compare Register 10	G1CMP0	XX16
013116	Data Compare Register 11	G1CMP1	XX16
013216	Data Compare Register 12	G1CMP2	XX16
013316	Data Compare Register 13	G1CMP3	XX16
013416	Data Mask Register 10	G1MSK0	XX16
013516	Data Mask Register 11	G1MSK1	XX16
013616			
013716			
013816	Receive CRC Code Register 1	G1RCRC	XX16
013916			XX16
013A16	Transmit CRC Code Register 1	G1TCRC	0016
013B16			0016
013C16	SI/O Extended Mode Register 1	G1EMR	0016
013D16	SI/O Extended Receive Control Register 1	G1ERC	0016
013E16	SI/O Special Communication Interrupt Detect Register 1	G1IRF	0016
013F16	SI/O Extended Transmit Control Register 1	G1ETC	0000 0XXX2
014016			
014116			
014216			
014316			
014416			
014516			
014616			
014716			
014816			
014916			
014A16			
014B16			
014C16			
014D16			
014E16			
014F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
021016 021116	CAN0 Slot Interrupt Mask Register	C0SIMKR	0016(2) 0016(2)
021216			
021316			
021416	CAN0 Error Interrupt Mask Register	C0EIMKR	XXXX X0002(2)
021516	CAN0 Error Interrupt Status Register	C0EISTR	XXXX X0002(2)
021616	CAN0 Error Cause Register	C0EFR	0016(2)
021716	CAN0 Baud Rate Prescaler	C0BRP	0000 00012(2)
021816			
021916	CAN0 Mode Register	C0MDR	XXXX XX002(2)
021A16			
021B16			
021C16			
021D16			
021E16			
021F16			
022016 022116	CAN0 Single-Shot Control Register	C0SSCTLR	0016(2) 0016(2)
022216			
022316			
022416 022516	CAN0 Single-Shot Status Register	C0SSSTR	0016(2) 0016(2)
022616			
022716			
022816	CAN0 Global Mask Register Standard ID0	C0GMR0	XXX0 00002(2)
022916	CAN0 Global Mask Register Standard ID1	C0GMR1	XX00 00002(2)
022A16	CAN0 Global Mask Register Extended ID0	C0GMR2	XXXX 00002(2)
022B16	CAN0 Global Mask Register Extended ID1	C0GMR3	0016(2)
022C16	CAN0 Global Mask Register Extended ID2	C0GMR4	XX00 00002(2)
022D16			
022E16			
022F16			
023016	CAN0 Message Slot 0 Control Register / CAN0 Local Mask Register A Standard ID0	C0MCTL0/ C0LMAR0	0000 00002(2) XXX0 00002(2)
023116	CAN0 Message Slot 1 Control Register / CAN0 Local Mask Register A Standard ID1	C0MCTL1/ C0LMAR1	0000 00002(2) XX00 00002(2)
023216	CAN0 Message Slot 2 Control Register / CAN0 Local Mask Register A Extended ID0	C0MCTL2/ C0LMAR2	0000 00002(2) XXXX 00002(2)
023316	CAN0 Message Slot 3 Control Register / CAN0 local Mask Register A Extended ID1	C0MCTL3/ C0LMAR3	0016(2) 0016(2)
023416	CAN0 Message Slot 4 Control Register / CAN0 Local Mask Register A Extended ID2	C0MCTL4/ C0LMAR4	0000 00002(2) XX00 00002(2)
023516	CAN0 Message Slot 5 Control Register	C0MCTL5	0016(2)
023616	CAN0 Message Slot 6 Control Register	C0MCTL6	0016(2)
023716	CAN0 Message Slot 7 Control Register	C0MCTL7	0016(2)
023816	CAN0 Message Slot 8 Control Register / CAN0 Local Mask Register B Standard ID0	C0MCTL8/ C0LMBR0	0000 00002(2) XXX0 00002(2)

(Note 1)

X: Indeterminate

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NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 022016 to 023F16.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and supplying the clock to the CAN module.

Address	Register	Symbol	Value after RESET
02C0$_{16}$ 02C1$_{16}$	X0 Register Y0 Register	X0R,Y0R	XX$_{16}$ XX$_{16}$
02C2$_{16}$ 02C3$_{16}$	X1 Register Y1 Register	X1R,Y1R	XX$_{16}$ XX$_{16}$
02C4$_{16}$ 02C5$_{16}$	X2 Register Y2 Register	X2R,Y2R	XX$_{16}$ XX$_{16}$
02C6$_{16}$ 02C7$_{16}$	X3 Register Y3 Register	X3R,Y3R	XX$_{16}$ XX$_{16}$
02C8$_{16}$ 02C9$_{16}$	X4 Register Y4 Register	X4R,Y4R	XX$_{16}$ XX$_{16}$
02CA$_{16}$ 02CB$_{16}$	X5 Register Y5 Register	X5R,Y5R	XX$_{16}$ XX$_{16}$
02CC$_{16}$ 02CD$_{16}$	X6 Register Y6 Register	X6R,Y6R	XX$_{16}$ XX$_{16}$
02CE$_{16}$ 02CF$_{16}$	X7 Register Y7 Register	X7R,Y7R	XX$_{16}$ XX$_{16}$
02D0$_{16}$ 02D1$_{16}$	X8 Register Y8 Register	X8R,Y8R	XX$_{16}$ XX$_{16}$
02D2$_{16}$ 02D3$_{16}$	X9 Register Y9 Register	X9R,Y9R	XX$_{16}$ XX$_{16}$
02D4$_{16}$ 02D5$_{16}$	X10 Register Y10 Register	X10R,Y10R	XX$_{16}$ XX$_{16}$
02D6$_{16}$ 02D7$_{16}$	X11 Register Y11 Register	X11R,Y11R	XX$_{16}$ XX$_{16}$
02D8$_{16}$ 02D9$_{16}$	X12 Register Y12 Register	X12R,Y12R	XX$_{16}$ XX$_{16}$
02DA$_{16}$ 02DB$_{16}$	X13 Register Y13 Register	X13R,Y13R	XX$_{16}$ XX$_{16}$
02DC$_{16}$ 02DD$_{16}$	X14 Register Y14 Register	X14R,Y14R	XX$_{16}$ XX$_{16}$
02DE$_{16}$ 02DF$_{16}$	X15 Register Y15 Register	X15R,Y15R	XX$_{16}$ XX$_{16}$
02E0$_{16}$	X/Y Control Register	XYC	XXXX XX00$_2$
02E1$_{16}$			
02E2$_{16}$			
02E3$_{16}$			
02E4$_{16}$	UART1 Special Mode Register 4	U1SMR4	00$_{16}$
02E5$_{16}$	UART1 Special Mode Register 3	U1SMR3	00$_{16}$
02E6$_{16}$	UART1 Special Mode Register 2	U1SMR2	00$_{16}$
02E7$_{16}$	UART1 Special Mode Register	U1SMR	00$_{16}$
02E8$_{16}$	UART1 Transmit/Receive Mode Register	U1MR	00$_{16}$
02E9$_{16}$	UART1 Bit Rate Register	U1BRG	XX$_{16}$
02EA$_{16}$ 02EB$_{16}$	UART1 Transmit Buffer Register	U1TB	XX$_{16}$ XX$_{16}$
02EC$_{16}$	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000$_2$
02ED$_{16}$	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010$_2$
02EE$_{16}$ 02EF$_{16}$	UART1 Receive Buffer Register	U1RB	XX$_{16}$ XX$_{16}$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
02F0₁₆			
02F1₁₆			
02F2₁₆			
02F3₁₆			
02F4₁₆	UART4 Special Mode Register 4	U4SMR4	00₁₆
02F5₁₆	UART4 Special Mode Register 3	U4SMR3	00₁₆
02F6₁₆	UART4 Special Mode Register 2	U4SMR2	00₁₆
02F7₁₆	UART4 Special Mode Register	U4SMR	00₁₆
02F8₁₆	UART4 Transmit/Receive Mode Register	U4MR	00₁₆
02F9₁₆	UART4 Bit Rate Register	U4BRG	XX₁₆
02FA₁₆	UART4 Transmit Buffer Register	U4TB	XX₁₆
02FB₁₆			XX₁₆
02FC₁₆	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000₂
02FD₁₆	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010₂
02FE₁₆	UART4 Receive Buffer Register	U4RB	XX₁₆
02FF₁₆			XX₁₆
0300₁₆	Timer B3, B4, B5 Count Start Flag	TBSR	000X XXXX₂
0301₁₆			
0302₁₆	Timer A1-1 Register	TA11	XX₁₆
0303₁₆			XX₁₆
0304₁₆	Timer A2-1 Register	TA21	XX₁₆
0305₁₆			XX₁₆
0306₁₆	Timer A4-1 Register	TA41	XX₁₆
0307₁₆			XX₁₆
0308₁₆	Three-Phase PWM Control Register 0	INVC0	00₁₆
0309₁₆	Three-Phase PWM Control Register 1	INVC1	00₁₆
030A₁₆	Three-Phase Output Buffer Register 0	IDB0	XX11 1111₂
030B₁₆	Three-Phase Output Buffer Register 1	IDB1	XX11 1111₂
030C₁₆	Dead Time Timer	DTT	XX₁₆
030D₁₆	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XX₁₆
030E₁₆			
030F₁₆			
0310₁₆	Timer B3 Register	TB3	XX₁₆
0311₁₆			XX₁₆
0312₁₆	Timer B4 Register	TB4	XX₁₆
0313₁₆			XX₁₆
0314₁₆	Timer B5 Register	TB5	XX₁₆
0315₁₆			XX₁₆
0316₁₆			
0317₁₆			
0318₁₆			
0319₁₆			
031A₁₆			
031B₁₆	Timer B3 Mode Register	TB3MR	00XX 0000₂
031C₁₆	Timer B4 Mode Register	TB4MR	00XX 0000₂
031D₁₆	Timer B5 Mode Register	TB5MR	00XX 0000₂
031E₁₆			
031F₁₆	External Interrupt Cause Select Register	IFSR	00₁₆

X: Indeterminate

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<100-pin Package>

Address	Register	Symbol	Value after RESET
03D0$_{16}$			
03D1$_{16}$			
03D2$_{16}$	Set default value to "FF$_{16}$"		
03D3$_{16}$	Set default value to "FF$_{16}$"		
03D4$_{16}$			
03D5$_{16}$			
03D6$_{16}$			
03D7$_{16}$			
03D8$_{16}$			
03D9$_{16}$			
03DA$_{16}$	Pull-Up Control Register 2	PUR2	00$_{16}$
03DB$_{16}$	Pull-Up Control Register 3	PUR3	00$_{16}$
03DC$_{16}$	Set default value to "00$_{16}$"		
03DD$_{16}$			
03DE$_{16}$			
03DF$_{16}$			
03E0$_{16}$	Port P0 Register	P0	XX$_{16}$
03E1$_{16}$	Port P1 Register	P1	XX$_{16}$
03E2$_{16}$	Port P0 Direction Register	PD0	00$_{16}$
03E3$_{16}$	Port P1 Direction Register	PD1	00$_{16}$
03E4$_{16}$	Port P2 Register	P2	XX$_{16}$
03E5$_{16}$	Port P3 Register	P3	XX$_{16}$
03E6$_{16}$	Port P2 Direction Register	PD2	00$_{16}$
03E7$_{16}$	Port P3 Direction Register	PD3	00$_{16}$
03E8$_{16}$	Port P4 Register	P4	XX$_{16}$
03E9$_{16}$	Port P5 Register	P5	XX$_{16}$
03EA$_{16}$	Port P4 Direction Register	PD4	00$_{16}$
03EB$_{16}$	Port P5 Direction Register	PD5	00$_{16}$
03EC$_{16}$			
03ED$_{16}$			
03EE$_{16}$			
03EF$_{16}$			
03F0$_{16}$	Pull-up Control Register 0	PUR0	00$_{16}$
03F1$_{16}$	Pull-up Control Register 1	PUR1	XXXX 0000$_{2}$
03F2$_{16}$			
03F3$_{16}$			
03F4$_{16}$			
03F5$_{16}$			
03F6$_{16}$			
03F7$_{16}$			
03F8$_{16}$			
03F9$_{16}$			
03FA$_{16}$			
03FB$_{16}$			
03FC$_{16}$			
03FD$_{16}$			
03FE$_{16}$			
03FF$_{16}$	Port Control Register	PCR	XXXX XXX0$_{2}$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

$V_{CC1}=V_{CC2}=5V$

Table 5.4 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=AV_{CC}=V_{REF}$=4.2 to 5.5V, V_{SS}= AV_{SS} = 0V at Topr=–20 to 85°C, f(BCLK) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
-	Resolution	$V_{REF}=V_{CC1}$				10	Bits
INL	Integral Nonlinearity Error	$V_{REF}=V_{CC1}=V_{CC2}$=5V	AN_0 to AN_7, $AN0_0$ to $AN0_7$, $AN2_0$ to $AN2_7$, $AN15_0$ to $AN15_7$, ANEX0, ANEX1			±3	LSB
							LSB
			External op-amp connection mode			±7	LSB
							LSB
DNL	Differential Nonlinearity Error					±1	LSB
-	Offset Error					±3	LSB
-	Gain Error					±3	LSB
R_{LADDER}	Resistor Ladder	$V_{REF}=V_{CC1}$		8		40	kΩ
t_{CONV}	10-bit Conversion Time(1, 2)			2.06			µs
t_{CONV}	8-bit Conversion Time(1, 2)			1.75			µs
t_{SAMP}	Sampling Time(1)			0.188			µs
V_{REF}	Reference Voltage			2		V_{CC1}	V
V_{IA}	Analog Input Voltage			0		V_{REF}	V

NOTES:
1. Divide f(X_{IN}), if exceeding 16 MHz, to keep ϕAD frequency at 16 MHz or less.
2. With using the sample and hold function.

Table 5.5 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=V_{REF}$=4.2 to 5.5V, $V_{SS}=AV_{SS}$=0V at Topr=–20 to 85°C, f(BCLK) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTES:
1. Measurement when using one D/A converter. The DAi register (i=0, 1) of the D/A converter, not being used, is set to "00_{16}". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr=–20 to 85°C unless otherwise specified)

Table 5.11 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	100		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	40		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	40		ns

Table 5.12 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	400		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	200		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	200		ns

Table 5.13 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	200		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 5.14 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 5.15 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAiOUT Input High ("H") Width	1000		ns
$t_{w(UPL)}$	TAiOUT Input Low ("L") Width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAiOUT Input Hold Time	400		ns

$V_{CC1}=V_{CC2}=5V$

Switching Characteristics

(V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.23 Memory Expansion Mode and Microprocessor Mode

(when accessing an external memory space with the multiplexed bus)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address Output Delay Time	See Figure 5.2		18	ns
th(BCLK-AD)	Address Output Hold Time (BCLK standard)		-3		ns
th(RD-AD)	Address Output Hold Time (RD standard)(5)		(Note 1)		ns
th(WR-AD)	Address Output Hold Time (WR standard)(5)		(Note 1)		ns
td(BCLK-CS)	Chip-Select Signal Output Delay Time			18	ns
th(BCLK-CS)	Chip-Select Signal Output Hold Time (BCLK standard)		-3		ns
th(RD-CS)	Chip-Select Signal Output Hold Time (RD standard)(5)		(Note 1)		ns
th(WR-CS)	Chip-Select Signal Output Hold Time (WR standard)(5)		(Note 1)		ns
td(BCLK-RD)	RD Signal Output Delay Time			18	ns
th(BCLK-RD)	RD Signal Output Hold Time		-5		ns
td(BCLK-WR)	WR Signal Output Delay Time			18	ns
th(BCLK-WR)	WR Signal Output Hold Time		-5		ns
td(DB-WR)	Data Output Delay Time (WR standard)		(Note 2)		ns
th(WR-DB)	Data Output Hold Time (WR standard)(5)		(Note 1)		ns
td(BCLK-ALE)	ALE Signal Output Delay Time (BCLK standard)			18	ns
th(BCLK-ALE)	ALE Signal Output Hold Time (BCLK standard)		-2		ns
td(AD-ALE)	ALE Signal Output Delay Time (address standard)		(Note 3)		ns
th(ALE-AD)	ALE Signal Output Hold Time (address standard)		(Note 4)		ns
tdz(RD-AD)	Address Output Float Start Time			8	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$th(RD-AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR-AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(RD-CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR-CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR-DB) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycle.

$$td(DB-WR) = \frac{10^9 \times m}{f(BCLK) \times 2} - 25 \quad [ns]$$ (if external bus cycle is aϕ + bϕ, m= (bx2)-1)

3. Values can be obtained from the following equations, according to BCLK frequency and external bus cycle.

$$td(AD-ALE) = \frac{10^9 \times n}{f(BCLK) \times 2} - 20 \quad [ns]$$ (if external bus cycle is aϕ + bϕ, n= a)

4. Values can be obtained from the following equations, according to BCLK frequency and external bus cycle.

$$th(ALE-AD) = \frac{10^9 \times n}{f(BCLK) \times 2} - 10 \quad [ns]$$ (if external bus cycle is aϕ + bϕ, n= a)

5. *tc* ns is added when recovery cycle is inserted.

$V_{CC1}=V_{CC2}=3.3V$

Timing Requirements

($V_{CC1}=V_{CC2}$= 3.0 to 3.6V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.27 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External Clock Input Cycle Time	41		ns
$t_{w(H)}$	External Clock Input High ("H") Width	18		ns
$t_{w(L)}$	External Clock Input Low ("L") Width	18		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

Table 5.28 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data Input Access Time (RD standard)		(Note 1)	ns
$t_{ac1(AD-DB)}$	Data Input Access Time (AD standard, CS standard)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{ac2(AD-DB)}$	Data Input Access Time (AD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{su(DB-BCLK)}$	Data Input Setup Time	30		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ Input Setup Time	40		ns
$t_{su(HOLD-BCLK)}$	$\overline{HOLD}$ Input Setup Time	60		ns
$t_{h(RD-DB)}$	Data Input Hold Time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ Input Hold Time	0		ns
$t_{h(BCLK-HOLD)}$	$\overline{HOLD}$ Input Hold Time	0		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ Output Delay Time		25	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequecncy and external bus cycles. Insert a wait state or lower the operation frequency, $f_{(BCLK)}$, if the calculated value is negative.

$$t_{ac1(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad \text{[ns] (if external bus cycle is a}\phi + \text{b}\phi\text{, m=(bx2)+1)}$$

$$t_{ac1(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)}} - 35 \quad \text{[ns] (if external bus cycle is a}\phi + \text{b}\phi\text{, n=a+b)}$$

$$t_{ac2(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad \text{[ns] (if external bus cycle is a}\phi + \text{b}\phi\text{, m=(bx2)-1)}$$

$$t_{ac2(AD-DB)} = \frac{10^9 \times p}{f_{(BCLK)} \times 2} - 35 \quad \text{[ns] (if external bus cycle is a}\phi + \text{b}\phi\text{, p=\{(a+b-1)x2\}+1)}$$

$V_{CC1}=V_{CC2}=3.3V$

Timing Requirements

($V_{CC1}=V_{CC2}$= 3.0 to 3.6V, V_{SS}= 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.29 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	100		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	40		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	40		ns

Table 5.30 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	400		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	200		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	200		ns

Table 5.31 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	200		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	100		ns

Table 5.32 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	100		ns

Table 5.33 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAi_{OUT} Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAi_{OUT} Input High ("H") Width	1000		ns
$t_{w(UPL)}$	TAi_{OUT} Input Low ("L") Width	1000		ns
$t_{su(UP-TIN)}$	TAi_{OUT} Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAi_{OUT} Input Hold Time	400		ns

Table 5.43 Recommended Operating Conditions

(V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS}=0V at Topr = -40 to 85°C (T version) unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V_{CC1}, V_{CC2}	Supply Voltage (V_{CC1}≥ V_{CC2})		4.2	5.0	5.5	V
AVcc	Analog Supply Voltage			V_{CC1}		V
Vss	Supply Voltage			0		V
AVss	Analog Supply Voltage			0		V
V_{IH}	Input High ("H") Voltage	$P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$(4)	0.8V_{CC2}		V_{CC2}	V
		$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4), X_{IN}, $\overline{RESET}$, CNVss, BYTE	0.8V_{CC1}		V_{CC1}	
		$P7_0$, $P7_1$	0.8V_{CC1}		6.0	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$	0.8V_{CC2}		V_{CC2}	
V_{IL}	Input Low ("L") Voltage	$P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$(4)	0		0.2V_{CC2}	V
		$P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4), X_{IN}, $\overline{RESET}$, CNVss, BYTE	0		0.2V_{CC1}	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$	0		0.2V_{CC2}	
$I_{OH(peak)}$	Peak Output High ("H") Current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			-10.0	mA
$I_{OH(avg)}$	Average Output High ("H") Current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			-5.0	mA
$I_{OL(peak)}$	Peak Output Low ("L") Current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			10.0	mA
$I_{OL(avg)}$	Average Output Low ("L") Current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			5.0	mA

NOTES:

1. Typical values when average output current is 100ms.
2. Total $I_{OL(peak)}$ for P0, P1, P2, $P8_6$, $P8_7$, P9, P10, P11, P14 and P15 must be 80mA or less.
   Total $I_{OL(peak)}$ for P3, P4, P5, P6, P7, $P8_0$ to $P8_4$, P12 and P13 must be 80mA or less.
   Total $I_{OH(peak)}$ for P0, P1, P2, and P11 must be -40mA or less.
   Total $I_{OH(peak)}$ for $P8_6$, $P8_7$, P9, P10, P14 and P15 must be -40mA or less.
   Total $I_{OH(peak)}$ for P3, P4, P5, P12 and P13 must be -40mA or less.
   Total $I_{OH(peak)}$ for P6, P7, and $P8_0$ to $P8_4$ must be -40mA or less.
3. V_{IH} and V_{IL} reference for $P8_7$ applies when $P8_7$ is used as a programmable input port.
   It does not apply when $P8_7$ is used as X_{CIN}.
4. P11 to P15 are provided in the 144-pin package only.

$V_{CC1}=V_{CC2}=5V$

Table 5.47 Flash Memory Version Electrical Characteristics

(V_{CC1}=4.5 to 5.5V, 3.3 to 3.6V at Topr= 0 to 60°C unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
-	Program and Erase Endurance(2)		100			cycles
-	Word Program Time (V_{CC1}=5.0V, Topr=25° C)			25	200	µs
-	Lock Bit Program Time			25	200	µs
-	Block Erase Time (V_{CC1}=5.0V, Topr=25° C)	4-Kbyte Block		0.3	4	s
		8-Kbyte Block		0.3	4	s
		32-Kbyte Block		0.5	4	s
		64-Kbyte Block		0.8	4	s
-	All-Unlocked-Block Erase Time(1)				4 x *n*	s
t_{PS}	Wait Time to Stabilize Flash Memory Circuit				15	µs
-	Data Hold Time (Topr=-40 to 85 ° C)		10			years

NOTES:
1. *n* denotes the number of block to be erased.
2. Number of program-erase cycles per block.
   If Program and Erase Endurance is *n* cycle (*n*=100), each block can be erased and programmed *n* cycles. For example, if a 4-Kbyte block A is erased after programming a word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data can not be programmed to the same address more than once without erasing the block. (rewrite prohibited).

Table 5.48 Power Supply Timing

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Wait Time to Stabilize Internal Supply Voltage when Power-on	V_{CC1}=3.0 to 5.5V			2	ms

$t_{d(P-R)}$
Wait Time to Stabilize Internal Supply Voltage when Power-on

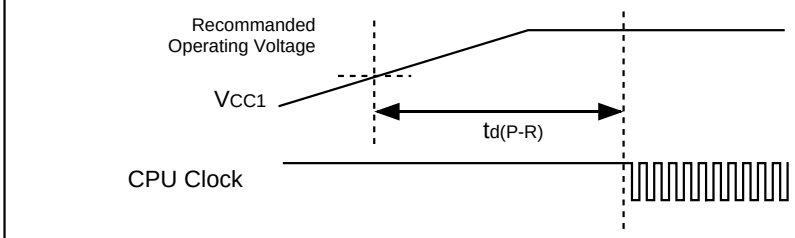


Figure 5.11 Power Supply Timing Diagram

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr= -40 to 85°C (T version) unless otherwise specified)

Table 5.50 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	100		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	40		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	40		ns

Table 5.51 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	400		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	200		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	200		ns

Table 5.52 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	200		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	100		ns

Table 5.53 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	100		ns

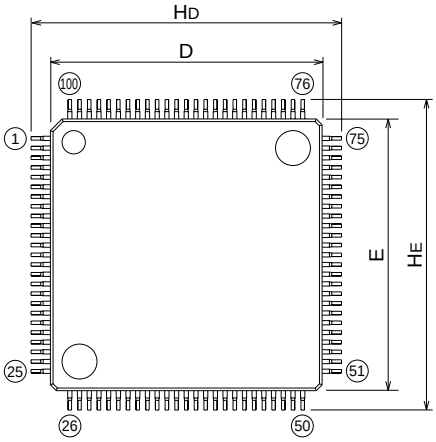
Table 5.54 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

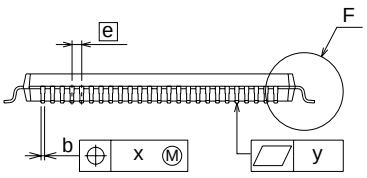
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAi_{OUT} Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAi_{OUT} Input High ("H") Width	1000		ns
$t_{w(UPL)}$	TAi_{OUT} Input Low ("L") Width	1000		ns
$t_{su(UP-TIN)}$	TAi_{OUT} Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAi_{OUT} Input Hold Time	400		ns

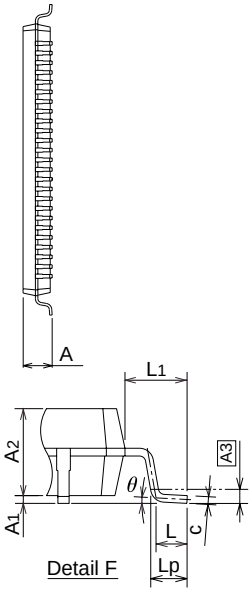
PLQP0100KB-A (100P6Q-A)

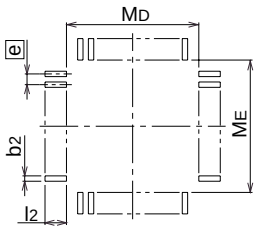
Plastic 100pin 14×14mm body LQFP

JEITA Package Code	RENESAS Code	Previous Code	Mass[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A	0.6g









Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	13.9	14.0	14.1
e	–	0.5	–
HD	15.8	16.0	16.2
HE	15.8	16.0	16.2
L	0.3	0.5	0.7
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	10°
b2	–	0.225	–
l2	0.9	–	–
MD	–	14.4	–
ME	–	14.4	–