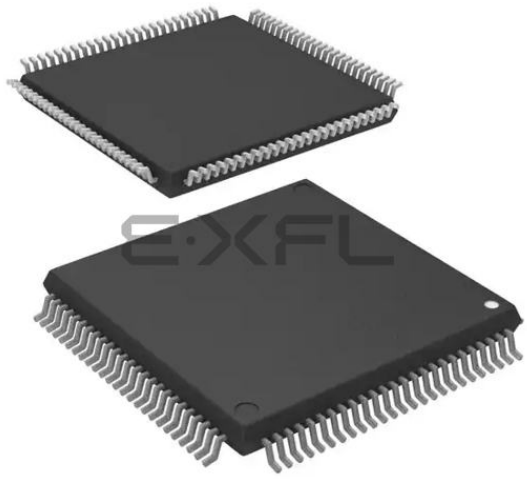
Renesas Electronics America Inc - M30843FWGP#U5 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	85
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30843fwgp-u5

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

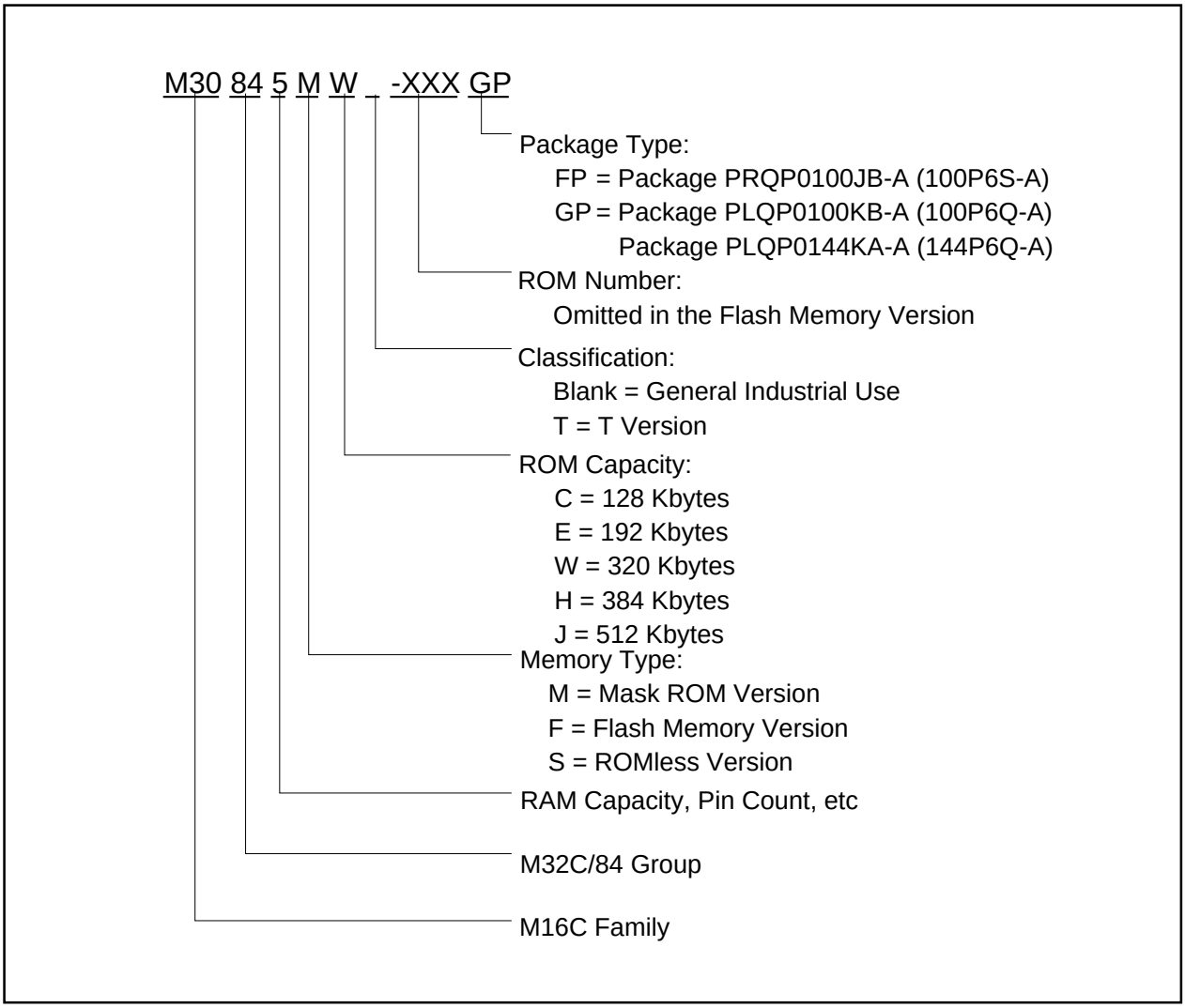
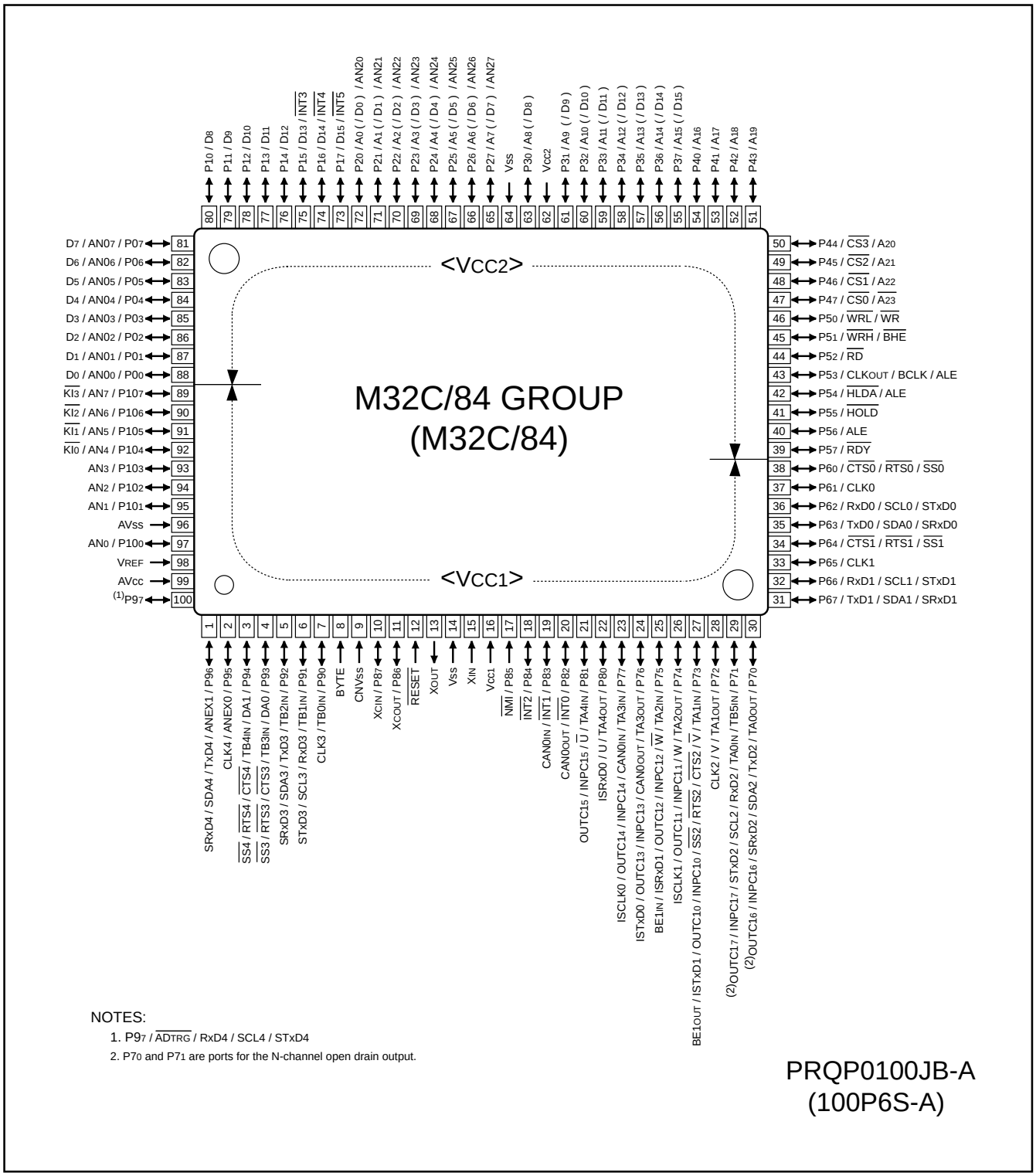


Figure 1.2 Product Numbering System

Table 1.4 Pin Characteristics for 144-Pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin(1)
1		P9$_6$			TxD4/SDA4/SRxD4		ANEX1	
2		P9$_5$			CLK4		ANEX0	
3		P9$_4$		TB4$_{IN}$	$\overline{CTS4}$/$\overline{RTS4}$/$\overline{SS4}$		DA1	
4		P9$_3$		TB3$_{IN}$	$\overline{CTS3}$/$\overline{RTS3}$/$\overline{SS3}$		DA0	
5		P9$_2$		TB2$_{IN}$	TxD3/SDA3/SRxD3			
6		P9$_1$		TB1$_{IN}$	RxD3/SCL3/STxD3			
7		P9$_0$		TB0$_{IN}$	CLK3			
8		P14$_6$						
9		P14$_5$						
10		P14$_4$						
11		P14$_3$				INPC17/OUTC17		
12		P14$_2$				INPC16/OUTC16		
13		P14$_1$				INPC15/OUTC15		
14		P14$_0$				INPC14/OUTC14		
15	BYTE							
16	CNV$_{SS}$							
17	X$_{CIN}$	P8$_7$						
18	X$_{COUT}$	P8$_6$						
19	$\overline{RESET}$							
20	X$_{OUT}$							
21	V$_{SS}$							
22	X$_{IN}$							
23	V$_{CC1}$							
24		P8$_5$	$\overline{NMI}$					
25		P8$_4$	$\overline{INT2}$					
26		P8$_3$	$\overline{INT1}$		CAN0$_{IN}$			
27		P8$_2$	$\overline{INT0}$		CAN0$_{OUT}$			
28		P8$_1$		TA4$_{IN}$/$\overline{U}$		INPC15/OUTC15		
29		P8$_0$		TA4$_{OUT}$/U		ISRxD0		
30		P7$_7$		TA3$_{IN}$	CAN0$_{IN}$	INPC14/OUTC14/ISCLK0		
31		P7$_6$		TA3$_{OUT}$	CAN0$_{OUT}$	INPC13/OUTC13/ISTxD0		
32		P7$_5$		TA2$_{IN}$/$\overline{W}$		INPC12/OUTC12/ISRxD1/BE1$_{IN}$		
33		P7$_4$		TA2$_{OUT}$/W		INPC11/OUTC11/ISCLK1		
34		P7$_3$		TA1$_{IN}$/$\overline{V}$	$\overline{CTS2}$/$\overline{RTS2}$/$\overline{SS2}$	INPC10/OUTC10/ISTxD1/BE1$_{OUT}$		
35		P7$_2$		TA1$_{OUT}$/V	CLK2			
36		P7$_1$		TB5$_{IN}$/TA0$_{IN}$	RxD2/SCL2/STxD2	INPC17/OUTC17		
37		P7$_0$		TA0$_{OUT}$	TxD2/SDA2/SRxD2	INPC16/OUTC16		
38		P6$_7$			TxD1/SDA1/SRxD1			
39	V$_{CC1}$							
40		P6$_6$			RxD1/SCL1/STxD1			
41	V$_{SS}$							
42		P6$_5$			CLK1			
43		P6$_4$			$\overline{CTS1}$/$\overline{RTS1}$/$\overline{SS1}$			
44		P6$_3$			TxD0/SDA0/SRxD0			
45		P6$_2$			RxD0/SCL0/STxD0			
46		P6$_1$			CLK0			
47		P6$_0$			$\overline{CTS0}$/$\overline{RTS0}$/$\overline{SS0}$			
48		P13$_7$						

NOTES:
1. Bus control pins in M32C/84T cannot be used.



NOTES:
1. P97 / ADTRG / RxD4 / SCL4 / STxD4
2. P70 and P71 are ports for the N-channel open drain output.

PRQP0100JB-A
(100P6S-A)

Figure 1.4 Pin Assignment for 100-Pin Package

Table 1.6 Pin Description (144-Pin Package only) (Continued)

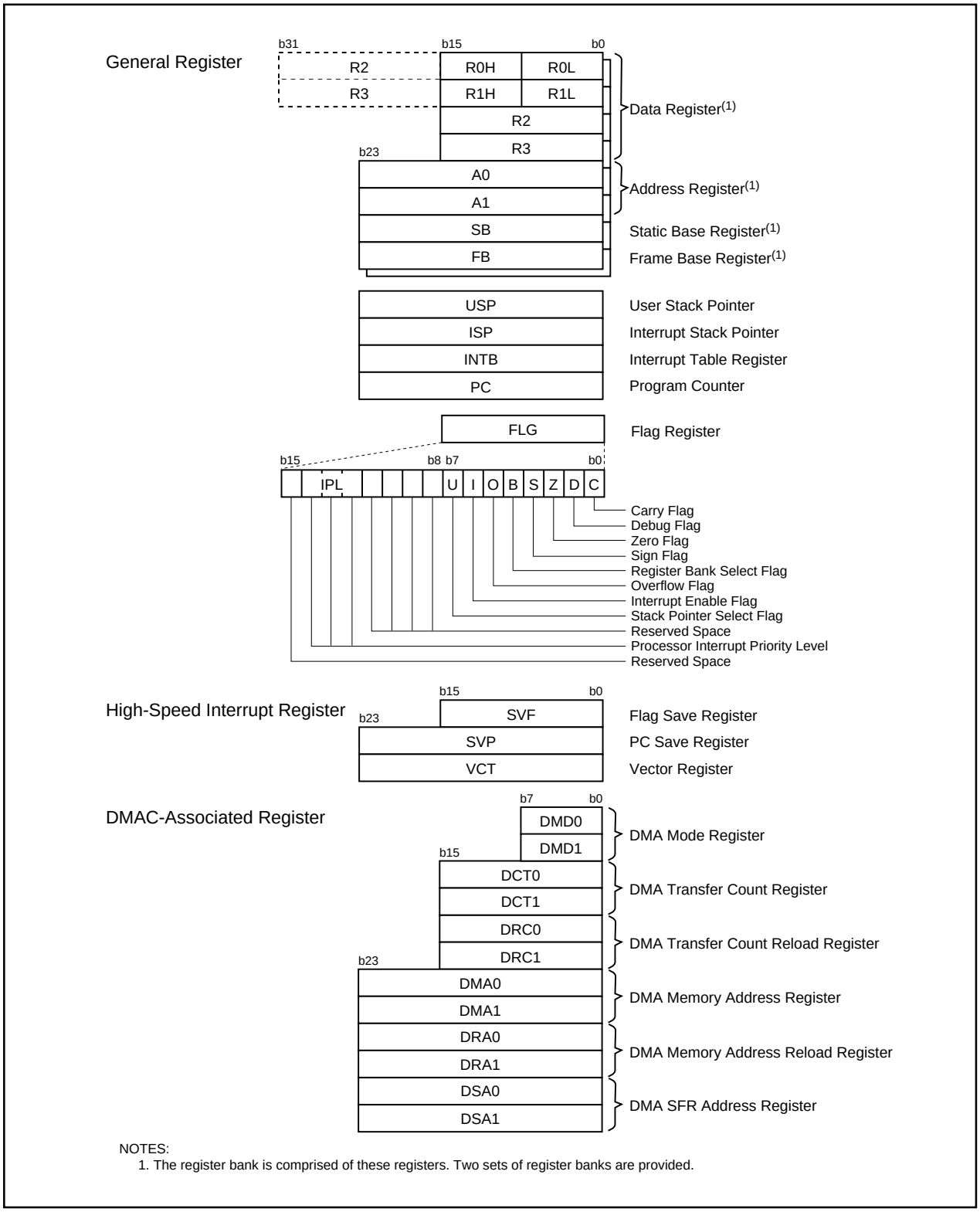
Classsfication	Symbol	I/O Type	Supply Voltage	Function
A/D Converter	$AN15_0$ to $AN15_7$	I	V_{CC1}	Analog input pins for the A/D converter
I/O Ports	$P11_0$ to $P11_4$ $P12_0$ to $P12_7$ $P13_0$ to $P13_7$	I/O	V_{CC2}	I/O ports having equivalent functions to P0
	$P14_0$ to $P14_6$ $P15_0$ to $P15_7$	I/O	V_{CC1}	I/O ports having equivalent functions to P0

I : Input O : Output I/O : Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.

The register bank is comprised of 8 registers (R0, R1, R2, R3, A0, A1, SB and FB) out of 28 CPU registers. Two sets of register banks are provided.



NOTES:
1. The register bank is comprised of these registers. Two sets of register banks are provided.

Figure 2.1 CPU Register

3. Memory

Figure 3.1 shows a memory map of the M32C/84 group (M32C/84, M32C/84T).

The M32C/84 group (M32C/84, M32C/84T) provides 16-Mbyte address space from addresses 000000$_{16}$ to FFFFFF$_{16}$.

The internal ROM is allocated lower addresses beginning with address FFFFFF$_{16}$. For example, a 64-Kbyte internal ROM is allocated in addresses FF0000$_{16}$ to FFFFFF$_{16}$.

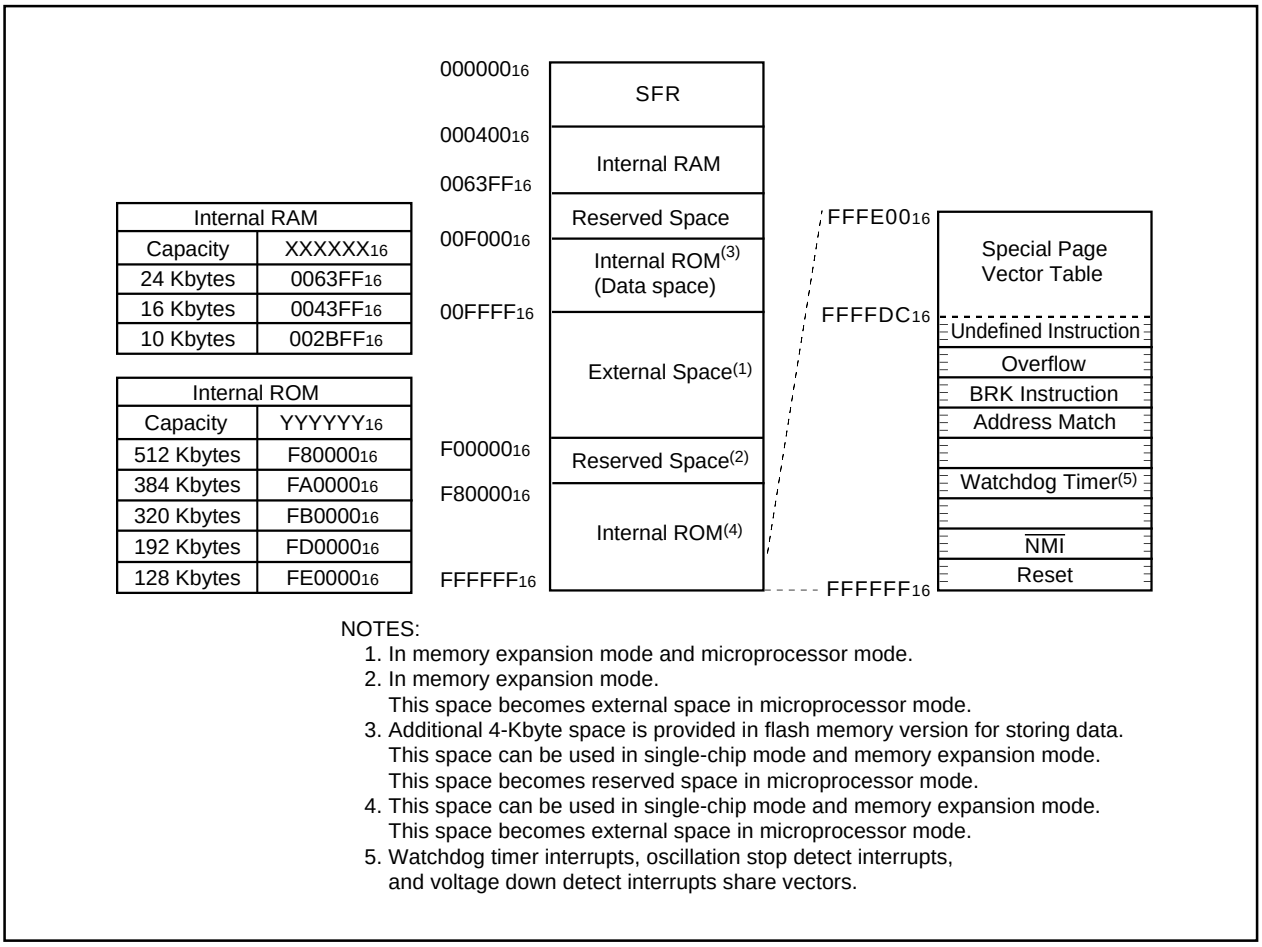
The fixed interrupt vectors are allocated addresses FFFFDC$_{16}$ to FFFFFF$_{16}$. It stores the starting address of each interrupt routine.

The internal RAM is allocated higher addresses beginning with address 000400$_{16}$. For example, a 10-Kbyte internal RAM is allocated addresses 000400$_{16}$ to 002BFF$_{16}$. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowleged.

SFR, consisting of control registers for peripheral functions such as I/O port, A/D converter, serial I/O, and timers, is allocated addresses 000000$_{16}$ to 0003FF$_{16}$. All blank spaces within SFR are reserved and cannot be accessed by users.

The special page vectors are allocated addresses FFFE00$_{16}$ to FFFFDB$_{16}$. It is used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **M32C/80 Series Software Manual** for details.

In memory expansion mode and microprocessor mode, some spaces are reserved and cannot be accessed by users.



Internal RAM	
Capacity	XXXXXX$_{16}$
24 Kbytes	0063FF$_{16}$
16 Kbytes	0043FF$_{16}$
10 Kbytes	002BFF$_{16}$

Internal ROM	
Capacity	YYYYYY$_{16}$
512 Kbytes	F80000$_{16}$
384 Kbytes	FA0000$_{16}$
320 Kbytes	FB0000$_{16}$
192 Kbytes	FD0000$_{16}$
128 Kbytes	FE0000$_{16}$

NOTES:
1. In memory expansion mode and microprocessor mode.
2. In memory expansion mode.
   This space becomes external space in microprocessor mode.
3. Additional 4-Kbyte space is provided in flash memory version for storing data.
   This space can be used in single-chip mode and memory expansion mode.
   This space becomes reserved space in microprocessor mode.
4. This space can be used in single-chip mode and memory expansion mode.
   This space becomes external space in microprocessor mode.
5. Watchdog timer interrupts, oscillation stop detect interrupts, and voltage down detect interrupts share vectors.

Figure 3.1 Memory Map

Address	Register	Symbol	Value after RESET
012016	Base Timer Register 1	G1BT	XX16
012116			XX16
012216	Base Timer Control Register 10	G1BCR0	0016
012316	Base Timer Control Register 11	G1BCR1	X000 000X2
012416	Time Measurement Prescaler Register 16	G1TPR6	0016
012516	Time Measurement Prescaler Register 17	G1TPR7	0016
012616	Function Enable Register 1	G1FE	0016
012716	Function Select Register 1	G1FS	0016
012816	SI/O Receive Buffer Register 1	G1RB	XXXX XXXX2
012916			X000 XXXX2
012A16	Transmit Buffer/Receive Data Register 1	G1TB/G1DR	XX16
012B16			
012C16	Receive Input Register 1	G1RI	XX16
012D16	SI/O Communication Mode Register 1	G1MR	0016
012E16	Transmit Output Register 1	G1TO	XX16
012F16	SI/O Communication Control Register 1	G1CR	0000 X0112
013016	Data Compare Register 10	G1CMP0	XX16
013116	Data Compare Register 11	G1CMP1	XX16
013216	Data Compare Register 12	G1CMP2	XX16
013316	Data Compare Register 13	G1CMP3	XX16
013416	Data Mask Register 10	G1MSK0	XX16
013516	Data Mask Register 11	G1MSK1	XX16
013616			
013716			
013816	Receive CRC Code Register 1	G1RCRC	XX16
013916			XX16
013A16	Transmit CRC Code Register 1	G1TCRC	0016
013B16			0016
013C16	SI/O Extended Mode Register 1	G1EMR	0016
013D16	SI/O Extended Receive Control Register 1	G1ERC	0016
013E16	SI/O Special Communication Interrupt Detect Register 1	G1IRF	0016
013F16	SI/O Extended Transmit Control Register 1	G1ETC	0000 0XXX2
014016			
014116			
014216			
014316			
014416			
014516			
014616			
014716			
014816			
014916			
014A16			
014B16			
014C16			
014D16			
014E16			
014F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0150₁₆			
0151₁₆			
0152₁₆			
0153₁₆			
0154₁₆			
0155₁₆			
0156₁₆			
0157₁₆			
0158₁₆			
0159₁₆			
015A₁₆			
015B₁₆			
015C₁₆			
015D₁₆			
015E₁₆			
015F₁₆			
0160₁₆			
0161₁₆			
0162₁₆			
0163₁₆			
0164₁₆			
0165₁₆			
0166₁₆			
0167₁₆			
0168₁₆			
0169₁₆			
016A₁₆			
016B₁₆			
016C₁₆			
016D₁₆			
016E₁₆			
016F₁₆			
0170₁₆			
0171₁₆			
0172₁₆			
0173₁₆			
0174₁₆			
0175₁₆			
0176₁₆			
0177₁₆			
0178₁₆	Input Function Select Register	IPS	00₁₆
0179₁₆	Input Function Select Register A	IPSA	00₁₆
017A₁₆			
017B₁₆			
017C₁₆			
017D₁₆ to 01DF₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
023916	CAN0 Message Slot 9 Control Register / CAN0 Local Mask Register B Standard ID1	C0MCTL9/ C0LMBR1	0000 00002(2) XX00 00002(2)
023A16	CAN0 Message Slot 10 Control Register / CAN0 Local Mask Register B Extended ID0	C0MCTL10/ C0LMBR2	0000 00002(2) XXXX 00002(2)
023B16	CAN0 Message Slot 11 Control Register / CAN0 Local Mask Register B Extended ID1	C0MCTL11/ C0LMBR3	0016(2) 0016(2)
023C16	CAN0 Message Slot 12 Control Register / CAN0 Local Mask Register B Extended ID2	C0MCTL12/ C0LMBR4	0000 00002(2) XX00 00002(2)
023D16	CAN0 Message Slot 13 Control Register	C0MCTL13	0016(2)
023E16	CAN0 Message Slot 14 Control Register	C0MCTL14	0016(2)
023F16	CAN0 Message Slot 15 Control Register	C0MCTL15	0016(2)
024016	CAN0 Slot Buffer Select Register	C0SBS	0016(2)
024116	CAN0 Control Register 1	C0CTLR1	X000 00XX2(2)
024216	CAN0 Sleep Control Register	C0SLPR	XXXX XXX02
024316			
024416 024516	CAN0 Acceptance Filter Support Register	C0AFS	0016(2) 0116(2)
024616			
024716			
024816			
024916			
024A16			
024B16			
024C16			
024D16			
024E16			
024F16			
025016			
025116			
025216			
025316			
025416			
025516			
025616			
025716			
025816			
025916			
025A16			
025B16			
025C16			
025D16 to 02BF16			

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 022016 to 023F16.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and supplying the clock to the CAN module.

Address	Register	Symbol	Value after RESET
02F0₁₆			
02F1₁₆			
02F2₁₆			
02F3₁₆			
02F4₁₆	UART4 Special Mode Register 4	U4SMR4	00₁₆
02F5₁₆	UART4 Special Mode Register 3	U4SMR3	00₁₆
02F6₁₆	UART4 Special Mode Register 2	U4SMR2	00₁₆
02F7₁₆	UART4 Special Mode Register	U4SMR	00₁₆
02F8₁₆	UART4 Transmit/Receive Mode Register	U4MR	00₁₆
02F9₁₆	UART4 Bit Rate Register	U4BRG	XX₁₆
02FA₁₆	UART4 Transmit Buffer Register	U4TB	XX₁₆
02FB₁₆			XX₁₆
02FC₁₆	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000₂
02FD₁₆	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010₂
02FE₁₆	UART4 Receive Buffer Register	U4RB	XX₁₆
02FF₁₆			XX₁₆
0300₁₆	Timer B3, B4, B5 Count Start Flag	TBSR	000X XXXX₂
0301₁₆			
0302₁₆	Timer A1-1 Register	TA11	XX₁₆
0303₁₆			XX₁₆
0304₁₆	Timer A2-1 Register	TA21	XX₁₆
0305₁₆			XX₁₆
0306₁₆	Timer A4-1 Register	TA41	XX₁₆
0307₁₆			XX₁₆
0308₁₆	Three-Phase PWM Control Register 0	INVC0	00₁₆
0309₁₆	Three-Phase PWM Control Register 1	INVC1	00₁₆
030A₁₆	Three-Phase Output Buffer Register 0	IDB0	XX11 1111₂
030B₁₆	Three-Phase Output Buffer Register 1	IDB1	XX11 1111₂
030C₁₆	Dead Time Timer	DTT	XX₁₆
030D₁₆	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XX₁₆
030E₁₆			
030F₁₆			
0310₁₆	Timer B3 Register	TB3	XX₁₆
0311₁₆			XX₁₆
0312₁₆	Timer B4 Register	TB4	XX₁₆
0313₁₆			XX₁₆
0314₁₆	Timer B5 Register	TB5	XX₁₆
0315₁₆			XX₁₆
0316₁₆			
0317₁₆			
0318₁₆			
0319₁₆			
031A₁₆			
031B₁₆	Timer B3 Mode Register	TB3MR	00XX 0000₂
031C₁₆	Timer B4 Mode Register	TB4MR	00XX 0000₂
031D₁₆	Timer B5 Mode Register	TB5MR	00XX 0000₂
031E₁₆			
031F₁₆	External Interrupt Cause Select Register	IFSR	00₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

$V_{CC1}=V_{CC2}=5V$

Table 5.4 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=AV_{CC}=V_{REF}$=4.2 to 5.5V, V_{SS}= AV_{SS} = 0V at Topr=–20 to 85°C, f(BCLK) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
-	Resolution	$V_{REF}=V_{CC1}$				10	Bits
INL	Integral Nonlinearity Error	$V_{REF}=V_{CC1}=V_{CC2}$=5V	AN_0 to AN_7, $AN0_0$ to $AN0_7$, $AN2_0$ to $AN2_7$, $AN15_0$ to $AN15_7$, ANEX0, ANEX1			±3	LSB
							LSB
			External op-amp connection mode			±7	LSB
							LSB
DNL	Differential Nonlinearity Error					±1	LSB
-	Offset Error					±3	LSB
-	Gain Error					±3	LSB
R_{LADDER}	Resistor Ladder	$V_{REF}=V_{CC1}$		8		40	kΩ
t_{CONV}	10-bit Conversion Time(1, 2)			2.06			µs
t_{CONV}	8-bit Conversion Time(1, 2)			1.75			µs
t_{SAMP}	Sampling Time(1)			0.188			µs
V_{REF}	Reference Voltage			2		V_{CC1}	V
V_{IA}	Analog Input Voltage			0		V_{REF}	V

NOTES:
1. Divide f(X_{IN}), if exceeding 16 MHz, to keep ϕAD frequency at 16 MHz or less.
2. With using the sample and hold function.

Table 5.5 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=V_{REF}$=4.2 to 5.5V, $V_{SS}=AV_{SS}$=0V at Topr=–20 to 85°C, f(BCLK) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTES:
1. Measurement when using one D/A converter. The DAi register (i=0, 1) of the D/A converter, not being used, is set to "00_{16}". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr=–20 to 85°C unless otherwise specified)

Table 5.9 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External Clock Input Cycle Time	31.25		ns
$t_{W(H)}$	External Clock Input High ("H") Width	13.75		ns
$t_{W(L)}$	External Clock Input Low ("L") Width	13.75		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

Table 5.10 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{AC1(RD-DB)}$	Data Input Access Time (RD standard)		(Note 1)	ns
$t_{AC1(AD-DB)}$	Data Input Access Time (AD standard, CS standard)		(Note 1)	ns
$t_{AC2(RD-DB)}$	Data Input Access Time (RD standard, when accessing a space with the multiplexrd bus)		(Note 1)	ns
$t_{AC2(AD-DB)}$	Data Input Access Time (AD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{SU(DB-BCLK)}$	Data Input Setup Time	26		ns
$t_{SU(RDY-BCLK)}$	$\overline{RDY}$ Input Setup Time	26		ns
$t_{SU(HOLD-BCLK)}$	$\overline{HOLD}$ Input Setup Time	30		ns
$t_{H(RD-DB)}$	Data Input Hold Time	0		ns
$t_{H(BCLK-RDY)}$	$\overline{RDY}$ Input Hold Time	0		ns
$t_{H(BCLK-HOLD)}$	$\overline{HOLD}$ Input Hold Time	0		ns
$t_{D(BCLK-HLDA)}$	$\overline{HLDA}$ Output Delay Time		25	ns

NOTES:
1. Values can be obtained from the following equations, according to BCLK frequecncy and external bus cycles. Insert a wait state or lower the operation frequency, $f_{(BCLK)}$, if the calculated value is negative.

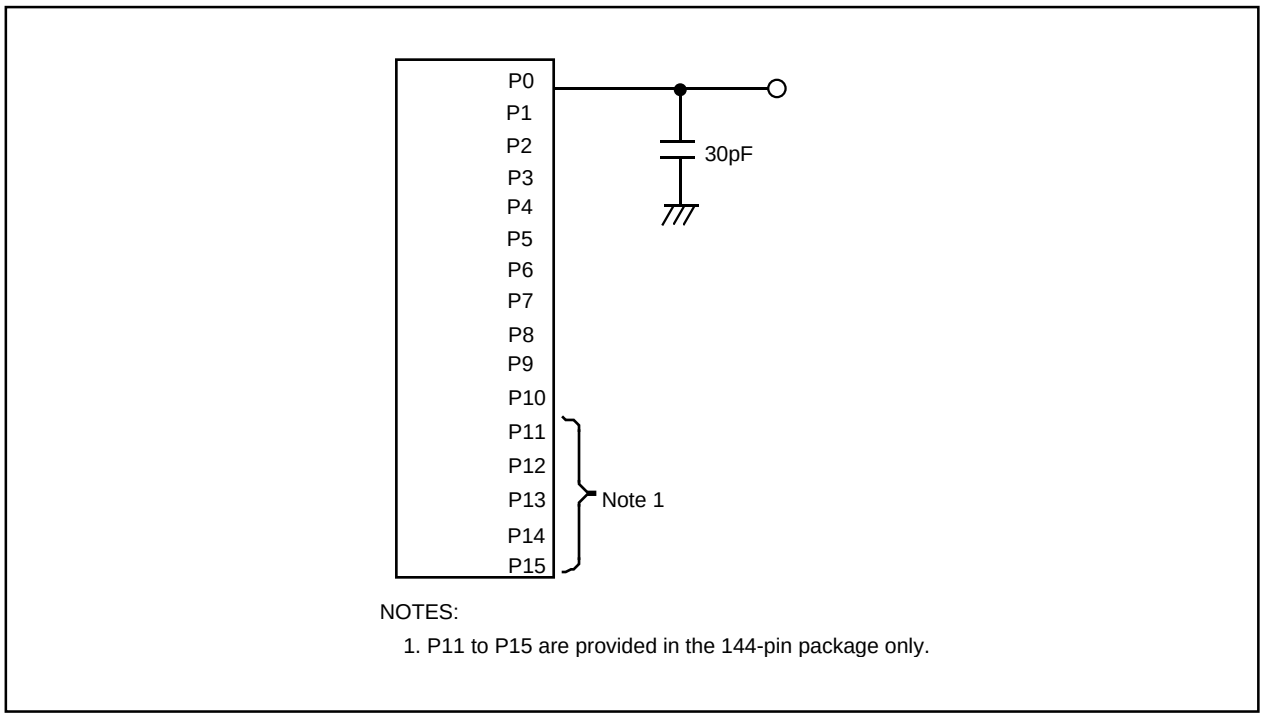
$$t_{AC1(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, m=(bx2)+1)

$$t_{AC1(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)}} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, n=a+b)

$$t_{AC2(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, m=(bx2)-1)

$$t_{AC2(AD-DB)} = \frac{10^9 \times p}{f_{(BCLK)} \times 2} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, p={(a+b-1)x2}+1)

$V_{CC1}=V_{CC2}=5V$



NOTES:
1. P11 to P15 are provided in the 144-pin package only.

Figure 5.2 P0 to P15 Measurement Circuit

$V_{CC1}=V_{CC2}=3.3V$

Switching Characteristics

($V_{CC1}=V_{CC2}$=3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.40 Memory Expansion Mode and Microprocessor Mode (when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 5.2		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)(3)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)(3)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-Select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-Select Signal Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-CS)}$	Chip-Select Signal Output Hold Time (RD standard)(3)		0		ns
$t_{h(WR-CS)}$	Chip-Select Signal Output Hold Time (WR standard)(3)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-3		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		0		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 2)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard)(3)		(Note 1)		ns
$t_{w(WR)}$	WR Output Width		(Note 2)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 20 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles.

$$t_{w(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [ns] \quad \text{(if external bus cycle is } a\phi + b\phi\text{, n=(b x 2)-1)}$$

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)}} - 20 \quad [ns] \quad \text{(if external bus cycle is } a\phi + b\phi\text{, m=b)}$$

3. *tc* ns is added when recovery cycle is inserted.

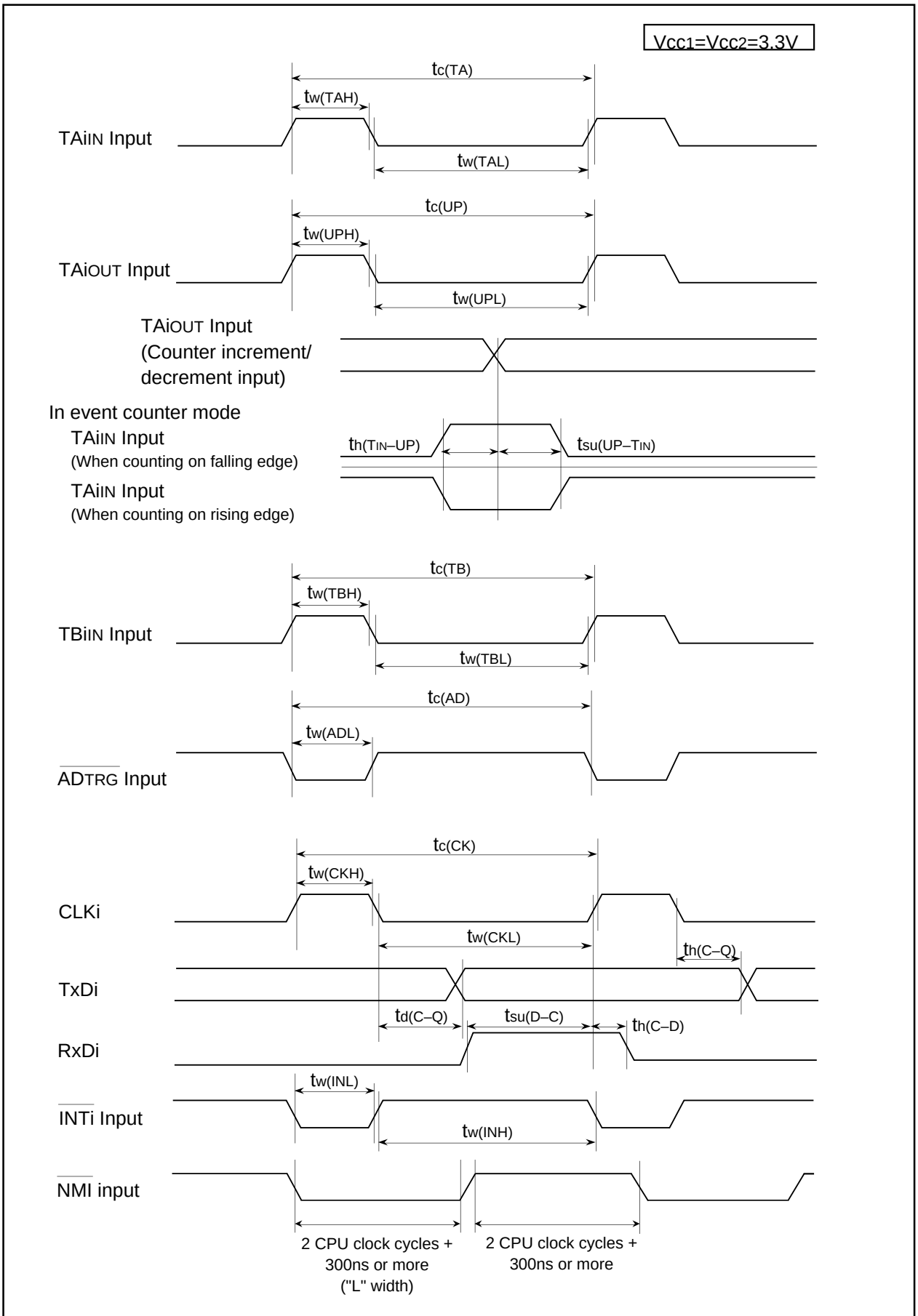


Figure 5.9 Vcc1=Vcc2=3.3V Timing Diagram (3)

$V_{CC1}=V_{CC2}=5V$

Table 5.45 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr= -40 to 85°C (T version), f(BCLK)=32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
-	Resolution	$V_{REF}=V_{CC1}$				10	Bits
INL	Integral Nonlinearity Error	$V_{REF}=V_{CC1}=V_{CC2}=5V$	AN_0 to AN_7, $AN0_0$ to $AN0_7$, $AN2_0$ to $AN2_7$, $AN15_0$ to $AN15_7$, ANEX0, ANEX1			±3	LSB
							LSB
			External op-amp connection mode			±7	LSB
							LSB
DNL	Differential Nonlinearity Error					±1	LSB
-	Offset Error					±3	LSB
-	Gain Error					±3	LSB
R_{LADDER}	Resistor Ladder	$V_{REF}=V_{CC1}$		8		40	kΩ
t_{CONV}	10-bit Conversion Time(1, 2)			2.06			µs
t_{CONV}	8-bit Conversion Time(1, 2)			1.75			µs
t_{SAMP}	Sampling Time(1)			0.188			µs
V_{REF}	Reference Voltage			2		V_{CC1}	V
V_{IA}	Analog Input Voltage			0		V_{REF}	V

NOTES:
1. Divide f(X_{IN}), if exceeding 16 MHz, to keep ϕAD frequency at 16 MHz or less.
2. With using the sample and hold function.

Table 5.46 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr= -40 to 85°C (T version), f(BCLK)=32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTES:
1. Measurement when using one D/A converter. The DAi register (i=0, 1) of the D/A converter, not being used, is set to "00_{16}". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr= -40 to 85°C (T version) unless otherwise specified)

Table 5.49 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External Clock Input Cycle Time	31.25		ns
$tw_{(H)}$	External Clock Input High ("H") Width	13.75		ns
$tw_{(L)}$	External Clock Input Low ("L") Width	13.75		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr= -40 to 85°C (T version) unless otherwise specified)

Table 5.55 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width (counted on both edges)	80		ns

Table 5.56 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width	200		ns

Table 5.57 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width	200		ns

Table 5.58 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max	
$t_{c(AD)}$	$\overline{ADTRG}$ Input Cycle Time (required for trigger)	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ Input Low ("L") Pulse Width	125		ns

Table 5.59 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Setup Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

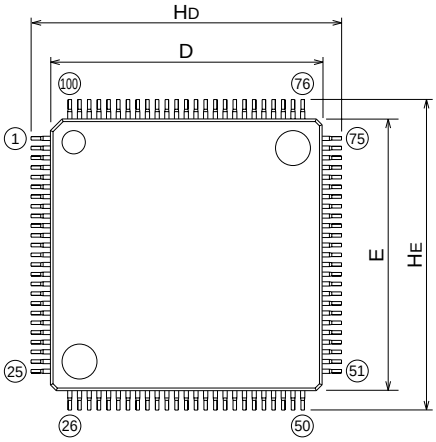
Table 5.60 External Interrupt $\overline{INTi}$ Input

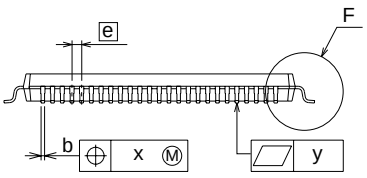
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input High ("H") Width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ Input Low ("L") Width	250		ns

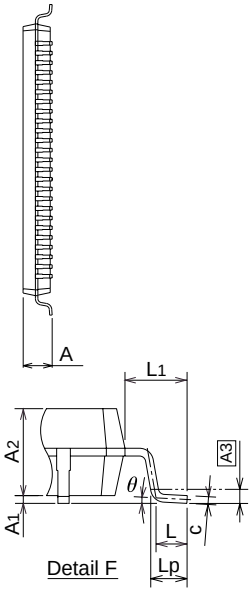
PLQP0100KB-A (100P6Q-A)

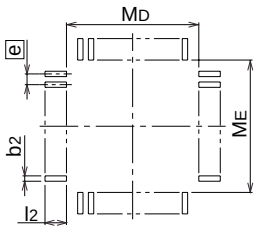
Plastic 100pin 14×14mm body LQFP

JEITA Package Code	RENESAS Code	Previous Code	Mass[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A	0.6g









Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	13.9	14.0	14.1
e	–	0.5	–
HD	15.8	16.0	16.2
HE	15.8	16.0	16.2
L	0.3	0.5	0.7
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	10°
b2	–	0.225	–
l2	0.9	–	–
MD	–	14.4	–
ME	–	14.4	–