Renesas Electronics America Inc - M30845FHGP#U3 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	121
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 34x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30845fhgp-u3

Table 1.4 Pin Characteristics for 144-Pin Package

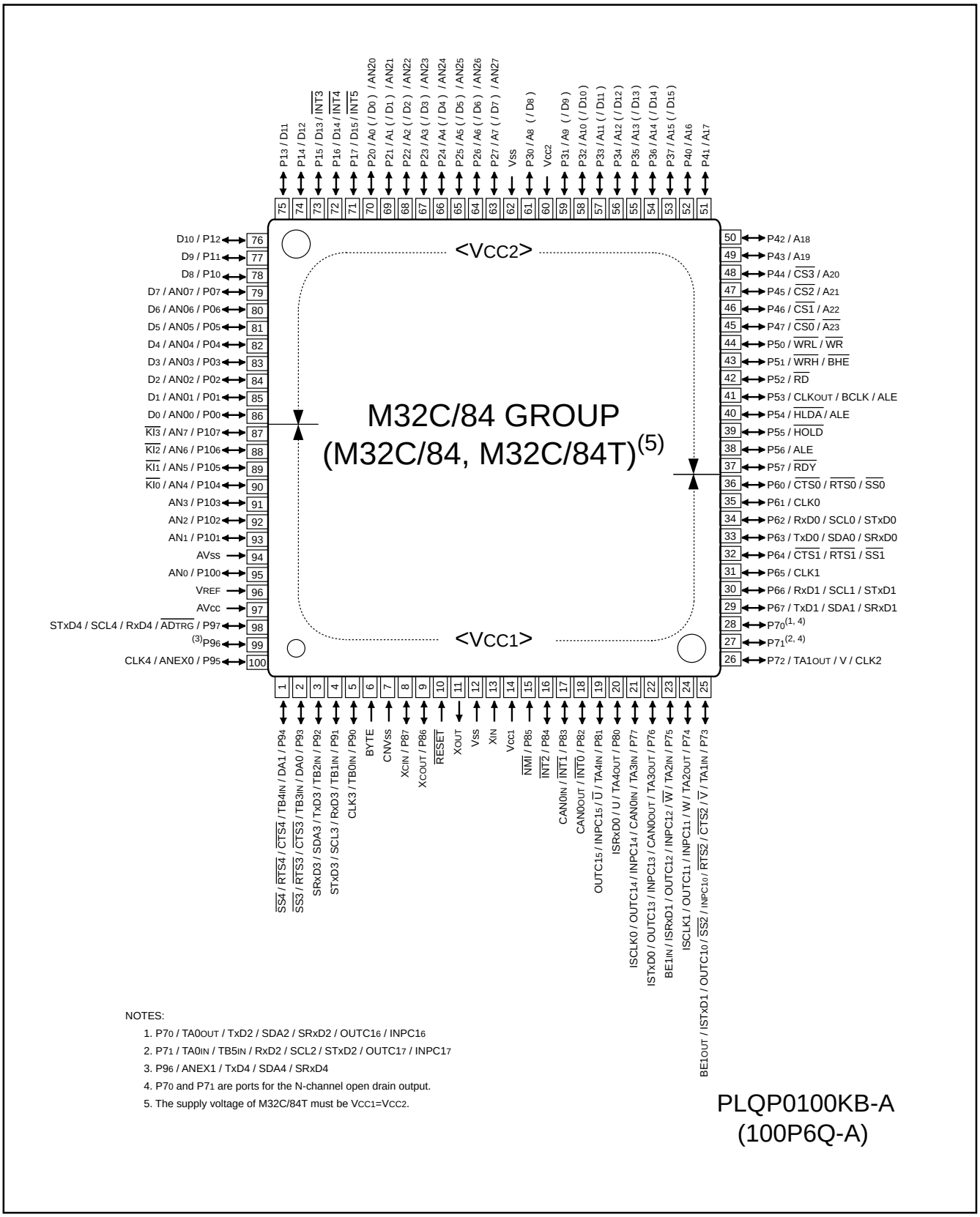
Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin(1)
1		P9$_6$			TxD4/SDA4/SRxD4		ANEX1	
2		P9$_5$			CLK4		ANEX0	
3		P9$_4$		TB4$_{IN}$	$\overline{CTS4}$/$\overline{RTS4}$/$\overline{SS4}$		DA1	
4		P9$_3$		TB3$_{IN}$	$\overline{CTS3}$/$\overline{RTS3}$/$\overline{SS3}$		DA0	
5		P9$_2$		TB2$_{IN}$	TxD3/SDA3/SRxD3			
6		P9$_1$		TB1$_{IN}$	RxD3/SCL3/STxD3			
7		P9$_0$		TB0$_{IN}$	CLK3			
8		P14$_6$						
9		P14$_5$						
10		P14$_4$						
11		P14$_3$				INPC17/OUTC17		
12		P14$_2$				INPC16/OUTC16		
13		P14$_1$				INPC15/OUTC15		
14		P14$_0$				INPC14/OUTC14		
15	BYTE							
16	CNV$_{SS}$							
17	X$_{CIN}$	P8$_7$						
18	X$_{COUT}$	P8$_6$						
19	$\overline{RESET}$							
20	X$_{OUT}$							
21	V$_{SS}$							
22	X$_{IN}$							
23	V$_{CC1}$							
24		P8$_5$	$\overline{NMI}$					
25		P8$_4$	$\overline{INT2}$					
26		P8$_3$	$\overline{INT1}$		CAN0$_{IN}$			
27		P8$_2$	$\overline{INT0}$		CAN0$_{OUT}$			
28		P8$_1$		TA4$_{IN}$/$\overline{U}$		INPC15/OUTC15		
29		P8$_0$		TA4$_{OUT}$/U		ISRxD0		
30		P7$_7$		TA3$_{IN}$	CAN0$_{IN}$	INPC14/OUTC14/ISCLK0		
31		P7$_6$		TA3$_{OUT}$	CAN0$_{OUT}$	INPC13/OUTC13/ISTxD0		
32		P7$_5$		TA2$_{IN}$/$\overline{W}$		INPC12/OUTC12/ISRxD1/BE1$_{IN}$		
33		P7$_4$		TA2$_{OUT}$/W		INPC11/OUTC11/ISCLK1		
34		P7$_3$		TA1$_{IN}$/$\overline{V}$	$\overline{CTS2}$/$\overline{RTS2}$/$\overline{SS2}$	INPC10/OUTC10/ISTxD1/BE1$_{OUT}$		
35		P7$_2$		TA1$_{OUT}$/V	CLK2			
36		P7$_1$		TB5$_{IN}$/TA0$_{IN}$	RxD2/SCL2/STxD2	INPC17/OUTC17		
37		P7$_0$		TA0$_{OUT}$	TxD2/SDA2/SRxD2	INPC16/OUTC16		
38		P6$_7$			TxD1/SDA1/SRxD1			
39	V$_{CC1}$							
40		P6$_6$			RxD1/SCL1/STxD1			
41	V$_{SS}$							
42		P6$_5$			CLK1			
43		P6$_4$			$\overline{CTS1}$/$\overline{RTS1}$/$\overline{SS1}$			
44		P6$_3$			TxD0/SDA0/SRxD0			
45		P6$_2$			RxD0/SCL0/STxD0			
46		P6$_1$			CLK0			
47		P6$_0$			$\overline{CTS0}$/$\overline{RTS0}$/$\overline{SS0}$			
48		P13$_7$						

NOTES:
1. Bus control pins in M32C/84T cannot be used.

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin(1)
97		P2$_4$					AN2$_4$	A$_4$(/D$_4$)
98		P2$_3$					AN2$_3$	A$_3$(/D$_3$)
99		P2$_2$					AN2$_2$	A$_2$(/D$_2$)
100		P2$_1$					AN2$_1$	A$_1$(/D$_1$)
101		P2$_0$					AN2$_0$	A$_0$(/D$_0$)
102		P1$_7$	$\overline{\text{INT5}}$					D$_{15}$
103		P1$_6$	$\overline{\text{INT4}}$					D$_{14}$
104		P1$_5$	$\overline{\text{INT3}}$					D$_{13}$
105		P1$_4$						D$_{12}$
106		P1$_3$						D$_{11}$
107		P1$_2$						D$_{10}$
108		P1$_1$						D$_9$
109		P1$_0$						D$_8$
110		P0$_7$					AN0$_7$	D$_7$
111		P0$_6$					AN0$_6$	D$_6$
112		P0$_5$					AN0$_5$	D$_5$
113		P0$_4$					AN0$_4$	D$_4$
114		P11$_4$						
115		P11$_3$				INPC1$_3$/OUTC1$_3$		
116		P11$_2$				INPC1$_2$/OUTC1$_2$/ISRxD1/BE1$_{IN}$		
117		P11$_1$				INPC1$_1$/OUTC1$_1$/ISCLK1		
118		P11$_0$				INPC1$_0$/OUTC1$_0$/ISTxD1/BE1$_{OUT}$		
119		P0$_3$					AN0$_3$	D$_3$
120		P0$_2$					AN0$_2$	D$_2$
121		P0$_1$					AN0$_1$	D$_1$
122		P0$_0$					AN0$_0$	D$_0$
123		P15$_7$					AN15$_7$	
124		P15$_6$					AN15$_6$	
125		P15$_5$					AN15$_5$	
126		P15$_4$					AN15$_4$	
127		P15$_3$					AN15$_3$	
128		P15$_2$				ISRxD0	AN15$_2$	
129		P15$_1$				ISCLK0	AN15$_1$	
130	V$_{SS}$							
131		P15$_0$				ISTxD0	AN15$_0$	
132	V$_{CC1}$							
133		P10$_7$	$\overline{\text{KI}_3}$				AN$_7$	
134		P10$_6$	$\overline{\text{KI}_2}$				AN$_6$	
135		P10$_5$	$\overline{\text{KI}_1}$				AN$_5$	
136		P10$_4$	$\overline{\text{KI}_0}$				AN$_4$	
137		P10$_3$					AN$_3$	
138		P10$_2$					AN$_2$	
139		P10$_1$					AN$_1$	
140	AV$_{SS}$							
141		P10$_0$					AN$_0$	
142	V$_{REF}$							
143	AV$_{CC}$							
144		P9$_7$			RxD4/SCL4/STxD4		$\overline{\text{AD}_{TRG}}$	

NOTES:
1. Bus control pins in M32C/84T cannot be used.



NOTES:
1. P70 / TA0OUT / TxD2 / SDA2 / SRxD2 / OUTC16 / INPC16
2. P71 / TA0IN / TB5IN / RxD2 / SCL2 / STxD2 / OUTC17 / INPC17
3. P96 / ANEX1 / TxD4 / SDA4 / SRxD4
4. P70 and P71 are ports for the N-channel open drain output.
5. The supply voltage of M32C/84T must be VCC1=VCC2.

PLQP0100KB-A
(100P6Q-A)

Figure 1.5 Pin Assignment for 100-Pin Package

Table 1.5 Pin Characteristics for 100-Pin Package

Package Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin(1)
FP	GP								
1	99		P9$_6$			TxD4/SDA4/SRxD4		ANEX1	
2	100		P9$_5$			CLK4		ANEX0	
3	1		P9$_4$		TB4$_{IN}$	$\overline{CTS4}$/$\overline{RTS4}$/$\overline{SS4}$		DA1	
4	2		P9$_3$		TB3$_{IN}$	$\overline{CTS3}$/$\overline{RTS3}$/$\overline{SS3}$		DA0	
5	3		P9$_2$		TB2$_{IN}$	TxD3/SDA3/SRxD3			
6	4		P9$_1$		TB1$_{IN}$	RxD3/SCL3/STxD3			
7	5		P9$_0$		TB0$_{IN}$	CLK3			
8	6	BYTE							
9	7	CNV$_{SS}$							
10	8	X$_{CIN}$	P8$_7$						
11	9	X$_{COUT}$	P8$_6$						
12	10	$\overline{RESET}$							
13	11	X$_{OUT}$							
14	12	V$_{SS}$							
15	13	X$_{IN}$							
16	14	V$_{CC1}$							
17	15		P8$_5$	$\overline{NMI}$					
18	16		P8$_4$	$\overline{INT2}$					
19	17		P8$_3$	$\overline{INT1}$		CAN0$_{IN}$			
20	18		P8$_2$	$\overline{INT0}$		CAN0$_{OUT}$			
21	19		P8$_1$		TA4$_{IN}$/$\overline{U}$		INPC1$_5$/OUTC1$_5$		
22	20		P8$_0$		TA4$_{OUT}$/U		ISRxD0		
23	21		P7$_7$		TA3$_{IN}$	CAN0$_{IN}$	INPC1$_4$/OUTC1$_4$/ISCLK0		
24	22		P7$_6$		TA3$_{OUT}$	CAN0$_{OUT}$	INPC1$_3$/OUTC1$_3$/ISTxD0		
25	23		P7$_5$		TA2$_{IN}$/$\overline{W}$		INPC1$_2$/OUTC1$_2$/ISRxD1/BE1$_{IN}$		
26	24		P7$_4$		TA2$_{OUT}$/W		INPC1$_1$/OUTC1$_1$/ISCLK1		
27	25		P7$_3$		TA1$_{IN}$/$\overline{V}$	$\overline{CTS2}$/$\overline{RTS2}$/$\overline{SS2}$	INPC1$_0$/OUTC1$_0$/ISTxD1/BE1$_{OUT}$		
28	26		P7$_2$		TA1$_{OUT}$/V	CLK2			
29	27		P7$_1$		TB5$_{IN}$/TA0$_{IN}$	RxD2/SCL2/STxD2	INPC1$_7$/OUTC1$_7$		
30	28		P7$_0$		TA0$_{OUT}$	TxD2/SDA2/SRxD2	INPC1$_6$/OUTC1$_6$		
31	29		P6$_7$			TxD1/SDA1/SRxD1			
32	30		P6$_6$			RxD1/SCL1/STxD1			
33	31		P6$_5$			CLK1			
34	32		P6$_4$			$\overline{CTS1}$/$\overline{RTS1}$/$\overline{SS1}$			
35	33		P6$_3$			TxD0/SDA0/SRxD0			
36	34		P6$_2$			RxD0/SCL0/STxD0			
37	35		P6$_1$			CLK0			
38	36		P6$_0$			$\overline{CTS0}$/$\overline{RTS0}$/$\overline{SS0}$			
39	37		P5$_7$						$\overline{RDY}$
40	38		P5$_6$						ALE
41	39		P5$_5$						$\overline{HOLD}$
42	40		P5$_4$						$\overline{HLDA}$/ALE
43	41		P5$_3$						CLK$_{OUT}$/BCLK/ALE
44	42		P5$_2$						$\overline{RD}$
45	43		P5$_1$						$\overline{WRH}$/$\overline{BHE}$
46	44		P5$_0$						$\overline{WRL}$/$\overline{WR}$
47	45		P4$_7$						$\overline{CS0}$/A$_{23}$
48	46		P4$_6$						$\overline{CS1}$/A$_{22}$
49	47		P4$_5$						$\overline{CS2}$/A$_{21}$
50	48		P4$_4$						$\overline{CS3}$/A$_{20}$

NOTES:
1. Bus control pins in M32C/84T cannot be used.

Table 1.6 Pin Description (144-Pin Package only) (Continued)

Classsfication	Symbol	I/O Type	Supply Voltage	Function
A/D Converter	$AN15_0$ to $AN15_7$	I	V_{CC1}	Analog input pins for the A/D converter
I/O Ports	$P11_0$ to $P11_4$ $P12_0$ to $P12_7$ $P13_0$ to $P13_7$	I/O	V_{CC2}	I/O ports having equivalent functions to P0
	$P14_0$ to $P14_6$ $P15_0$ to $P15_7$	I/O	V_{CC1}	I/O ports having equivalent functions to P0

I : Input O : Output I/O : Input and output

Address	Register	Symbol	Value after RESET
00F0$_{16}$	Data Compare Register 00	G0CMP0	XX$_{16}$
00F1$_{16}$	Data Compare Register 01	G0CMP1	XX$_{16}$
00F2$_{16}$	Data Compare Register 02	G0CMP2	XX$_{16}$
00F3$_{16}$	Data Compare Register 03	G0CMP3	XX$_{16}$
00F4$_{16}$	Data Mask Register 00	G0MSK0	XX$_{16}$
00F5$_{16}$	Data Mask Register 01	G0MSK1	XX$_{16}$
00F6$_{16}$	Communication Clock Select Register	CCS	XXXX 0000$_2$
00F7$_{16}$			
00F8$_{16}$ 00F9$_{16}$	Receive CRC Code Register 0	G0RCRC	XX$_{16}$ XX$_{16}$
00FA$_{16}$ 00FB$_{16}$	Transmit CRC Code Register 0	G0TCRC	00$_{16}$ 00$_{16}$
00FC$_{16}$	SI/O Extended Mode Register 0	G0EMR	00$_{16}$
00FD$_{16}$	SI/O Extended Receive Control Register 0	G0ERC	00$_{16}$
00FE$_{16}$	SI/O Special Communication Interrupt Detect Register 0	G0IRF	00$_{16}$
00FF$_{16}$	SI/O Extended Transmit Control Register 0	G0ETC	0000 0XXX$_2$
0100$_{16}$ 0101$_{16}$	Time Measurement/Waveform Generating Register 10	G1TM0/G1PO0	XX$_{16}$ XX$_{16}$
0102$_{16}$ 0103$_{16}$	Time Measurement/Waveform Generating Register 11	G1TM1/G1PO1	XX$_{16}$ XX$_{16}$
0104$_{16}$ 0105$_{16}$	Time Measurement/Waveform Generating Register 12	G1TM2/G1PO2	XX$_{16}$ XX$_{16}$
0106$_{16}$ 0107$_{16}$	Time Measurement/Waveform Generating Register 13	G1TM3/G1PO3	XX$_{16}$ XX$_{16}$
0108$_{16}$ 0109$_{16}$	Time Measurement/Waveform Generating Register 14	G1TM4/G1PO4	XX$_{16}$ XX$_{16}$
010A$_{16}$ 010B$_{16}$	Time Measurement/Waveform Generating Register 15	G1TM5/G1PO5	XX$_{16}$ XX$_{16}$
010C$_{16}$ 010D$_{16}$	Time Measurement/Waveform Generating Register 16	G1TM6/G1PO6	XX$_{16}$ XX$_{16}$
010E$_{16}$ 010F$_{16}$	Time Measurement/Waveform Generating Register 17	G1TM7/G1PO7	XX$_{16}$ XX$_{16}$
0110$_{16}$	Waveform Generating Control Register 10	G1POCR0	0000 X000$_2$
0111$_{16}$	Waveform Generating Control Register 11	G1POCR1	0X00 X000$_2$
0112$_{16}$	Waveform Generating Control Register 12	G1POCR2	0X00 X000$_2$
0113$_{16}$	Waveform Generating Control Register 13	G1POCR3	0X00 X000$_2$
0114$_{16}$	Waveform Generating Control Register 14	G1POCR4	0X00 X000$_2$
0115$_{16}$	Waveform Generating Control Register 15	G1POCR5	0X00 X000$_2$
0116$_{16}$	Waveform Generating Control Register 16	G1POCR6	0X00 X000$_2$
0117$_{16}$	Waveform Generating Control Register 17	G1POCR7	0X00 X000$_2$
0118$_{16}$	Time Measurement Control Register 10	G1TMCR0	00$_{16}$
0119$_{16}$	Time Measurement Control Register 11	G1TMCR1	00$_{16}$
011A$_{16}$	Time Measurement Control Register 12	G1TMCR2	00$_{16}$
011B$_{16}$	Time Measurement Control Register 13	G1TMCR3	00$_{16}$
011C$_{16}$	Time Measurement Control Register 14	G1TMCR4	00$_{16}$
011D$_{16}$	Time Measurement Control Register 15	G1TMCR5	00$_{16}$
011E$_{16}$	Time Measurement Control Register 16	G1TMCR6	00$_{16}$
011F$_{16}$	Time Measurement Control Register 17	G1TMCR7	00$_{16}$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
021016 021116	CAN0 Slot Interrupt Mask Register	C0SIMKR	0016(2) 0016(2)
021216			
021316			
021416	CAN0 Error Interrupt Mask Register	C0EIMKR	XXXX X0002(2)
021516	CAN0 Error Interrupt Status Register	C0EISTR	XXXX X0002(2)
021616	CAN0 Error Cause Register	C0EFR	0016(2)
021716	CAN0 Baud Rate Prescaler	C0BRP	0000 00012(2)
021816			
021916	CAN0 Mode Register	C0MDR	XXXX XX002(2)
021A16			
021B16			
021C16			
021D16			
021E16			
021F16			
022016 022116	CAN0 Single-Shot Control Register	C0SSCTLR	0016(2) 0016(2)
022216			
022316			
022416 022516	CAN0 Single-Shot Status Register	C0SSSTR	0016(2) 0016(2)
022616			
022716			
022816	CAN0 Global Mask Register Standard ID0	C0GMR0	XXX0 00002(2)
022916	CAN0 Global Mask Register Standard ID1	C0GMR1	XX00 00002(2)
022A16	CAN0 Global Mask Register Extended ID0	C0GMR2	XXXX 00002(2)
022B16	CAN0 Global Mask Register Extended ID1	C0GMR3	0016(2)
022C16	CAN0 Global Mask Register Extended ID2	C0GMR4	XX00 00002(2)
022D16			
022E16			
022F16			
023016	CAN0 Message Slot 0 Control Register / CAN0 Local Mask Register A Standard ID0	C0MCTL0/ C0LMAR0	0000 00002(2) XXX0 00002(2)
023116	CAN0 Message Slot 1 Control Register / CAN0 Local Mask Register A Standard ID1	C0MCTL1/ C0LMAR1	0000 00002(2) XX00 00002(2)
023216	CAN0 Message Slot 2 Control Register / CAN0 Local Mask Register A Extended ID0	C0MCTL2/ C0LMAR2	0000 00002(2) XXXX 00002(2)
023316	CAN0 Message Slot 3 Control Register / CAN0 local Mask Register A Extended ID1	C0MCTL3/ C0LMAR3	0016(2) 0016(2)
023416	CAN0 Message Slot 4 Control Register / CAN0 Local Mask Register A Extended ID2	C0MCTL4/ C0LMAR4	0000 00002(2) XX00 00002(2)
023516	CAN0 Message Slot 5 Control Register	C0MCTL5	0016(2)
023616	CAN0 Message Slot 6 Control Register	C0MCTL6	0016(2)
023716	CAN0 Message Slot 7 Control Register	C0MCTL7	0016(2)
023816	CAN0 Message Slot 8 Control Register / CAN0 Local Mask Register B Standard ID0	C0MCTL8/ C0LMBR0	0000 00002(2) XXX0 00002(2)

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 022016 to 023F16.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and supplying the clock to the CAN module.

Address	Register	Symbol	Value after RESET
0320₁₆			
0321₁₆			
0322₁₆			
0323₁₆			
0324₁₆	UART3 Special Mode Register 4	U3SMR4	00₁₆
0325₁₆	UART3 Special Mode Register 3	U3SMR3	00₁₆
0326₁₆	UART3 Special Mode Register 2	U3SMR2	00₁₆
0327₁₆	UART3 Special Mode Register	U3SMR	00₁₆
0328₁₆	UART3 Transmit/Receive Mode Register	U3MR	00₁₆
0329₁₆	UART3 Bit Rate Register	U3BRG	XX₁₆
032A₁₆ 032B₁₆	UART3 Transmit Buffer Register	U3TB	XX₁₆ XX₁₆
032C₁₆	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000₂
032D₁₆	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010₂
032E₁₆ 032F₁₆	UART3 Receive Buffer Register	U3RB	XX₁₆ XX₁₆
0330₁₆			
0331₁₆			
0332₁₆			
0333₁₆			
0334₁₆	UART2 Special Mode Register 4	U2SMR4	00₁₆
0335₁₆	UART2 Special Mode Register 3	U2SMR3	00₁₆
0336₁₆	UART2 Special Mode Register 2	U2SMR2	00₁₆
0337₁₆	UART2 Special Mode Register	U2SMR	00₁₆
0338₁₆	UART2 Transmit/Receive Mode Register	U2MR	00₁₆
0339₁₆	UART2 Bit Rate Register	U2BRG	XX₁₆
033A₁₆ 033B₁₆	UART2 Transmit Buffer Register	U2TB	XX₁₆ XX₁₆
033C₁₆	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000₂
033D₁₆	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010₂
033E₁₆ 033F₁₆	UART2 Receive Buffer Register	U2RB	XX₁₆ XX₁₆
0340₁₆	Count Start Flag	TABSR	00₁₆
0341₁₆	Clock Prescaler Reset Flag	CPSRF	0XXX XXXX₂
0342₁₆	One-Shot Start Flag	ONSF	00₁₆
0343₁₆	Trigger Select Register	TRGSR	00₁₆
0344₁₆	Up/Down Flag	UDF	00₁₆
0345₁₆			
0346₁₆ 0347₁₆	Timer A0 Register	TA0	XX₁₆ XX₁₆
0348₁₆ 0349₁₆	Timer A1 Register	TA1	XX₁₆ XX₁₆
034A₁₆ 034B₁₆	Timer A2 Register	TA2	XX₁₆ XX₁₆
034C₁₆ 034D₁₆	Timer A3 Register	TA3	XX₁₆ XX₁₆
034E₁₆ 034F₁₆	Timer A4 Register	TA4	XX₁₆ XX₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<144-pin Package>

Address	Register	Symbol	Value after RESET
03A0$_{16}$	Function Select Register A8	PS8	X000 0000$_2$
03A1$_{16}$	Function Select Register A9	PS9	00$_{16}$
03A2$_{16}$			
03A3$_{16}$			
03A4$_{16}$			
03A5$_{16}$			
03A6$_{16}$			
03A7$_{16}$	Function Select Register D1	PSD1	X0XX XX00$_2$
03A8$_{16}$			
03A9$_{16}$			
03AA$_{16}$			
03AB$_{16}$			
03AC$_{16}$	Function Select Register C2	PSC2	XXXX X00X$_2$
03AD$_{16}$	Function Select Register C3	PSC3	X0XX XXXX$_2$
03AE$_{16}$			
03AF$_{16}$	Function Select Register C	PSC	00X0 0000$_2$
03B0$_{16}$	Function Select Register A0	PS0	00$_{16}$
03B1$_{16}$	Function Select Register A1	PS1	00$_{16}$
03B2$_{16}$	Function Select Register B0	PSL0	00$_{16}$
03B3$_{16}$	Function Select Register B1	PSL1	00$_{16}$
03B4$_{16}$	Function Select Register A2	PS2	00X0 0000$_2$
03B5$_{16}$	Function Select Register A3	PS3	00$_{16}$
03B6$_{16}$	Function Select Register B2	PSL2	00X0 0000$_2$
03B7$_{16}$	Function Select Register B3	PSL3	00$_{16}$
03B8$_{16}$			
03B9$_{16}$	Function Select Register A5	PS5	XXX0 0000$_2$
03BA$_{16}$			
03BB$_{16}$			
03BC$_{16}$			
03BD$_{16}$			
03BE$_{16}$			
03BF$_{16}$			
03C0$_{16}$	Port P6 Register	P6	XX$_{16}$
03C1$_{16}$	Port P7 Register	P7	XX$_{16}$
03C2$_{16}$	Port P6 Direction Register	PD6	00$_{16}$
03C3$_{16}$	Port P7 Direction Register	PD7	00$_{16}$
03C4$_{16}$	Port P8 Register	P8	XX$_{16}$
03C5$_{16}$	Port P9 Register	P9	XX$_{16}$
03C6$_{16}$	Port P8 Direction Register	PD8	00X0 0000$_2$
03C7$_{16}$	Port P9 Direction Register	PD9	00$_{16}$
03C8$_{16}$	Port P10 Register	P10	XX$_{16}$
03C9$_{16}$	Port P11 Register	P11	XX$_{16}$
03CA$_{16}$	Port P10 Direction Register	PD10	00$_{16}$
03CB$_{16}$	Port P11 Direction Register	PD11	XXX0 0000$_2$
03CC$_{16}$	Port P12 Register	P12	XX$_{16}$
03CD$_{16}$	Port P13 Register	P13	XX$_{16}$
03CE$_{16}$	Port P12 Direction Register	PD12	00$_{16}$
03CF$_{16}$	Port P13 Direction Register	PD13	00$_{16}$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<100-pin Package>

Address	Register	Symbol	Value after RESET
03A0$_{16}$			
03A1$_{16}$			
03A2$_{16}$			
03A3$_{16}$			
03A4$_{16}$			
03A5$_{16}$			
03A6$_{16}$			
03A7$_{16}$	Function Select Register D1	PSD1	X0XX XX00$_2$
03A8$_{16}$			
03A9$_{16}$			
03AA$_{16}$			
03AB$_{16}$			
03AC$_{16}$	Function Select Register C2	PSC2	XXXX X00X$_2$
03AD$_{16}$	Function Select Register C3	PSC3	X0XX XXXX$_2$
03AE$_{16}$			
03AF$_{16}$	Function Select Register C	PSC	00X0 0000$_2$
03B0$_{16}$	Function Select Register A0	PS0	00$_{16}$
03B1$_{16}$	Function Select Register A1	PS1	00$_{16}$
03B2$_{16}$	Function Select Register B0	PSL0	00$_{16}$
03B3$_{16}$	Function Select Register B1	PSL1	00$_{16}$
03B4$_{16}$	Function Select Register A2	PS2	00X0 0000$_2$
03B5$_{16}$	Function Select Register A3	PS3	00$_{16}$
03B6$_{16}$	Function Select Register B2	PSL2	00X0 0000$_2$
03B7$_{16}$	Function Select Register B3	PSL3	00$_{16}$
03B8$_{16}$			
03B9$_{16}$			
03BA$_{16}$			
03BB$_{16}$			
03BC$_{16}$			
03BD$_{16}$			
03BE$_{16}$			
03BF$_{16}$			
03C0$_{16}$	Port P6 Register	P6	XX$_{16}$
03C1$_{16}$	Port P7 Register	P7	XX$_{16}$
03C2$_{16}$	Port P6 Direction Register	PD6	00$_{16}$
03C3$_{16}$	Port P7 Direction Register	PD7	00$_{16}$
03C4$_{16}$	Port P8 Register	P8	XX$_{16}$
03C5$_{16}$	Port P9 Register	P9	XX$_{16}$
03C6$_{16}$	Port P8 Direction Register	PD8	00X0 0000$_2$
03C7$_{16}$	Port P9 Direction Register	PD9	00$_{16}$
03C8$_{16}$	Port P10 Register	P10	XX$_{16}$
03C9$_{16}$			
03CA$_{16}$	Port P10 Direction Register	PD10	00$_{16}$
03CB$_{16}$	Set default value to "FF$_{16}$"		
03CC$_{16}$			
03CD$_{16}$			
03CE$_{16}$	Set default value to "FF$_{16}$"		
03CF$_{16}$	Set default value to "FF$_{16}$"		

X: Indeterminate

Blank spaces are reserved. No access is allowed.

$V_{CC1}=V_{CC2}=5V$

Table 5.4 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=AV_{CC}=V_{REF}$=4.2 to 5.5V, V_{SS}= AV_{SS} = 0V at Topr=–20 to 85°C, f(BCLK) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
-	Resolution	$V_{REF}=V_{CC1}$				10	Bits
INL	Integral Nonlinearity Error	$V_{REF}=V_{CC1}=V_{CC2}$=5V	AN_0 to AN_7, $AN0_0$ to $AN0_7$, $AN2_0$ to $AN2_7$, $AN15_0$ to $AN15_7$, ANEX0, ANEX1			±3	LSB
							LSB
			External op-amp connection mode			±7	LSB
							LSB
DNL	Differential Nonlinearity Error					±1	LSB
-	Offset Error					±3	LSB
-	Gain Error					±3	LSB
R_{LADDER}	Resistor Ladder	$V_{REF}=V_{CC1}$		8		40	kΩ
t_{CONV}	10-bit Conversion Time(1, 2)			2.06			µs
t_{CONV}	8-bit Conversion Time(1, 2)			1.75			µs
t_{SAMP}	Sampling Time(1)			0.188			µs
V_{REF}	Reference Voltage			2		V_{CC1}	V
V_{IA}	Analog Input Voltage			0		V_{REF}	V

NOTES:
1. Divide f(X_{IN}), if exceeding 16 MHz, to keep ϕAD frequency at 16 MHz or less.
2. With using the sample and hold function.

Table 5.5 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=V_{REF}$=4.2 to 5.5V, $V_{SS}=AV_{SS}$=0V at Topr=–20 to 85°C, f(BCLK) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTES:
1. Measurement when using one D/A converter. The DAi register (i=0, 1) of the D/A converter, not being used, is set to "00_{16}". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

$V_{CC1}=V_{CC2}=5V$

Table 5.7 Voltage Detection Circuit Electrical Characteristics ($V_{CC1}=V_{CC2}=3.0$ to 5.5V, Vss=0V at Topr=25°C unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet4	Low Voltage Detection Voltage(1)	V_{CC1}=3.0 to 5.5V		3.8		V
Vdet3	Reset Space Detection Voltage(1)			3.0		V
Vdet3s	Low Voltage Reset Hold Voltage		2.0			V
Vdet3r	Low Voltage Reset Release Voltage(2)			3.1		V

NOTES:
1. Vdet4 >Vdet3
2. Vdet3r >Vdet3 is not guaranteed.

Table 5.8 Power Supply Timing

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Wait Time to Stabilize Internal Supply Voltage when Power-on	V_{CC1}=3.0 to 5.5V			2	ms
td(S-R)	Wait Time to Release Brown-out. Detection Reset	V_{CC1}=Vdet3r to 5.5V		6(1)	20	ms
td(E-A)	Start-up Time for Low Voltage Detection Circuit Operation	V_{CC1}=3.0 to 5.5V			20	µs

NOTES:
1. V_{CC1}=5V

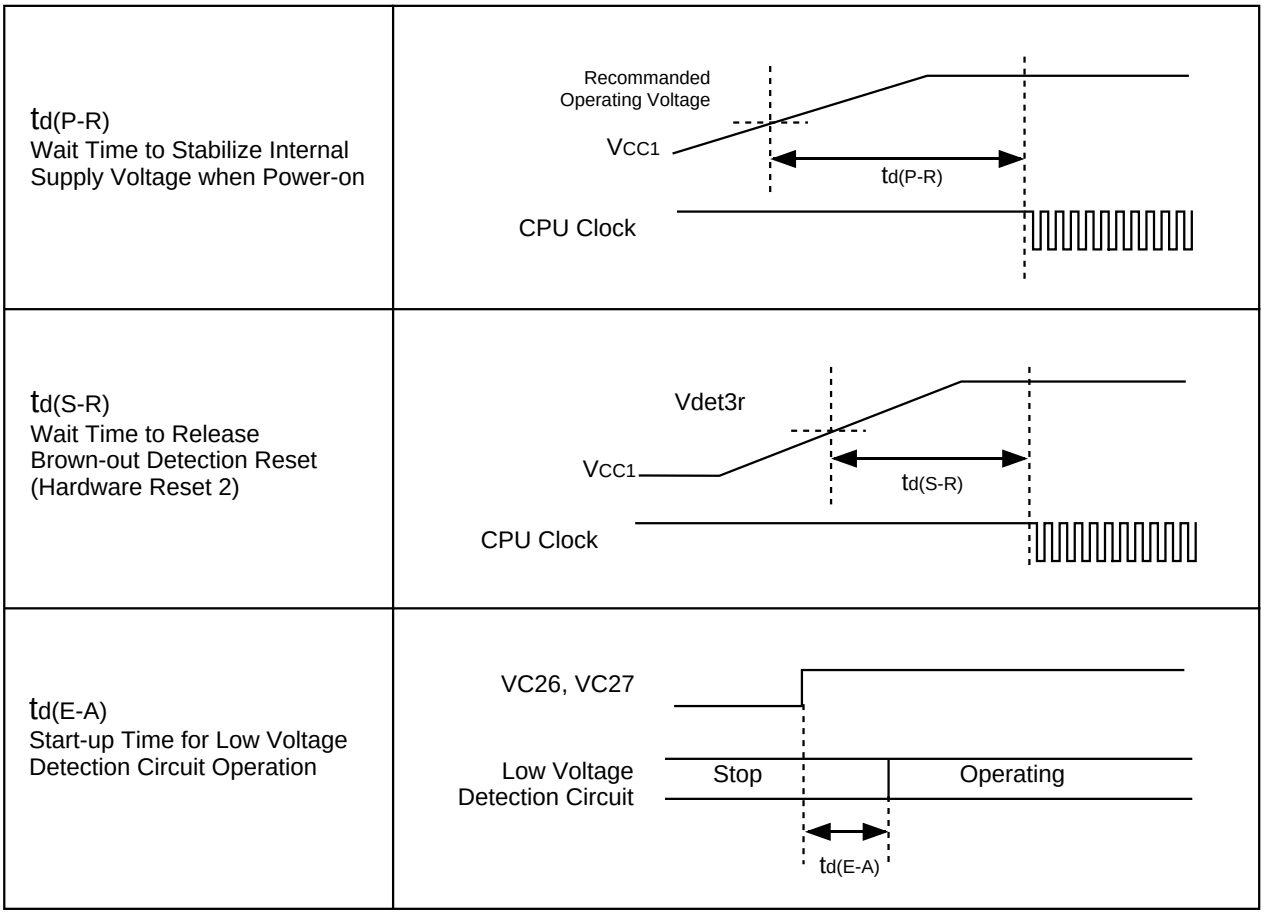


Figure 5.1 Power Supply Timing Diagram

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr=–20 to 85°C unless otherwise specified)

Table 5.9 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External Clock Input Cycle Time	31.25		ns
$t_{W(H)}$	External Clock Input High ("H") Width	13.75		ns
$t_{W(L)}$	External Clock Input Low ("L") Width	13.75		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

Table 5.10 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{AC1(RD-DB)}$	Data Input Access Time (RD standard)		(Note 1)	ns
$t_{AC1(AD-DB)}$	Data Input Access Time (AD standard, CS standard)		(Note 1)	ns
$t_{AC2(RD-DB)}$	Data Input Access Time (RD standard, when accessing a space with the multiplexrd bus)		(Note 1)	ns
$t_{AC2(AD-DB)}$	Data Input Access Time (AD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{SU(DB-BCLK)}$	Data Input Setup Time	26		ns
$t_{SU(RDY-BCLK)}$	$\overline{RDY}$ Input Setup Time	26		ns
$t_{SU(HOLD-BCLK)}$	$\overline{HOLD}$ Input Setup Time	30		ns
$t_{H(RD-DB)}$	Data Input Hold Time	0		ns
$t_{H(BCLK-RDY)}$	$\overline{RDY}$ Input Hold Time	0		ns
$t_{H(BCLK-HOLD)}$	$\overline{HOLD}$ Input Hold Time	0		ns
$t_{D(BCLK-HLDA)}$	$\overline{HLDA}$ Output Delay Time		25	ns

NOTES:
1. Values can be obtained from the following equations, according to BCLK frequecncy and external bus cycles. Insert a wait state or lower the operation frequency, $f_{(BCLK)}$, if the calculated value is negative.

$$t_{AC1(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, m=(bx2)+1)

$$t_{AC1(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)}} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, n=a+b)

$$t_{AC2(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, m=(bx2)-1)

$$t_{AC2(AD-DB)} = \frac{10^9 \times p}{f_{(BCLK)} \times 2} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, p={(a+b-1)x2}+1)

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr=–20 to 85°C unless otherwise specified)

Table 5.11 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	100		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	40		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	40		ns

Table 5.12 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	400		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	200		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	200		ns

Table 5.13 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	200		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 5.14 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 5.15 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAiOUT Input High ("H") Width	1000		ns
$t_{w(UPL)}$	TAiOUT Input Low ("L") Width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAiOUT Input Hold Time	400		ns

$V_{CC1}=V_{CC2}=5V$

Switching Characteristics

(V_{CC1} = V_{CC2} = 4.2 to 5.5V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.22 Memory Expansion Mode and Microprocessor Mode (when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 5.2		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)(3)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)(3)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-Select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-Select Signal Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-CS)}$	Chip-Select Signal Output Hold Time (RD standard)(3)		0		ns
$t_{h(WR-CS)}$	Chip-Select Signal Output Hold Time (WR standard)(3)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-5		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		-5		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 2)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard)(3)		(Note 1)		ns
$t_{w(WR)}$	WR Output Width		(Note 2)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles.

$$t_{w(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [ns]$$ (if external bus cycle is aϕ + bϕ, n=(bx2)-1)

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)}} - 20 \quad [ns]$$ (if external bus cycle is aϕ + bϕ, m= b)

3. *tc* ns is added when recovery cycle is inserted.

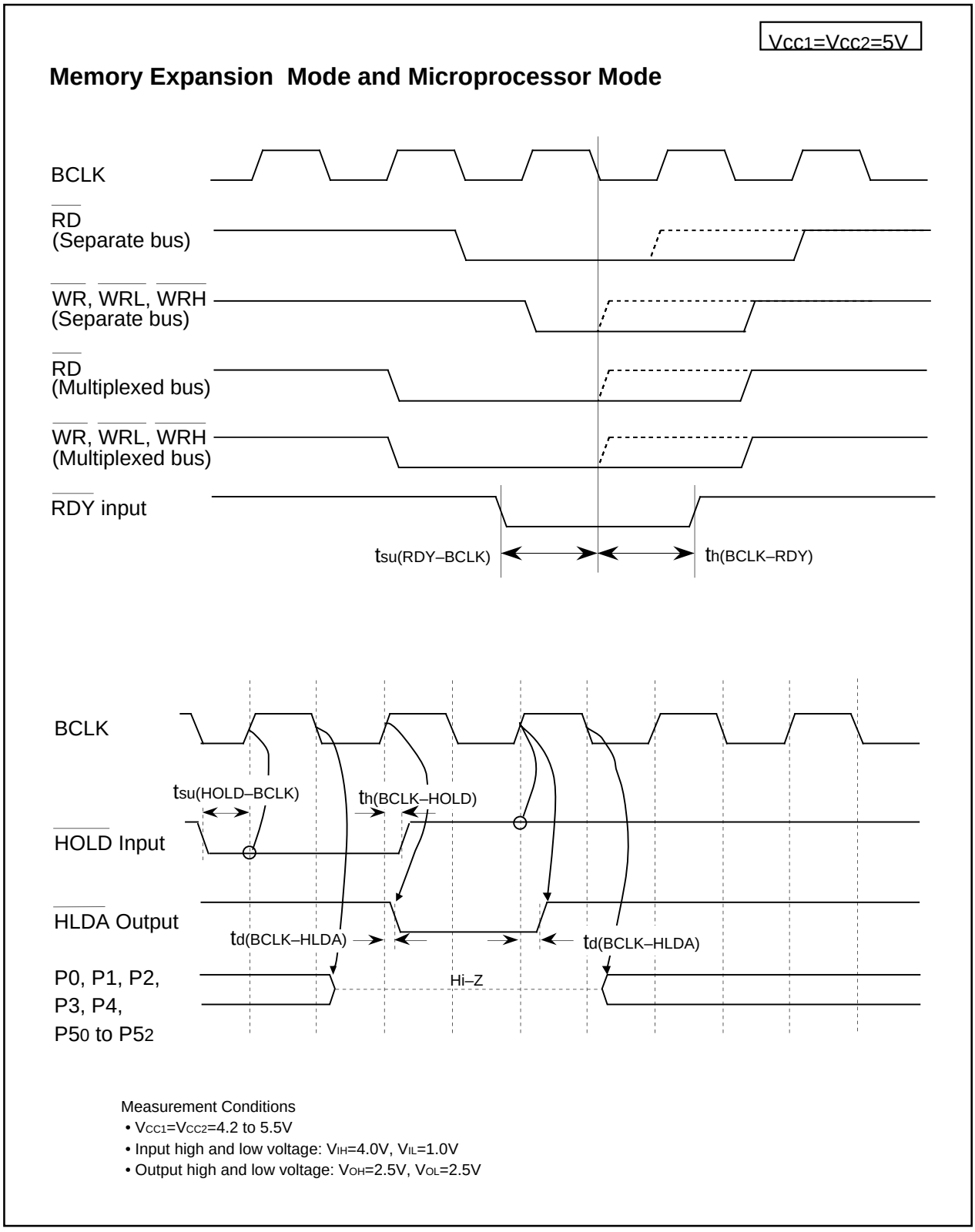


Figure 5.6 Vcc1=Vcc2=5V Timing Diagram (4)

$V_{CC1}=V_{CC2}=3.3V$

Timing Requirements

($V_{CC1}=V_{CC2}$= 3.0 to 3.6V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.34 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width (counted on both edges)	80		ns

Table 5.35 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Wdth	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width	200		ns

Table 5.36 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width	200		ns

Table 5.37 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{ADTRG}$ Input Cycle Time (required for trigger)	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ Input Low ("L") Width	125		ns

Table 5.38 Serial I/O

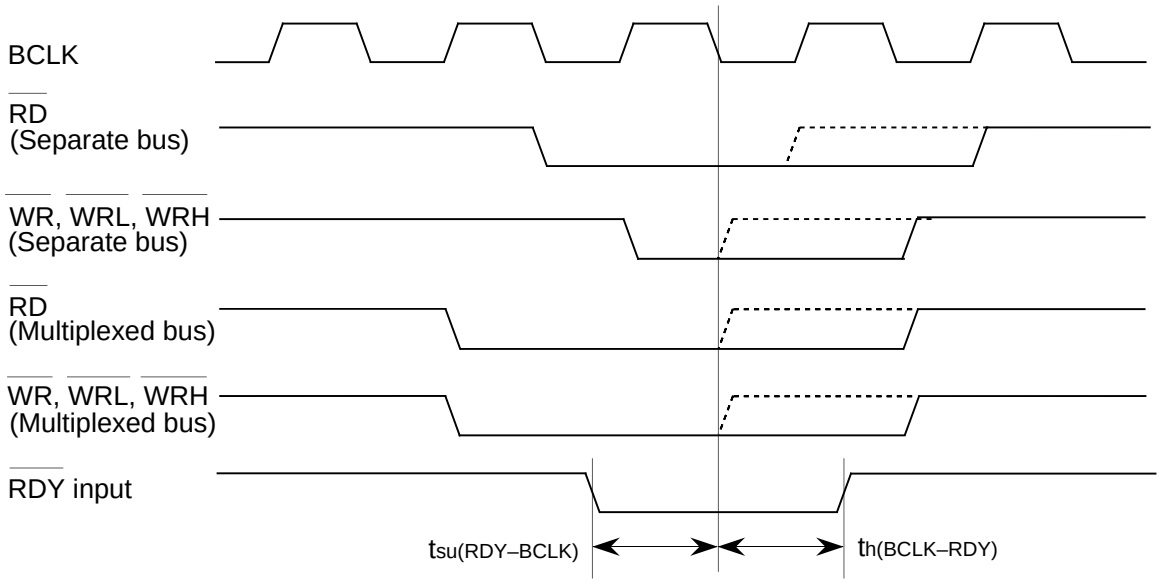
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Setup Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

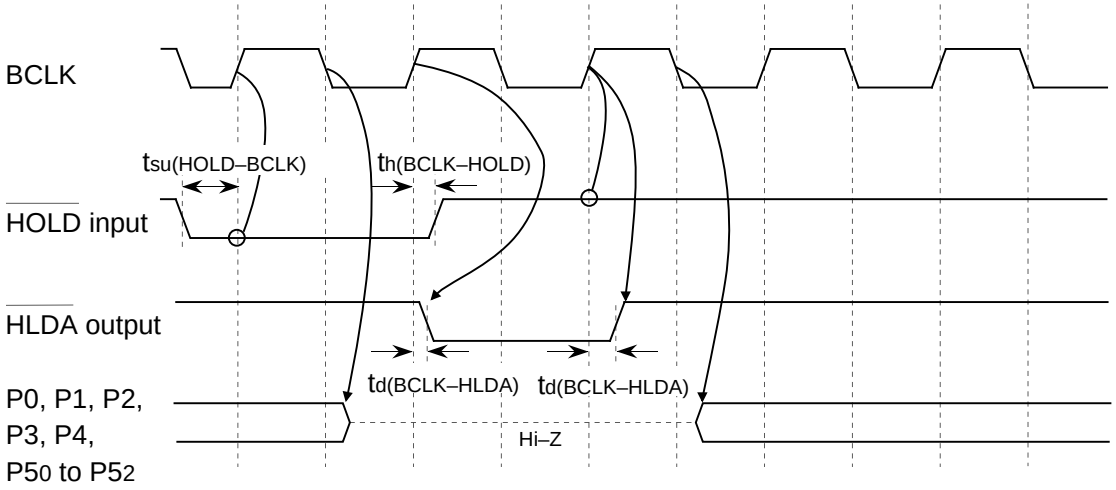
Table 5.39 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input High ("H") Width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ Input Low ("L") Width	250		ns

$V_{CC1}=V_{CC2}=3.3V$

Memory Expansion Mode and Microprocessor Mode





Measurement Conditions:
- $V_{CC1}=V_{CC2}=3.0$ to 3.6V
- Input high and low voltage: $V_{IH}=2.4V$, $V_{IL}=0.6V$
- Output high and low voltage: $V_{OH}=1.5V$, $V_{OL}=1.5V$

Figure 5.10 $V_{CC1}=V_{CC2}=3.3V$ Timing Diagram (4)

Table 5.43 Recommended Operating Conditions

(V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS}=0V at Topr = -40 to 85°C (T version) unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V_{CC1}, V_{CC2}	Supply Voltage (V_{CC1}≥ V_{CC2})		4.2	5.0	5.5	V
AVcc	Analog Supply Voltage			V_{CC1}		V
Vss	Supply Voltage			0		V
AVss	Analog Supply Voltage			0		V
V_{IH}	Input High ("H") Voltage	$P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$(4)	0.8V_{CC2}		V_{CC2}	V
		$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4), X_{IN}, $\overline{RESET}$, CNVss, BYTE	0.8V_{CC1}		V_{CC1}	
		$P7_0$, $P7_1$	0.8V_{CC1}		6.0	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$	0.8V_{CC2}		V_{CC2}	
V_{IL}	Input Low ("L") Voltage	$P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$(4)	0		0.2V_{CC2}	V
		$P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4), X_{IN}, $\overline{RESET}$, CNVss, BYTE	0		0.2V_{CC1}	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$	0		0.2V_{CC2}	
$I_{OH(peak)}$	Peak Output High ("H") Current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			-10.0	mA
$I_{OH(avg)}$	Average Output High ("H") Current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			-5.0	mA
$I_{OL(peak)}$	Peak Output Low ("L") Current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			10.0	mA
$I_{OL(avg)}$	Average Output Low ("L") Current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			5.0	mA

NOTES:

1. Typical values when average output current is 100ms.
2. Total $I_{OL(peak)}$ for P0, P1, P2, $P8_6$, $P8_7$, P9, P10, P11, P14 and P15 must be 80mA or less.
   Total $I_{OL(peak)}$ for P3, P4, P5, P6, P7, $P8_0$ to $P8_4$, P12 and P13 must be 80mA or less.
   Total $I_{OH(peak)}$ for P0, P1, P2, and P11 must be -40mA or less.
   Total $I_{OH(peak)}$ for $P8_6$, $P8_7$, P9, P10, P14 and P15 must be -40mA or less.
   Total $I_{OH(peak)}$ for P3, P4, P5, P12 and P13 must be -40mA or less.
   Total $I_{OH(peak)}$ for P6, P7, and $P8_0$ to $P8_4$ must be -40mA or less.
3. V_{IH} and V_{IL} reference for $P8_7$ applies when $P8_7$ is used as a programmable input port.
   It does not apply when $P8_7$ is used as X_{CIN}.
4. P11 to P15 are provided in the 144-pin package only.

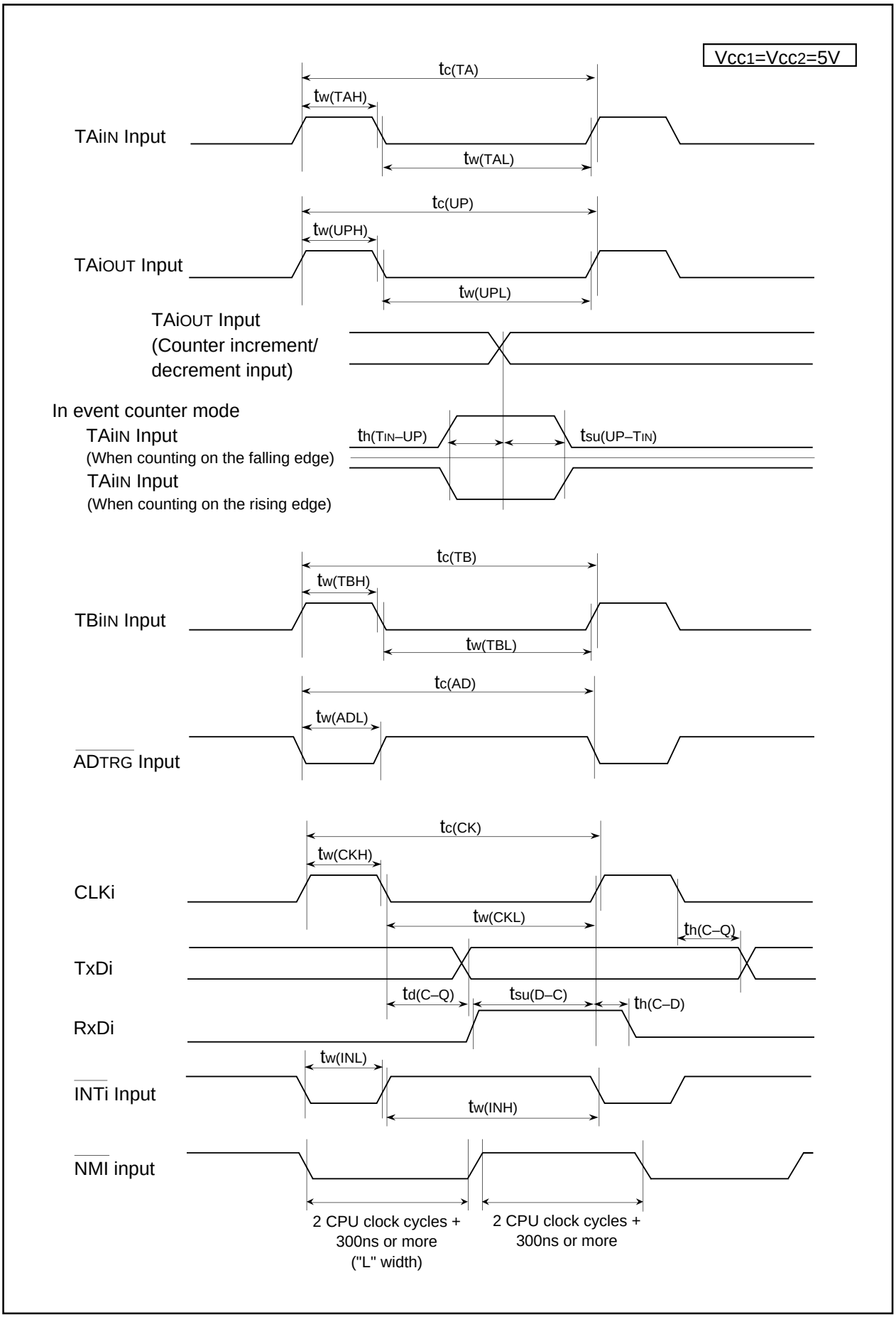


Figure 5.13 Vcc1=Vcc2=5V Timing Diagram