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Details

Product Status	Not For New Designs
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, I ² C, IEBus, SIO, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	121
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 34x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30845fjgp-u3

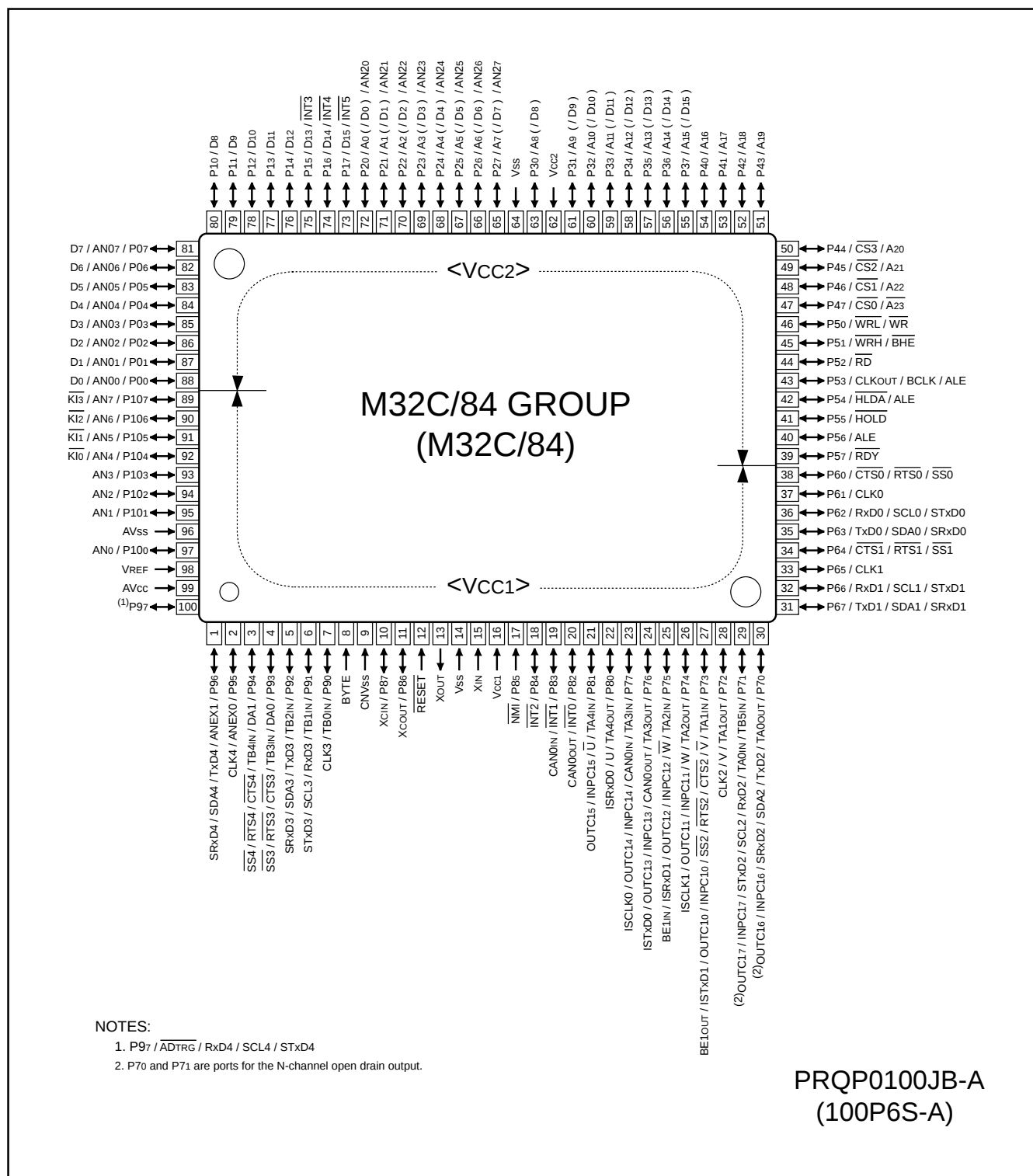


Figure 1.4 Pin Assignment for 100-Pin Package

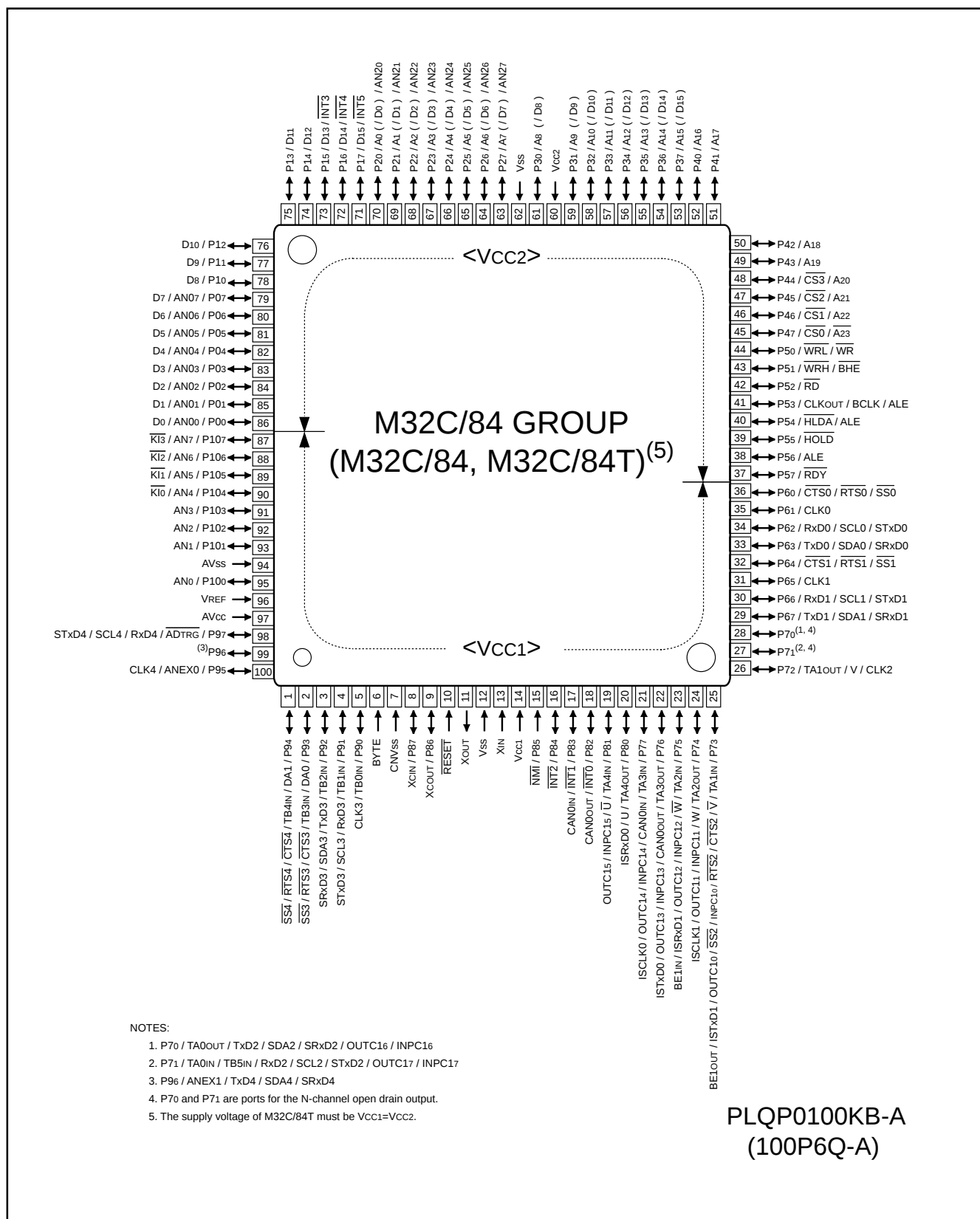


Figure 1.5 Pin Assignment for 100-Pin Package

Table 1.5 Pin Characteristics for 100-Pin Package (Continued)

Package Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
FP	GP								
51	49		P43						A19
52	50		P42						A18
53	51		P41						A17
54	52		P40						A16
55	53		P37						A15(/D15)
56	54		P36						A14(/D14)
57	55		P35						A13(/D13)
58	56		P34						A12(/D12)
59	57		P33						A11(/D11)
60	58		P32						A10(/D10)
61	59		P31						A9(/D9)
62	60	Vcc2							
63	61		P30						A8(/D8)
64	62	Vss							
65	63		P27					AN27	A7(/D7)
66	64		P26					AN26	A6(/D6)
67	65		P25					AN25	A5(/D5)
68	66		P24					AN24	A4(/D4)
69	67		P23					AN23	A3(/D3)
70	68		P22					AN22	A2(/D2)
71	69		P21					AN21	A1(/D1)
72	70		P20					AN20	A0(/D0)
73	71		P17	INT5					D15
74	72		P16	INT4					D14
75	73		P15	INT3					D13
76	74		P14						D12
77	75		P13						D11
78	76		P12						D10
79	77		P11						D9
80	78		P10						D8
81	79		P07					AN07	D7
82	80		P06					AN06	D6
83	81		P05					AN05	D5
84	82		P04					AN04	D4
85	83		P03					AN03	D3
86	84		P02					AN02	D2
87	85		P01					AN01	D1
88	86		P00					AN00	D0
89	87		P107	KI3				AN7	
90	88		P106	KI2				AN6	
91	89		P105	KI1				AN5	
92	90		P104	KI0				AN4	
93	91		P103					AN3	
94	92		P102					AN2	
95	93		P101					AN1	
96	94	AVss							
97	95		P100					AN0	
98	96	VREF							
99	97	AVcc							
100	98		P97			RxD4/SCL4/STxD4		ADTRG	

NOTES:

1. Bus control pins in M32C/84T cannot be used.

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Classification	Symbol	I/O Type	Supply Voltage	Function
Reference Voltage Input	VREF	I	-	Applies reference voltage to the A/D converter and D/A converter
A/D Converter	AN0 to AN7 AN00 to AN07 AN20 to AN27	I	VCC1	Analog input pins for the A/D converter
	ADTRG	I	VCC1	Input pin for an external A/D trigger
	ANEX0	I/O	VCC1	Extended analog input pin for the A/D converter and output pin in external op-amp connection mode
	ANEX1	I	VCC1	Extended analog input pin for the A/D converter
D/A Converter	DA0, DA1	O	VCC1	Output pin for the D/A converter
Intelligent I/O	INPC10 to INPC13	I	VCC1/VCC2 ⁽¹⁾	Input pins for the time measurement function
	INPC14 to INPC17	I	VCC1	
	OUTC10 to OUTC13	O	VCC1/VCC2 ⁽¹⁾	Output pins for the waveform generating function (OUTC16 and OUTC17 assigned to P70 and P71 are pins for the N-channel open drain output.)
	OUTC14 to OUTC17	O	VCC1	
	ISCLK0	I/O	VCC1	Inputs and outputs the clock for the intellignet I/O communication function
	ISCLK1	I/O	VCC1/VCC2 ⁽¹⁾	
	ISRXD0	I	VCC1	Inputs data for the intellignet I/O communication function
	ISRXD1	I	VCC1/VCC2 ⁽¹⁾	
	ISTXD0	O	VCC1	Outputs data for the intellignet I/O communication function
	ISTXD1	O	VCC1/VCC2 ⁽¹⁾	
	BE1IN	I	VCC1/VCC2 ⁽¹⁾	Inputs data for the intellignet I/O communication function
	BE1OUT	O	VCC1/VCC2 ⁽¹⁾	Outputs data for the intellignet I/O communication function
CAN	CAN0IN	I	VCC1	Input pin for the CAN communication function
	CAN0OUT	O	VCC1	Output pin for the CAN communication function
I/O Ports	P00 to P07 P10 to P17 P20 to P27 P30 to P37 P40 to P47 P50 to P57	I/O	VCC2	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resistor available in 4-bit units
	P60 to P67 P70 to P77 P90 to P97 P100 to P107	I/O	VCC1	
	P80 to P84 P86, P87	I/O	VCC1	
Input Port	P85	I	VCC1	Shares a pin with $\overline{\text{NMI}}$. $\overline{\text{NMI}}$ input state can be got by reading P85

I : Input O : Output I/O : Input and output

NOTES:

1. VCC2 is not available in the 100-pin package. VCC1 only available.

Table 1.6 Pin Description (144-Pin Package only) (Continued)

Classsification	Symbol	I/O Type	Supply Voltage	Function
A/D Converter	AN150 to AN157	I	Vcc1	Analog input pins for the A/D converter
I/O Ports	P110 to P114 P120 to P127 P130 to P137	I/O	Vcc2	I/O ports having equivalent functions to P0
	P140 to P146 P150 to P157	I/O	Vcc1	I/O ports having equivalent functions to P0

I : Input O : Output I/O : Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.

The register bank is comprised of 8 registers (R0, R1, R2, R3, A0, A1, SB and FB) out of 28 CPU registers. Two sets of register banks are provided.

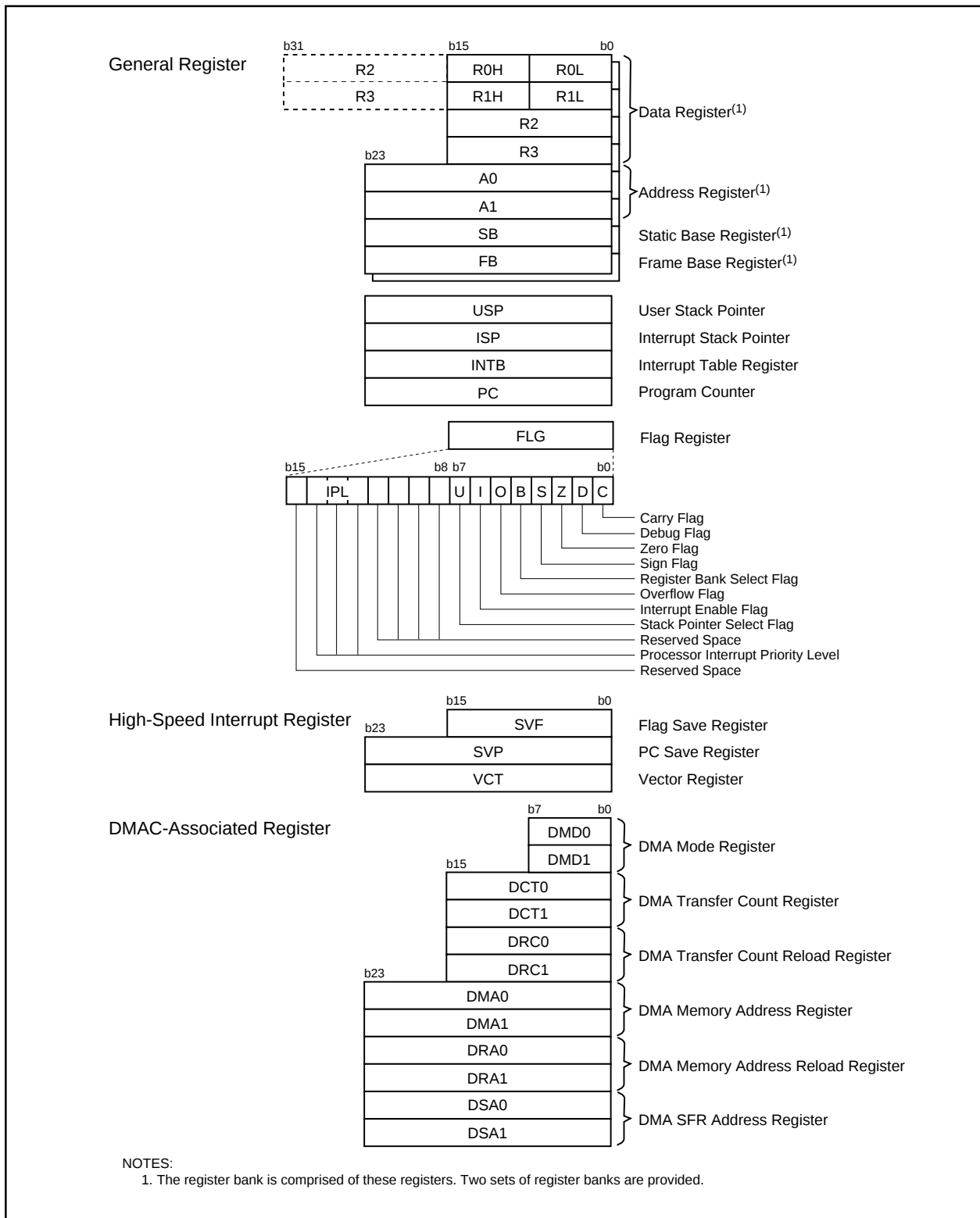


Figure 2.1 CPU Register

Address	Register	Symbol	Value after RESET
0210 ₁₆	CAN0 Slot Interrupt Mask Register	C0SIMKR	00 ₁₆ ⁽²⁾
0211 ₁₆			00 ₁₆ ⁽²⁾
0212 ₁₆			
0213 ₁₆			
0214 ₁₆	CAN0 Error Interrupt Mask Register	C0EIMKR	XXXX X000 ₂ ⁽²⁾
0215 ₁₆	CAN0 Error Interrupt Status Register	C0EISTR	XXXX X000 ₂ ⁽²⁾
0216 ₁₆	CAN0 Error Cause Register	C0EFR	00 ₁₆ ⁽²⁾
0217 ₁₆	CAN0 Baud Rate Prescaler	C0BRP	0000 0001 ₂ ⁽²⁾
0218 ₁₆			
0219 ₁₆	CAN0 Mode Register	C0MDR	XXXX XX00 ₂ ⁽²⁾
021A ₁₆			
021B ₁₆			
021C ₁₆			
021D ₁₆			
021E ₁₆			
021F ₁₆			
0220 ₁₆	CAN0 Single-Shot Control Register	C0SSCTLR	00 ₁₆ ⁽²⁾
0221 ₁₆			00 ₁₆ ⁽²⁾
0222 ₁₆			
0223 ₁₆			
0224 ₁₆	CAN0 Single-Shot Status Register	C0SSSTR	00 ₁₆ ⁽²⁾
0225 ₁₆			00 ₁₆ ⁽²⁾
0226 ₁₆			
0227 ₁₆			
0228 ₁₆	CAN0 Global Mask Register Standard ID0	C0GMR0	XXX0 0000 ₂ ⁽²⁾
0229 ₁₆	CAN0 Global Mask Register Standard ID1	C0GMR1	XX00 0000 ₂ ⁽²⁾
022A ₁₆	CAN0 Global Mask Register Extended ID0	C0GMR2	XXXX 0000 ₂ ⁽²⁾
022B ₁₆	CAN0 Global Mask Register Extended ID1	C0GMR3	00 ₁₆ ⁽²⁾
022C ₁₆	CAN0 Global Mask Register Extended ID2	C0GMR4	XX00 0000 ₂ ⁽²⁾
022D ₁₆			
022E ₁₆			
022F ₁₆			
0230 ₁₆	CAN0 Message Slot 0 Control Register / CAN0 Local Mask Register A Standard ID0	C0MCTL0/ C0LMAR0	0000 0000 ₂ ⁽²⁾ XXX0 0000 ₂ ⁽²⁾
0231 ₁₆	CAN0 Message Slot 1 Control Register / CAN0 Local Mask Register A Standard ID1	C0MCTL1/ C0LMAR1	0000 0000 ₂ ⁽²⁾ XX00 0000 ₂ ⁽²⁾
0232 ₁₆	CAN0 Message Slot 2 Control Register / CAN0 Local Mask Register A Extended ID0	C0MCTL2/ C0LMAR2	0000 0000 ₂ ⁽²⁾ XXXX 0000 ₂ ⁽²⁾
0233 ₁₆	CAN0 Message Slot 3 Control Register / CAN0 local Mask Register A Extended ID1	C0MCTL3/ C0LMAR3	00 ₁₆ ⁽²⁾ 00 ₁₆ ⁽²⁾
0234 ₁₆	CAN0 Message Slot 4 Control Register / CAN0 Local Mask Register A Extended ID2	C0MCTL4/ C0LMAR4	0000 0000 ₂ ⁽²⁾ XX00 0000 ₂ ⁽²⁾
0235 ₁₆	CAN0 Message Slot 5 Control Register	C0MCTL5	00 ₁₆ ⁽²⁾
0236 ₁₆	CAN0 Message Slot 6 Control Register	C0MCTL6	00 ₁₆ ⁽²⁾
0237 ₁₆	CAN0 Message Slot 7 Control Register	C0MCTL7	00 ₁₆ ⁽²⁾
0238 ₁₆	CAN0 Message Slot 8 Control Register / CAN0 Local Mask Register B Standard ID0	C0MCTL8/ C0LMBR0	0000 0000 ₂ ⁽²⁾ XXX0 0000 ₂ ⁽²⁾

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 0220₁₆ to 023F₁₆.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and supplying the clock to the CAN module.

Address	Register	Symbol	Value after RESET
02F0 ₁₆			
02F1 ₁₆			
02F2 ₁₆			
02F3 ₁₆			
02F4 ₁₆	UART4 Special Mode Register 4	U4SMR4	00 ₁₆
02F5 ₁₆	UART4 Special Mode Register 3	U4SMR3	00 ₁₆
02F6 ₁₆	UART4 Special Mode Register 2	U4SMR2	00 ₁₆
02F7 ₁₆	UART4 Special Mode Register	U4SMR	00 ₁₆
02F8 ₁₆	UART4 Transmit/Receive Mode Register	U4MR	00 ₁₆
02F9 ₁₆	UART4 Bit Rate Register	U4BRG	XX ₁₆
02FA ₁₆	UART4 Transmit Buffer Register	U4TB	XX ₁₆
02FB ₁₆			XX ₁₆
02FC ₁₆	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000 ₂
02FD ₁₆	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010 ₂
02FE ₁₆	UART4 Receive Buffer Register	U4RB	XX ₁₆
02FF ₁₆			XX ₁₆
0300 ₁₆	Timer B3, B4, B5 Count Start Flag	TBSR	000X XXXX ₂
0301 ₁₆			
0302 ₁₆	Timer A1-1 Register	TA11	XX ₁₆
0303 ₁₆			XX ₁₆
0304 ₁₆	Timer A2-1 Register	TA21	XX ₁₆
0305 ₁₆			XX ₁₆
0306 ₁₆	Timer A4-1 Register	TA41	XX ₁₆
0307 ₁₆			XX ₁₆
0308 ₁₆	Three-Phase PWM Control Register 0	INVC0	00 ₁₆
0309 ₁₆	Three-Phase PWM Control Register 1	INVC1	00 ₁₆
030A ₁₆	Three-Phase Output Buffer Register 0	IDB0	XX11 1111 ₂
030B ₁₆	Three-Phase Output Buffer Register 1	IDB1	XX11 1111 ₂
030C ₁₆	Dead Time Timer	DTT	XX ₁₆
030D ₁₆	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XX ₁₆
030E ₁₆			
030F ₁₆			
0310 ₁₆	Timer B3 Register	TB3	XX ₁₆
0311 ₁₆			XX ₁₆
0312 ₁₆	Timer B4 Register	TB4	XX ₁₆
0313 ₁₆			XX ₁₆
0314 ₁₆	Timer B5 Register	TB5	XX ₁₆
0315 ₁₆			XX ₁₆
0316 ₁₆			
0317 ₁₆			
0318 ₁₆			
0319 ₁₆			
031A ₁₆			
031B ₁₆	Timer B3 Mode Register	TB3MR	00XX 0000 ₂
031C ₁₆	Timer B4 Mode Register	TB4MR	00XX 0000 ₂
031D ₁₆	Timer B5 Mode Register	TB5MR	00XX 0000 ₂
031E ₁₆			
031F ₁₆	External Interrupt Cause Select Register	IFSR	00 ₁₆

X: Indeterminate

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Address	Register	Symbol	Value after RESET
0320 ₁₆			
0321 ₁₆			
0322 ₁₆			
0323 ₁₆			
0324 ₁₆	UART3 Special Mode Register 4	U3SMR4	00 ₁₆
0325 ₁₆	UART3 Special Mode Register 3	U3SMR3	00 ₁₆
0326 ₁₆	UART3 Special Mode Register 2	U3SMR2	00 ₁₆
0327 ₁₆	UART3 Special Mode Register	U3SMR	00 ₁₆
0328 ₁₆	UART3 Transmit/Receive Mode Register	U3MR	00 ₁₆
0329 ₁₆	UART3 Bit Rate Register	U3BRG	XX ₁₆
032A ₁₆	UART3 Transmit Buffer Register	U3TB	XX ₁₆
032B ₁₆			XX ₁₆
032C ₁₆	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000 ₂
032D ₁₆	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010 ₂
032E ₁₆	UART3 Receive Buffer Register	U3RB	XX ₁₆
032F ₁₆			XX ₁₆
0330 ₁₆			
0331 ₁₆			
0332 ₁₆			
0333 ₁₆			
0334 ₁₆	UART2 Special Mode Register 4	U2SMR4	00 ₁₆
0335 ₁₆	UART2 Special Mode Register 3	U2SMR3	00 ₁₆
0336 ₁₆	UART2 Special Mode Register 2	U2SMR2	00 ₁₆
0337 ₁₆	UART2 Special Mode Register	U2SMR	00 ₁₆
0338 ₁₆	UART2 Transmit/Receive Mode Register	U2MR	00 ₁₆
0339 ₁₆	UART2 Bit Rate Register	U2BRG	XX ₁₆
033A ₁₆	UART2 Transmit Buffer Register	U2TB	XX ₁₆
033B ₁₆			XX ₁₆
033C ₁₆	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000 ₂
033D ₁₆	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010 ₂
033E ₁₆	UART2 Receive Buffer Register	U2RB	XX ₁₆
033F ₁₆			XX ₁₆
0340 ₁₆	Count Start Flag	TABSR	00 ₁₆
0341 ₁₆	Clock Prescaler Reset Flag	CPSRF	0XXX XXXX ₂
0342 ₁₆	One-Shot Start Flag	ONSF	00 ₁₆
0343 ₁₆	Trigger Select Register	TRGSR	00 ₁₆
0344 ₁₆	Up/Down Flag	UDF	00 ₁₆
0345 ₁₆			
0346 ₁₆	Timer A0 Register	TA0	XX ₁₆
0347 ₁₆			XX ₁₆
0348 ₁₆	Timer A1 Register	TA1	XX ₁₆
0349 ₁₆			XX ₁₆
034A ₁₆	Timer A2 Register	TA2	XX ₁₆
034B ₁₆			XX ₁₆
034C ₁₆	Timer A3 Register	TA3	XX ₁₆
034D ₁₆			XX ₁₆
034E ₁₆	Timer A4 Register	TA4	XX ₁₆
034F ₁₆			XX ₁₆

X: Indeterminate

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Address	Register	Symbol	Value after RESET
0380 ₁₆ 0381 ₁₆	A/D0 Register 0	AD00	XXXX XXXX ₂ 0000 0000 ₂
0382 ₁₆ 0383 ₁₆	A/D0 Register 1	AD01	XX ₁₆ XX ₁₆
0384 ₁₆ 0385 ₁₆	A/D0 Register 2	AD02	XX ₁₆ XX ₁₆
0386 ₁₆ 0387 ₁₆	A/D0 Register 3	AD03	XX ₁₆ XX ₁₆
0388 ₁₆ 0389 ₁₆	A/D0 Register 4	AD04	XX ₁₆ XX ₁₆
038A ₁₆ 038B ₁₆	A/D0 Register 5	AD05	XX ₁₆ XX ₁₆
038C ₁₆ 038D ₁₆	A/D0 Register 6	AD06	XX ₁₆ XX ₁₆
038E ₁₆ 038F ₁₆	A/D0 Register 7	AD07	XX ₁₆ XX ₁₆
0390 ₁₆			
0391 ₁₆			
0392 ₁₆ 0393 ₁₆	A/D0 Control Register 4	AD0CON4	XXXX 00XX ₂
0394 ₁₆	A/D0 Control Register 2	AD0CON2	XX0X X000 ₂
0395 ₁₆	A/D0 Control Register 3	AD0CON3	XXXX X000 ₂
0396 ₁₆	A/D0 Control Register 0	AD0CON0	00 ₁₆
0397 ₁₆	A/D0 Control Register 1	AD0CON1	00 ₁₆
0398 ₁₆ 0399 ₁₆	D/A Register 0	DA0	XX ₁₆
039A ₁₆ 039B ₁₆	D/A Register 1	DA1	XX ₁₆
039C ₁₆ 039D ₁₆	D/A Control Register	DACON	XXXX XX00 ₂
039E ₁₆			
039F ₁₆			

X: Indeterminate

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<100-pin Package>

Address	Register	Symbol	Value after RESET
03A0 ₁₆			
03A1 ₁₆			
03A2 ₁₆			
03A3 ₁₆			
03A4 ₁₆			
03A5 ₁₆			
03A6 ₁₆			
03A7 ₁₆	Function Select Register D1	PSD1	X0XX XX00 ₂
03A8 ₁₆			
03A9 ₁₆			
03AA ₁₆			
03AB ₁₆			
03AC ₁₆	Function Select Register C2	PSC2	XXXX X00X ₂
03AD ₁₆	Function Select Register C3	PSC3	X0XX XXXX ₂
03AE ₁₆			
03AF ₁₆	Function Select Register C	PSC	00X0 0000 ₂
03B0 ₁₆	Function Select Register A0	PS0	00 ₁₆
03B1 ₁₆	Function Select Register A1	PS1	00 ₁₆
03B2 ₁₆	Function Select Register B0	PSL0	00 ₁₆
03B3 ₁₆	Function Select Register B1	PSL1	00 ₁₆
03B4 ₁₆	Function Select Register A2	PS2	00X0 0000 ₂
03B5 ₁₆	Function Select Register A3	PS3	00 ₁₆
03B6 ₁₆	Function Select Register B2	PSL2	00X0 0000 ₂
03B7 ₁₆	Function Select Register B3	PSL3	00 ₁₆
03B8 ₁₆			
03B9 ₁₆			
03BA ₁₆			
03BB ₁₆			
03BC ₁₆			
03BD ₁₆			
03BE ₁₆			
03BF ₁₆			
03C0 ₁₆	Port P6 Register	P6	XX ₁₆
03C1 ₁₆	Port P7 Register	P7	XX ₁₆
03C2 ₁₆	Port P6 Direction Register	PD6	00 ₁₆
03C3 ₁₆	Port P7 Direction Register	PD7	00 ₁₆
03C4 ₁₆	Port P8 Register	P8	XX ₁₆
03C5 ₁₆	Port P9 Register	P9	XX ₁₆
03C6 ₁₆	Port P8 Direction Register	PD8	00X0 0000 ₂
03C7 ₁₆	Port P9 Direction Register	PD9	00 ₁₆
03C8 ₁₆	Port P10 Register	P10	XX ₁₆
03C9 ₁₆			
03CA ₁₆	Port P10 Direction Register	PD10	00 ₁₆
03CB ₁₆	Set default value to "FF ₁₆ "		
03CC ₁₆			
03CD ₁₆			
03CE ₁₆	Set default value to "FF ₁₆ "		
03CF ₁₆	Set default value to "FF ₁₆ "		

X: Indeterminate

Blank spaces are reserved. No access is allowed.

$$V_{CC1}=V_{CC2}=5V$$

Table 5.3 Electrical Characteristics (Continued)

($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr} = -20$ to $85^{\circ}C$, $f(BCLK)=32MHz$ unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
I _{cc}	Power Supply Current	In single-chip mode, output pins are left open and other pins are connected to V _{SS} .	f(BCLK)=32 MHz, Square wave, No division		28	45	mA
			f(BCLK)=32 kHz, In low-power consumption mode, Program running on ROM		430		μA
			Flash Memory		25		
			Masked ROM				
			f(BCLK)=32 kHz, In low-power consumption mode, Program running on RAM ⁽¹⁾		25		μA
			f(BCLK)=32 kHz, In wait mode, T _{opr} =25° C		10		μA
			While clock stops, T _{opr} =25° C		0.8	5	μA
			While clock stops, T _{opr} =85° C			50	μA

NOTES:

- Value is obtained when setting the FMSTP bit in the FMR0 register to "1" (flash memory stopped).

$$V_{CC1}=V_{CC2}=5V$$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr}=-20$ to $85^{\circ}C$ unless otherwise specified)

Table 5.9 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External Clock Input Cycle Time	31.25		ns
$t_{w(H)}$	External Clock Input High ("H") Width	13.75		ns
$t_{w(L)}$	External Clock Input Low ("L") Width	13.75		ns
t_r	External Clock Rise Time		5	ns
t_f	External Clock Fall Time		5	ns

Table 5.10 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data Input Access Time (RD standard)		(Note 1)	ns
$t_{ac1(AD-DB)}$	Data Input Access Time (AD standard, CS standard)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (RD standard, when accessing a space with the multiplexrd bus)		(Note 1)	ns
$t_{ac2(AD-DB)}$	Data Input Access Time (AD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{su(DB-BCLK)}$	Data Input Setup Time	26		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ Input Setup Time	26		ns
$t_{su(HOLD-BCLK)}$	$\overline{HOLD}$ Input Setup Time	30		ns
$t_{h(RD-DB)}$	Data Input Hold Time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ Input Hold Time	0		ns
$t_{h(BCLK-HOLD)}$	$\overline{HOLD}$ Input Hold Time	0		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ Output Delay Time		25	ns

NOTES:

- Values can be obtained from the following equations, according to BCLK frequency and external bus cycles. Insert a wait state or lower the operation frequency, $f_{(BCLK)}$, if the calculated value is negative.

$$t_{ac1(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, m=(bx2)+1)$$

$$t_{ac1(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)}} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, n=a+b)$$

$$t_{ac2(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, m=(bx2)-1)$$

$$t_{ac2(AD-DB)} = \frac{10^9 \times p}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, p=\{(a+b-1) \times 2\}+1)$$

$$V_{CC1}=V_{CC2}=3.3V$$

Timing Requirements

($V_{CC1}=V_{CC2}= 3.0$ to $3.6V$, $V_{SS} = 0V$ at $T_{opr} = -20$ to $85^{\circ}C$ unless otherwise specified)

Table 5.27 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External Clock Input Cycle Time	41		ns
$t_{w(H)}$	External Clock Input High ("H") Width	18		ns
$t_{w(L)}$	External Clock Input Low ("L") Width	18		ns
t_r	External Clock Rise Time		5	ns
t_f	External Clock Fall Time		5	ns

Table 5.28 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data Input Access Time (RD standard)		(Note 1)	ns
$t_{ac1(AD-DB)}$	Data Input Access Time (AD standard, CS standard)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{ac2(AD-DB)}$	Data Input Access Time (AD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{su(DB-BCLK)}$	Data Input Setup Time	30		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ Input Setup Time	40		ns
$t_{su(HOLD-BCLK)}$	$\overline{HOLD}$ Input Setup Time	60		ns
$t_{h(RD-DB)}$	Data Input Hold Time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ Input Hold Time	0		ns
$t_{h(BCLK-HOLD)}$	$\overline{HOLD}$ Input Hold Time	0		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ Output Delay Time		25	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles. Insert a wait state or lower the operation frequency, $f_{(BCLK)}$, if the calculated value is negative.

$$t_{ac1(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, m=(bx2)+1)$$

$$t_{ac1(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)}} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, n=a+b)$$

$$t_{ac2(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, m=(bx2)-1)$$

$$t_{ac2(AD-DB)} = \frac{10^9 \times p}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, p=\{(a+b-1) \times 2\}+1)$$

$$V_{CC1}=V_{CC2}=3.3V$$

Timing Requirements

($V_{CC1}=V_{CC2}= 3.0$ to $3.6V$, $V_{SS}= 0V$ at $T_{opr} = -20$ to $85^{\circ}C$ unless otherwise specified)

Table 5.29 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN Input Cycle Time	100		ns
$t_{W(TAH)}$	TAiIN Input High ("H") Width	40		ns
$t_{W(TAL)}$	TAiIN Input Low ("L") Width	40		ns

Table 5.30 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN Input Cycle Time	400		ns
$t_{W(TAH)}$	TAiIN Input High ("H") Width	200		ns
$t_{W(TAL)}$	TAiIN Input Low ("L") Width	200		ns

Table 5.31 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN Input Cycle Time	200		ns
$t_{W(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{W(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 5.32 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{W(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 5.33 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(UP)}$	TAiOUT Input Cycle Time	2000		ns
$t_{W(UPH)}$	TAiOUT Input High ("H") Width	1000		ns
$t_{W(UPL)}$	TAiOUT Input Low ("L") Width	1000		ns
$t_{SU(UP-TIN)}$	TAiOUT Input Setup Time	400		ns
$t_{H(TIN-UP)}$	TAiOUT Input Hold Time	400		ns

$$V_{CC1}=V_{CC2}=3.3V$$

Switching Characteristics

($V_{CC1}=V_{CC2}=3.0$ to $3.6V$, $V_{SS} = 0V$ at $T_{opr} = -20$ to $85^{\circ}C$ unless otherwise specified)

Table 5.40 Memory Expansion Mode and Microprocessor Mode
(when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 5.2		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard) ⁽³⁾		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard) ⁽³⁾		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-Select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-Select Signal Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-CS)}$	Chip-Select Signal Output Hold Time (RD standard) ⁽³⁾		0		ns
$t_{h(WR-CS)}$	Chip-Select Signal Output Hold Time (WR standard) ⁽³⁾		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-3		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		0		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 2)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard) ⁽³⁾		(Note 1)		ns
$t_{w(WR)}$	WR Output Width		(Note 2)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 20 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

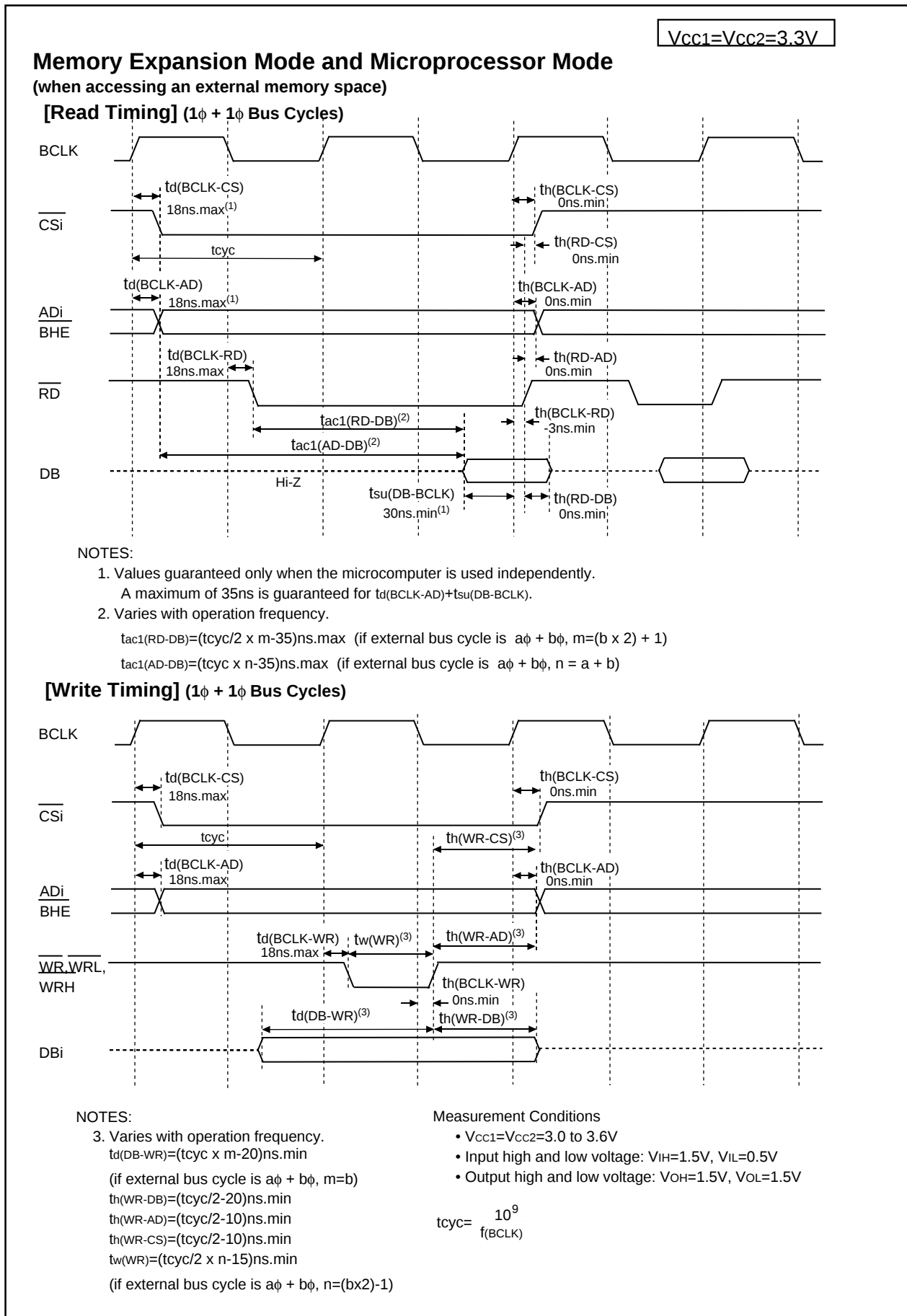
$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles.

$$t_{w(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, n=(b \times 2)-1)$$

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)}} - 20 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, m=b)$$

3. t_{cns} is added when recovery cycle is inserted.

Figure 5.7 V_{CC1}=V_{CC2}=3.3V Timing Diagram (1)

$$V_{CC1}=V_{CC2}=5V$$

Table 5.45 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr}= -40$ to $85^{\circ}C$ (T version), $f(BCLK)=32MHz$ unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution	$V_{REF}=V_{CC1}$			10	Bits
INL	Integral Nonlinearity Error	$V_{REF}=V_{CC1}=V_{CC2}=5V$			± 3	LSB
						LSB
		External op-amp connection mode			± 7	LSB
DNL	Differential Nonlinearity Error				± 1	LSB
-	Offset Error				± 3	LSB
-	Gain Error				± 3	LSB
RLADDER	Resistor Ladder	$V_{REF}=V_{CC1}$	8		40	k Ω
t _{CONV}	10-bit Conversion Time ^(1, 2)		2.06			μs
t _{CONV}	8-bit Conversion Time ^(1, 2)		1.75			μs
t _{SAMP}	Sampling Time ⁽¹⁾		0.188			μs
V _{REF}	Reference Voltage		2		V_{CC1}	V
V _{IA}	Analog Input Voltage		0		V_{REF}	V

NOTES:

1. Divide $f(X_{IN})$, if exceeding 16 MHz, to keep ϕ_{AD} frequency at 16 MHz or less.
2. With using the sample and hold function.

Table 5.46 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr}= -40$ to $85^{\circ}C$ (T version), $f(BCLK)=32MHz$ unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t _{SU}	Setup Time				3	μs
R _O	Output Resistance		4	10	20	k Ω
I _{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTES:

1. Measurement when using one D/A converter. The DA_i register (i=0, 1) of the D/A converter, not being used, is set to "00₁₆". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

$$V_{CC1}=V_{CC2}=5V$$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr}= -40$ to $85^{\circ}C$ (T version) unless otherwise specified)

Table 5.50 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	100		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	40		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	40		ns

Table 5.51 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	400		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	200		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	200		ns

Table 5.52 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	200		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 5.53 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 5.54 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAiOUT Input High ("H") Width	1000		ns
$t_{w(UPL)}$	TAiOUT Input Low ("L") Width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAiOUT Input Hold Time	400		ns

REVISION HISTORY	M32C/84 Group (M32C/84, M32C/84T) Datasheet
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Rev.	Date	Description	
		Page	Summary
		63	• Table 5.28 Memory Expansion Mode and Microprocessor Mode $t_{su}(DB-BCLK)$, $t_{su}(RDY-BCLK)$ and $t_{su}(HOLD-BCLK)$ value modified
		66	• Table 5.40 Memory Expansion Mode and Microprocessor Mode equation of $t_h(WR-DB)$ modified
		67	• Table 5.41 Memory Expansion Mode and Microprocessor Mode $t_h(BCLK-ALE)$ value modified; equation of $t_h(WR-DB)$ modified
		72	• 5.2 Electrical Characteristics (M32C/84T) added
1.10	Jun.28, 2004	-	High-reliability version (U version) deleted
			Overview
		5	• Table 1.3 M32C/84 Group (1) (2) development status modified
		6	• Figure 1.2 Product Numbering System figure modified
1.20	Apr.18, 2005		Overview
		2, 3	• Table 1.1 and Table 1.2 M32C/84 Group (M32C/84, M32C/84T) Performance Note 4 added
		6	• Table 1.3 M32C/84 Group (1) (2) Information updated
		16, 17	• Table 1.6 Pin Description Note 2 deleted
			Memory
		22	• Figure 3.1 Memory Map Description added to Note 3
			SFR
		24	• The PWCR0 and PWCR1 registers newly added to address 004C16 and 004D16 • “Values after RESET” for the G0RB, G1BCR1, G1RB, IDB0, IDB1, DM0SL to DM3SL and PSC registers revised
			Electrical Characteristics
		46	• Table 5.3 Electrical Characteristics I_{CC} standard value revised
		49	• Table 5.6 Flash Memory Electrical Characteristics T_{opr} value modified
		50	• Table 5.7 Voltage Detection Circuit Electrical Characteristics V_{CC1} value modified
		58	• Figure 5.4 $V_{CC1}=V_{CC2}=5V$ Timing Diagram (2) Diagram modified
		61	• Table 5.24 Electrical Characteristics I_{CC} standard value revised
		63	• Table 5.28 Memory Expansion Mode and Microprocessor Mode $t_{ac1}(AD-DB)$ expression modified
		75	• Table 5.44 Electrical Characteristics I_{CC} standard value revised
		78	• Table 5.47 Flash Memory Electrical Characteristics T_{opr} value modified
1.21	Jul.08, 2005		Special Function Register (SFR)
		37	• The TCSPR register Value after reset modified
			Electrical Characteristics
		45	• Table 5.2 Electrical Characteristics Parameter $f(BCLK)$ and its values added
		51	• Table 5.10 Memory Expansion Mode and Microprocessor Mode $t_{ac1}(RD-DB)$ expression on Note 1 modified; $t_{ac2}(RD-DB)$ expression on Note 1 added