Renesas Electronics America Inc - M30845FWGP#U3 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	121
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 34x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30845fwgp-u3

1.2 Performance Overview

Tables 1.1 and 1.2 list performance overview of the M32C/84 group (M32C/84, M32C/84T).

Table 1.1 M32C/84 Group (M32C/84, M32C/84T) Performance (144-Pin Package)

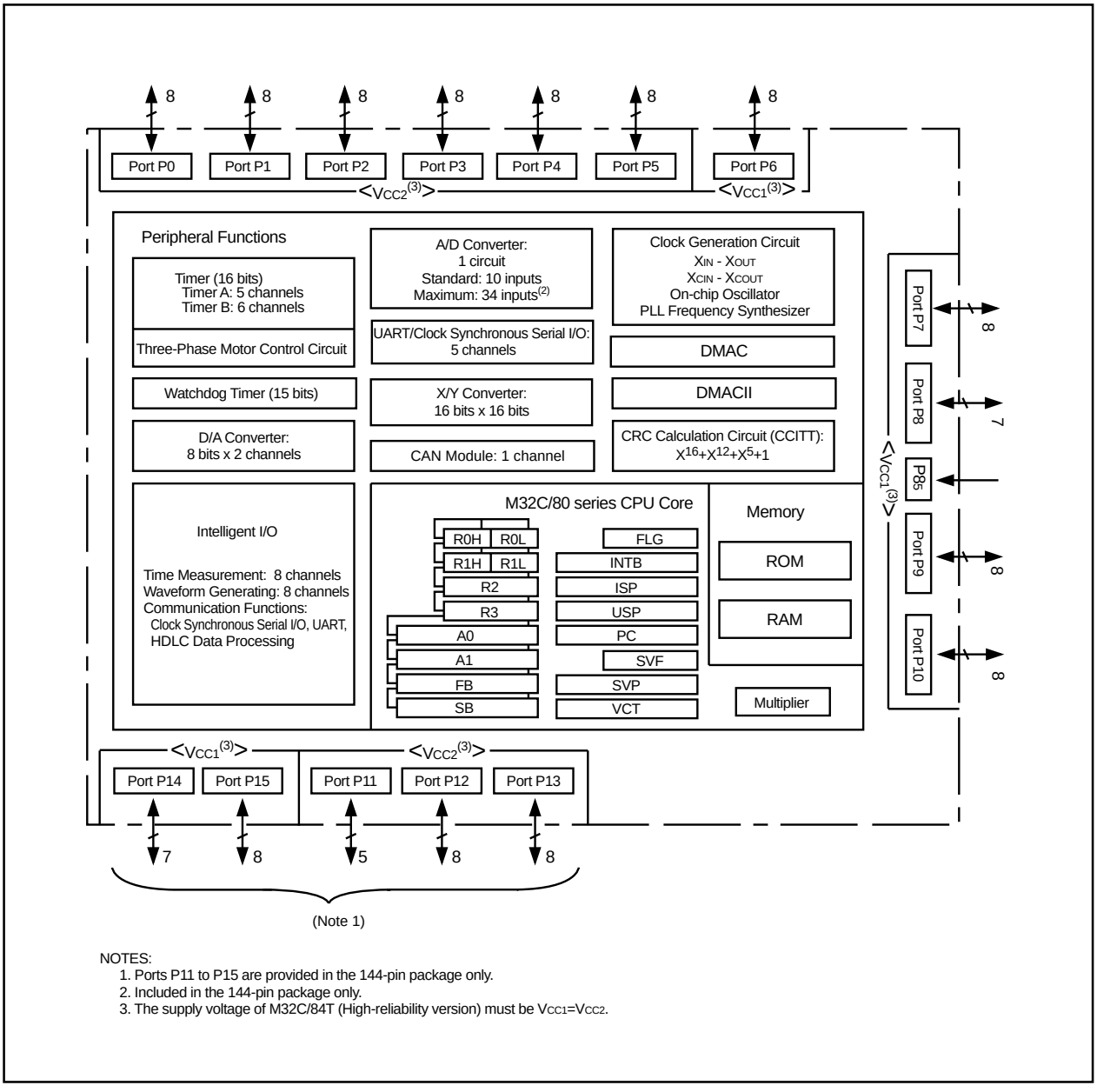
Characteristic		Performance	
		M32C/84	M32C/84T
CPU	Basic Instructions	108 instructions	
	Shortest Instruction Execution Time	31.3 ns (f(BCLK)=32 MHz, V_{CC1}=4.2 V to 5.5 V) 41.7 ns (f(BCLK)=24 MHz, V_{CC1}=3.0 V to 5.5 V)	31.3 ns (f(BCLK)=32 MHz, V_{CC1}=4.2 V to 5.5 V)
	Operation Mode	Single-chip mode, Memory expansion mode and Microprocessor mode	Single-chip mode
	Address Space	16 Mbytes	
	Memory Capacity	See Table 1.3	
Peripheral Function	I/O Port	123 I/O pins and 1 input pin	
	Multifunction Timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit	
	Intelligent I/O	Time measurement function or Waveform generating function: 16 bits x 8 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing)	
	Serial I/O	5 Channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus(1), I^2C bus(2)	
	CAN Module	1 channel Supporting CAN 2.0B specification	
	A/D Converter	10-bit A/D converter: 1 circuit, 34 channels	
	D/A Converter	8 bits x 2 channels	
	DMAC	4 channels	
	DMAC II	Can be activated by all peripheral function interrupt sources Immediate transfer, Calculation transfer and Chain transfer functions	
	CRC Calculation Circuit	CRC-CCITT	
	X/Y Converter	16 bits x 16 bits	
	Watchdog Timer	15 bits x 1 channel (with prescaler)	
	Interrupt	38 internal and 8 external sources, 5 software sources Interrupt priority level: 7	
	Clock Generation Circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally	
	Oscillation Stop Detect Function	Main clock oscillation stop detect function	
	Voltage Detection Circuit	Available (optional)	Not available(4)
Electrical Characteristics	Supply Voltage	V_{CC1}=4.2 V to 5.5 V, V_{CC2}=3.0 V to V_{CC1} (f(BCLK)=32 MHz) V_{CC1}=3.0 V to 5.5 V, V_{CC2}=3.0 V to V_{CC1} (f(BCLK)=24 MHz)	V_{CC1}=V_{CC2}=4.2 V to 5.5 V, (f(BCLK)=32 MHz)(3)
	Power Consumption	28 mA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 MHz) 22 mA (V_{CC1}=V_{CC2}=3.3 V, f(BCLK)=24 MHz) 10µA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 kHz, in wait mode)	28 mA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 MHz) 10µA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 kHz, in wait mode)
Flash Memory	Program/Erase Supply Voltage	3.3 V ± 0.3 V or 5.0 V ± 0.5 V	5.0 V ± 0.5 V
	Program and Erase Endurance	100 times (all space)	
Operating Ambient Temperature		–20 to 85°C –40 to 85°C (optional)	–40 to 85°C (T version)
Package		144-pin plastic molded LQFP	

NOTES:
1. IEBus is a trademark of NEC Electronics Corporation.
2. I^2C bus is a trademark of Koninklijke Philips Electronics N. V.
3. The supply voltage of M32C/84T (High-reliability version) must be V_{CC1}=V_{CC2}.
4. The cold start-up/warm start-up determine function is available only at the user's option.

All options are on a request basis.

1.3 Block Diagram

Figure 1.1 shows a block diagram of the M32C/84 group (M32C/84, M32C/84T) microcomputer.



NOTES:
1. Ports P11 to P15 are provided in the 144-pin package only.
2. Included in the 144-pin package only.
3. The supply voltage of M32C/84T (High-reliability version) must be V_{CC1}=V_{CC2}.

Figure 1.1 M32C/84 Group (M32C/84, M32C/84T) Block Diagram

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin
49		P13$_6$						
50		P13$_5$						
51		P13$_4$						
52		P5$_7$						$\overline{\text{RDY}}$
53		P5$_6$						ALE
54		P5$_5$						$\overline{\text{HOLD}}$
55		P5$_4$						$\overline{\text{HLDA}}$/ALE
56		P13$_3$						
57	V_{SS}							
58		P13$_2$						
59	V_{CC2}							
60		P13$_1$						
61		P13$_0$						
62		P5$_3$						CLK$_{OUT}$/BCLK/ALE
63		P5$_2$						$\overline{\text{RD}}$
64		P5$_1$						$\overline{\text{WRH}}$/$\overline{\text{BHE}}$
65		P5$_0$						$\overline{\text{WRL}}$/$\overline{\text{WR}}$
66		P12$_7$						
67		P12$_6$						
68		P12$_5$						
69		P4$_7$						$\overline{\text{CS0}}$/A$_{23}$
70		P4$_6$						$\overline{\text{CS1}}$/A$_{22}$
71		P4$_5$						$\overline{\text{CS2}}$/A$_{21}$
72		P4$_4$						$\overline{\text{CS3}}$/A$_{20}$
73		P4$_3$						A$_{19}$
74	V_{CC2}							
75		P4$_2$						A$_{18}$
76	V_{SS}							
77		P4$_1$						A$_{17}$
78		P4$_0$						A$_{16}$
79		P3$_7$						A$_{15}$(/D$_{15}$)
80		P3$_6$						A$_{14}$(/D$_{14}$)
81		P3$_5$						A$_{13}$(/D$_{13}$)
82		P3$_4$						A$_{12}$(/D$_{12}$)
83		P3$_3$						A$_{11}$(/D$_{11}$)
84		P3$_2$						A$_{10}$(/D$_{10}$)
85		P3$_1$						A$_9$(/D$_9$)
86		P12$_4$						
87		P12$_3$						
88		P12$_2$						
89		P12$_1$						
90		P12$_0$						
91	V_{CC2}							
92		P3$_0$						A$_8$(/D$_8$)
93	V_{SS}							
94		P2$_7$					AN2$_7$	A$_7$(/D$_7$)
95		P2$_6$					AN2$_6$	A$_6$(/D$_6$)
96		P2$_5$					AN2$_5$	A$_5$(/D$_5$)

NOTES:
1. Bus control pins in M32C/84T cannot be used.

1.6 Pin Description

Table 1.6 Pin Description (100-Pin and 144-Pin Packages)

Classsfication	Symbol	I/O Type	Supply Voltage	Function
Power Supply	V_{CC1}, V_{CC2} V_{SS}	I	–	Apply 3.0 to 5.5V to both V_{CC1} and V_{CC2} pins. Apply 0V to the V_{SS} pin. $V_{CC1} \geq V_{CC2}$(1, 2)
Analog Power Supply	AVCC AVSS	I	V_{CC1}	Supplies power to the A/D converter. Connect the AVCC pin to V_{CC1} and the AVSS pin to V_{SS}
Reset Input	$\overline{RESET}$	I	V_{CC1}	The microcomputer is in a reset state when "L" is applied to the $\overline{RESET}$ pin
CNVSS	CNVSS	I	V_{CC1}	Switches processor mode. Connect the CNVSS pin to V_{SS} to start up in single-chip mode or to V_{CC1} to start up in microprocessor mode
Input to Switch External Data Bus Width(3)	BYTE	I	V_{CC1}	Switches data bus width in external memory space 3. The data bus is 16 bits wide when the BYTE pin is held "L" and 8 bits wide when it is held "H". Set to either. Connect the BYTE pin to V_{SS} to use the microcomputer in single-chip mode
Bus Control Pins(3)	D_0 to D_7	I/O	V_{CC2}	Inputs and outputs data (D_0 to D_7) while accessing an external memory space with separate bus
	D_8 to D_{15}	I/O	V_{CC2}	Inputs and outputs data (D_8 to D_{15}) while accessing an external memory space with 16-bit separate bus
	A_0 to A_{22}	O	V_{CC2}	Outputs address bits A_0 to A_{22}
	$\overline{A_{23}}$	O	V_{CC2}	Outputs inversed address bit A_{23}
	A_0/D_0 to A_7/D_7	I/O	V_{CC2}	Inputs and outputs data (D_0 to D_7) and outputs 8 low-order address bits (A_0 to A_7) by time-sharing while accessing an external memory space with multiplexed bus
	A_8/D_8 to A_{15}/D_{15}	I/O	V_{CC2}	Inputs and outputs data (D_8 to D_{15}) and outputs 8 middle-order address bits (A_8 to A_{15}) by time-sharing while accessing an external memory space with 16-bit multiplexed bus
	$\overline{CS0}$ to $\overline{CS3}$	O	V_{CC2}	Outputs $\overline{CS0}$ to $\overline{CS3}$ that are chip-select signals specifying an external space
	$\overline{WRL}$ / $\overline{WR}$ $\overline{WRH}$ / $\overline{BHE}$ $\overline{RD}$	O	V_{CC2}	Outputs $\overline{WRL}$, $\overline{WRH}$, ($\overline{WR}$, $\overline{BHE}$) and $\overline{RD}$ signals. $\overline{WRL}$ and $\overline{WRH}$ can be switched with $\overline{WR}$ and $\overline{BHE}$ by program ■ $\overline{WRL}$, $\overline{WRH}$ and $\overline{RD}$ selected: If external data bus is 16 bits wide, data is written to an even address in external memory space when $\overline{WRL}$ is held "L". Data is written to an odd address when $\overline{WRH}$ is held "L". Data is read when $\overline{RD}$ is held "L". ■ $\overline{WR}$, $\overline{BHE}$ and $\overline{RD}$ selected: Data is written to external memory space when $\overline{WR}$ is held "L". Data in an external memory space is read when $\overline{RD}$ is held "L". An odd address is accessed when $\overline{BHE}$ is held "L". Select $\overline{WR}$, $\overline{BHE}$ and $\overline{RD}$ for external 8-bit data bus.
	ALE	O	V_{CC2}	ALE is a signal latching the address
	$\overline{HOLD}$	I	V_{CC2}	The microcomputer is placed in a hold state while the $\overline{HOLD}$ pin is held "L"
	$\overline{HLDA}$	O	V_{CC2}	Outputs an "L" signal while the microcomputer is placed in a hold state
	$\overline{RDY}$	I	V_{CC2}	Bus is placed in a wait state while the $\overline{RDY}$ pin is held "L"

I : Input O : Output I/O : Input and output

NOTES:
1. V_{CC1} is hereinafter referred to as V_{CC} unless otherwise noted.
2. Apply 4.2 to 5.5V to the V_{CC1} and V_{CC2} pins when using M32C/84T. V_{CC1}=V_{CC2}.
3. Bus cotrol pins in M32C/84T cannot be used.

3. Memory

Figure 3.1 shows a memory map of the M32C/84 group (M32C/84, M32C/84T).

The M32C/84 group (M32C/84, M32C/84T) provides 16-Mbyte address space from addresses 000000$_{16}$ to FFFFFF$_{16}$.

The internal ROM is allocated lower addresses beginning with address FFFFFF$_{16}$. For example, a 64-Kbyte internal ROM is allocated in addresses FF0000$_{16}$ to FFFFFF$_{16}$.

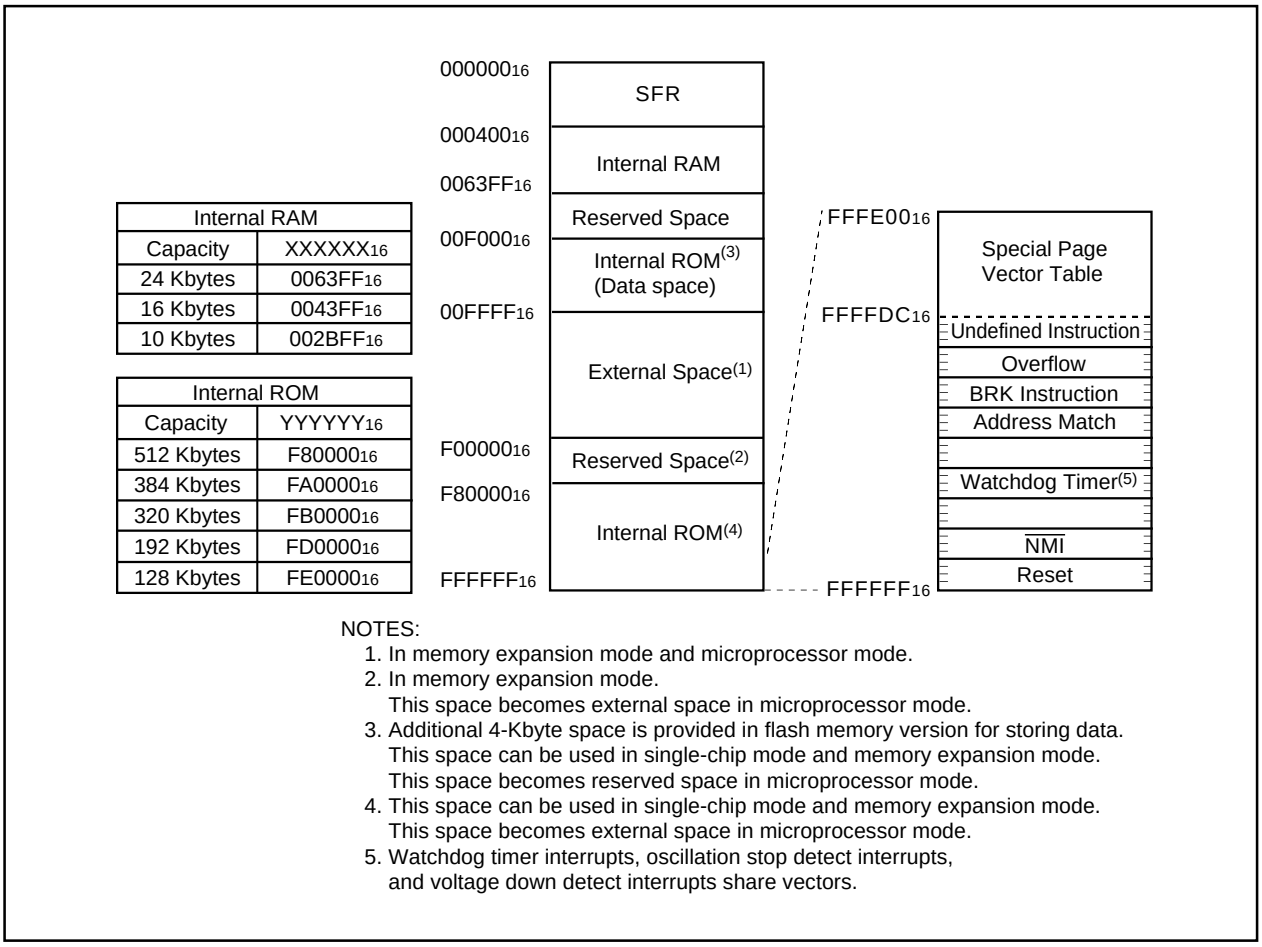
The fixed interrupt vectors are allocated addresses FFFFDC$_{16}$ to FFFFFF$_{16}$. It stores the starting address of each interrupt routine.

The internal RAM is allocated higher addresses beginning with address 000400$_{16}$. For example, a 10-Kbyte internal RAM is allocated addresses 000400$_{16}$ to 002BFF$_{16}$. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowleged.

SFR, consisting of control registers for peripheral functions such as I/O port, A/D converter, serial I/O, and timers, is allocated addresses 000000$_{16}$ to 0003FF$_{16}$. All blank spaces within SFR are reserved and cannot be accessed by users.

The special page vectors are allocated addresses FFFE00$_{16}$ to FFFFDB$_{16}$. It is used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **M32C/80 Series Software Manual** for details.

In memory expansion mode and microprocessor mode, some spaces are reserved and cannot be accessed by users.



Internal RAM	
Capacity	XXXXXX$_{16}$
24 Kbytes	0063FF$_{16}$
16 Kbytes	0043FF$_{16}$
10 Kbytes	002BFF$_{16}$

Internal ROM	
Capacity	YYYYYY$_{16}$
512 Kbytes	F80000$_{16}$
384 Kbytes	FA0000$_{16}$
320 Kbytes	FB0000$_{16}$
192 Kbytes	FD0000$_{16}$
128 Kbytes	FE0000$_{16}$

NOTES:
1. In memory expansion mode and microprocessor mode.
2. In memory expansion mode.
   This space becomes external space in microprocessor mode.
3. Additional 4-Kbyte space is provided in flash memory version for storing data.
   This space can be used in single-chip mode and memory expansion mode.
   This space becomes reserved space in microprocessor mode.
4. This space can be used in single-chip mode and memory expansion mode.
   This space becomes external space in microprocessor mode.
5. Watchdog timer interrupts, oscillation stop detect interrupts, and voltage down detect interrupts share vectors.

Figure 3.1 Memory Map

Address	Register	Symbol	Value after RESET
0030₁₆			
0031₁₆			
0032₁₆			
0033₁₆			
0034₁₆			
0035₁₆			
0036₁₆			
0037₁₆			
0038₁₆ 0039₁₆ 003A₁₆	Address Match Interrupt Register 6	RMAD6	000000₁₆
003B₁₆			
003C₁₆ 003D₁₆ 003E₁₆	Address Match Interrupt Register 7	RMAD7	000000₁₆
003F₁₆			
0040₁₆			
0041₁₆			
0042₁₆			
0043₁₆			
0044₁₆			
0045₁₆			
0046₁₆			
0047₁₆			
0048₁₆	External Space Wait Control Register 0(1)	EWCR0	X0X0 0011₂
0049₁₆	External Space Wait Control Register 1(1)	EWCR1	X0X0 0011₂
004A₁₆	External Space Wait Control Register 2(1)	EWCR2	X0X0 0011₂
004B₁₆	External Space Wait Control Register 3(1)	EWCR3	X0X0 0011₂
004C₁₆	Page Mode Wait Control Register 0(2)	PWCR0	0001 0001₂
004D₁₆	Page Mode Wait Control Register 1(2)	PWCR1	0001 0001₂
004E₁₆			
004F₁₆			
0050₁₆			
0051₁₆			
0052₁₆			
0053₁₆			
0054₁₆			
0055₁₆	Flash Memory Control Register 1	FMR1	0000 0101₂
0056₁₆			
0057₁₆	Flash Memory Control Register 0	FMR0	0000 0001₂(Flash memory version) XXXX XXX0₂(Masked ROM version)
0058₁₆			
0059₁₆			
005A₁₆			
005B₁₆			
005C₁₆			
005D₁₆			
005E₁₆			
005F₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. These registers in M32C/84T cannot be used.
2. These registers can be used only in the ROMless version.

Address	Register	Symbol	Value after RESET
00F0$_{16}$	Data Compare Register 00	G0CMP0	XX$_{16}$
00F1$_{16}$	Data Compare Register 01	G0CMP1	XX$_{16}$
00F2$_{16}$	Data Compare Register 02	G0CMP2	XX$_{16}$
00F3$_{16}$	Data Compare Register 03	G0CMP3	XX$_{16}$
00F4$_{16}$	Data Mask Register 00	G0MSK0	XX$_{16}$
00F5$_{16}$	Data Mask Register 01	G0MSK1	XX$_{16}$
00F6$_{16}$	Communication Clock Select Register	CCS	XXXX 0000$_2$
00F7$_{16}$			
00F8$_{16}$ 00F9$_{16}$	Receive CRC Code Register 0	G0RCRC	XX$_{16}$ XX$_{16}$
00FA$_{16}$ 00FB$_{16}$	Transmit CRC Code Register 0	G0TCRC	00$_{16}$ 00$_{16}$
00FC$_{16}$	SI/O Extended Mode Register 0	G0EMR	00$_{16}$
00FD$_{16}$	SI/O Extended Receive Control Register 0	G0ERC	00$_{16}$
00FE$_{16}$	SI/O Special Communication Interrupt Detect Register 0	G0IRF	00$_{16}$
00FF$_{16}$	SI/O Extended Transmit Control Register 0	G0ETC	0000 0XXX$_2$
0100$_{16}$ 0101$_{16}$	Time Measurement/Waveform Generating Register 10	G1TM0/G1PO0	XX$_{16}$ XX$_{16}$
0102$_{16}$ 0103$_{16}$	Time Measurement/Waveform Generating Register 11	G1TM1/G1PO1	XX$_{16}$ XX$_{16}$
0104$_{16}$ 0105$_{16}$	Time Measurement/Waveform Generating Register 12	G1TM2/G1PO2	XX$_{16}$ XX$_{16}$
0106$_{16}$ 0107$_{16}$	Time Measurement/Waveform Generating Register 13	G1TM3/G1PO3	XX$_{16}$ XX$_{16}$
0108$_{16}$ 0109$_{16}$	Time Measurement/Waveform Generating Register 14	G1TM4/G1PO4	XX$_{16}$ XX$_{16}$
010A$_{16}$ 010B$_{16}$	Time Measurement/Waveform Generating Register 15	G1TM5/G1PO5	XX$_{16}$ XX$_{16}$
010C$_{16}$ 010D$_{16}$	Time Measurement/Waveform Generating Register 16	G1TM6/G1PO6	XX$_{16}$ XX$_{16}$
010E$_{16}$ 010F$_{16}$	Time Measurement/Waveform Generating Register 17	G1TM7/G1PO7	XX$_{16}$ XX$_{16}$
0110$_{16}$	Waveform Generating Control Register 10	G1POCR0	0000 X000$_2$
0111$_{16}$	Waveform Generating Control Register 11	G1POCR1	0X00 X000$_2$
0112$_{16}$	Waveform Generating Control Register 12	G1POCR2	0X00 X000$_2$
0113$_{16}$	Waveform Generating Control Register 13	G1POCR3	0X00 X000$_2$
0114$_{16}$	Waveform Generating Control Register 14	G1POCR4	0X00 X000$_2$
0115$_{16}$	Waveform Generating Control Register 15	G1POCR5	0X00 X000$_2$
0116$_{16}$	Waveform Generating Control Register 16	G1POCR6	0X00 X000$_2$
0117$_{16}$	Waveform Generating Control Register 17	G1POCR7	0X00 X000$_2$
0118$_{16}$	Time Measurement Control Register 10	G1TMCR0	00$_{16}$
0119$_{16}$	Time Measurement Control Register 11	G1TMCR1	00$_{16}$
011A$_{16}$	Time Measurement Control Register 12	G1TMCR2	00$_{16}$
011B$_{16}$	Time Measurement Control Register 13	G1TMCR3	00$_{16}$
011C$_{16}$	Time Measurement Control Register 14	G1TMCR4	00$_{16}$
011D$_{16}$	Time Measurement Control Register 15	G1TMCR5	00$_{16}$
011E$_{16}$	Time Measurement Control Register 16	G1TMCR6	00$_{16}$
011F$_{16}$	Time Measurement Control Register 17	G1TMCR7	00$_{16}$

X: Indeterminate

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Address	Register	Symbol	Value after RESET
012016	Base Timer Register 1	G1BT	XX16
012116			XX16
012216	Base Timer Control Register 10	G1BCR0	0016
012316	Base Timer Control Register 11	G1BCR1	X000 000X2
012416	Time Measurement Prescaler Register 16	G1TPR6	0016
012516	Time Measurement Prescaler Register 17	G1TPR7	0016
012616	Function Enable Register 1	G1FE	0016
012716	Function Select Register 1	G1FS	0016
012816	SI/O Receive Buffer Register 1	G1RB	XXXX XXXX2
012916			X000 XXXX2
012A16	Transmit Buffer/Receive Data Register 1	G1TB/G1DR	XX16
012B16			
012C16	Receive Input Register 1	G1RI	XX16
012D16	SI/O Communication Mode Register 1	G1MR	0016
012E16	Transmit Output Register 1	G1TO	XX16
012F16	SI/O Communication Control Register 1	G1CR	0000 X0112
013016	Data Compare Register 10	G1CMP0	XX16
013116	Data Compare Register 11	G1CMP1	XX16
013216	Data Compare Register 12	G1CMP2	XX16
013316	Data Compare Register 13	G1CMP3	XX16
013416	Data Mask Register 10	G1MSK0	XX16
013516	Data Mask Register 11	G1MSK1	XX16
013616			
013716			
013816	Receive CRC Code Register 1	G1RCRC	XX16
013916			XX16
013A16	Transmit CRC Code Register 1	G1TCRC	0016
013B16			0016
013C16	SI/O Extended Mode Register 1	G1EMR	0016
013D16	SI/O Extended Receive Control Register 1	G1ERC	0016
013E16	SI/O Special Communication Interrupt Detect Register 1	G1IRF	0016
013F16	SI/O Extended Transmit Control Register 1	G1ETC	0000 0XXX2
014016			
014116			
014216			
014316			
014416			
014516			
014616			
014716			
014816			
014916			
014A16			
014B16			
014C16			
014D16			
014E16			
014F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
02F0₁₆			
02F1₁₆			
02F2₁₆			
02F3₁₆			
02F4₁₆	UART4 Special Mode Register 4	U4SMR4	00₁₆
02F5₁₆	UART4 Special Mode Register 3	U4SMR3	00₁₆
02F6₁₆	UART4 Special Mode Register 2	U4SMR2	00₁₆
02F7₁₆	UART4 Special Mode Register	U4SMR	00₁₆
02F8₁₆	UART4 Transmit/Receive Mode Register	U4MR	00₁₆
02F9₁₆	UART4 Bit Rate Register	U4BRG	XX₁₆
02FA₁₆	UART4 Transmit Buffer Register	U4TB	XX₁₆
02FB₁₆			XX₁₆
02FC₁₆	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000₂
02FD₁₆	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010₂
02FE₁₆	UART4 Receive Buffer Register	U4RB	XX₁₆
02FF₁₆			XX₁₆
0300₁₆	Timer B3, B4, B5 Count Start Flag	TBSR	000X XXXX₂
0301₁₆			
0302₁₆	Timer A1-1 Register	TA11	XX₁₆
0303₁₆			XX₁₆
0304₁₆	Timer A2-1 Register	TA21	XX₁₆
0305₁₆			XX₁₆
0306₁₆	Timer A4-1 Register	TA41	XX₁₆
0307₁₆			XX₁₆
0308₁₆	Three-Phase PWM Control Register 0	INVC0	00₁₆
0309₁₆	Three-Phase PWM Control Register 1	INVC1	00₁₆
030A₁₆	Three-Phase Output Buffer Register 0	IDB0	XX11 1111₂
030B₁₆	Three-Phase Output Buffer Register 1	IDB1	XX11 1111₂
030C₁₆	Dead Time Timer	DTT	XX₁₆
030D₁₆	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XX₁₆
030E₁₆			
030F₁₆			
0310₁₆	Timer B3 Register	TB3	XX₁₆
0311₁₆			XX₁₆
0312₁₆	Timer B4 Register	TB4	XX₁₆
0313₁₆			XX₁₆
0314₁₆	Timer B5 Register	TB5	XX₁₆
0315₁₆			XX₁₆
0316₁₆			
0317₁₆			
0318₁₆			
0319₁₆			
031A₁₆			
031B₁₆	Timer B3 Mode Register	TB3MR	00XX 0000₂
031C₁₆	Timer B4 Mode Register	TB4MR	00XX 0000₂
031D₁₆	Timer B5 Mode Register	TB5MR	00XX 0000₂
031E₁₆			
031F₁₆	External Interrupt Cause Select Register	IFSR	00₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
038016 038116	A/D0 Register 0	AD00	XXXX XXXX2 0000 00002
038216 038316	A/D0 Register 1	AD01	XX16 XX16
038416 038516	A/D0 Register 2	AD02	XX16 XX16
038616 038716	A/D0 Register 3	AD03	XX16 XX16
038816 038916	A/D0 Register 4	AD04	XX16 XX16
038A16 038B16	A/D0 Register 5	AD05	XX16 XX16
038C16 038D16	A/D0 Register 6	AD06	XX16 XX16
038E16 038F16	A/D0 Register 7	AD07	XX16 XX16
039016			
039116			
039216	A/D0 Control Register 4	AD0CON4	XXXX 00XX2
039316			
039416	A/D0 Control Register 2	AD0CON2	XX0X X0002
039516	A/D0 Control Register 3	AD0CON3	XXXX X0002
039616	A/D0 Control Register 0	AD0CON0	0016
039716	A/D0 Control Register 1	AD0CON1	0016
039816	D/A Register 0	DA0	XX16
039916			
039A16	D/A Register 1	DA1	XX16
039B16			
039C16	D/A Control Register	DACON	XXXX XX002
039D16			
039E16			
039F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<144-pin Package>

Address	Register	Symbol	Value after RESET
03D0₁₆	Port P14 Register	P14	XX₁₆
03D1₁₆	Port P15 Register	P15	XX₁₆
03D2₁₆	Port P14 Direction Register	PD14	X000 0000₂
03D3₁₆	Port P15 Direction Register	PD15	00₁₆
03D4₁₆			
03D5₁₆			
03D6₁₆			
03D7₁₆			
03D8₁₆			
03D9₁₆			
03DA₁₆	Pull-Up Control Register 2	PUR2	00₁₆
03DB₁₆	Pull-Up Control Register 3	PUR3	00₁₆
03DC₁₆	Pull-Up Control Register 4	PUR4	XXXX 0000₂
03DD₁₆			
03DE₁₆			
03DF₁₆			
03E0₁₆	Port P0 Register	P0	XX₁₆
03E1₁₆	Port P1 Register	P1	XX₁₆
03E2₁₆	Port P0 Direction Register	PD0	00₁₆
03E3₁₆	Port P1 Direction Register	PD1	00₁₆
03E4₁₆	Port P2 Register	P2	XX₁₆
03E5₁₆	Port P3 Register	P3	XX₁₆
03E6₁₆	Port P2 Direction Register	PD2	00₁₆
03E7₁₆	Port P3 Direction Register	PD3	00₁₆
03E8₁₆	Port P4 Register	P4	XX₁₆
03E9₁₆	Port P5 Register	P5	XX₁₆
03EA₁₆	Port P4 Direction Register	PD4	00₁₆
03EB₁₆	Port P5 Direction Register	PD5	00₁₆
03EC₁₆			
03ED₁₆			
03EE₁₆			
03EF₁₆			
03F0₁₆	Pull-Up Control Register 0	PUR0	00₁₆
03F1₁₆	Pull-Up Control Register 1	PUR1	XXXX 0000₂
03F2₁₆			
03F3₁₆			
03F4₁₆			
03F5₁₆			
03F6₁₆			
03F7₁₆			
03F8₁₆			
03F9₁₆			
03FA₁₆			
03FB₁₆			
03FC₁₆			
03FD₁₆			
03FE₁₆			
03FF₁₆	Port Control Register	PCR	XXXX XXX0₂

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Table 5.2 Recommended Operating Conditions (Continued)
(V_{CC1}=V_{CC2}=3.0V to 5.5V at Topr=–20 to 85°C unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$f(BCLK)$	CPU Clock Frequency	V_{CC1}=4.2 to 5.5V	0		32	MHz
		V_{CC1}=3.0 to 5.5V	0		24	MHz
$f(X_{IN})$	Main Clock Input Frequency	V_{CC1}=4.2 to 5.5V	0		32	MHz
		V_{CC1}=3.0 to 5.5V	0		24	MHz
$f(X_{CIN})$	Sub Clock Frequency			32.768	50	kHz
$f(Ring)$	On-chip Oscillator Frequency (V_{CC1}=V_{CC2}=5.0V, Topr=25° C)		0.5	1	2	MHz
$f(PLL)$	PLL Clock Frequency	V_{CC1}=4.2 to 5.5V	10		32	MHz
		V_{CC1}=3.0 to 5.5V	10		24	MHz
$t_{SU(PLL)}$	Wait Time to Stabilize PLL Frequency Synthesizer	V_{CC1}=5.0V			5	ms
		V_{CC1}=3.3V			10	ms

$V_{CC1}=V_{CC2}=5V$

Table 5.4 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=AV_{CC}=V_{REF}$=4.2 to 5.5V, V_{SS}= AV_{SS} = 0V at Topr=–20 to 85°C, f(BCLK) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
-	Resolution	$V_{REF}=V_{CC1}$				10	Bits
INL	Integral Nonlinearity Error	$V_{REF}=V_{CC1}=V_{CC2}$=5V	AN_0 to AN_7, $AN0_0$ to $AN0_7$, $AN2_0$ to $AN2_7$, $AN15_0$ to $AN15_7$, ANEX0, ANEX1			±3	LSB
							LSB
			External op-amp connection mode			±7	LSB
							LSB
DNL	Differential Nonlinearity Error					±1	LSB
-	Offset Error					±3	LSB
-	Gain Error					±3	LSB
R_{LADDER}	Resistor Ladder	$V_{REF}=V_{CC1}$		8		40	kΩ
t_{CONV}	10-bit Conversion Time(1, 2)			2.06			µs
t_{CONV}	8-bit Conversion Time(1, 2)			1.75			µs
t_{SAMP}	Sampling Time(1)			0.188			µs
V_{REF}	Reference Voltage			2		V_{CC1}	V
V_{IA}	Analog Input Voltage			0		V_{REF}	V

NOTES:
1. Divide f(X_{IN}), if exceeding 16 MHz, to keep ϕAD frequency at 16 MHz or less.
2. With using the sample and hold function.

Table 5.5 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=V_{REF}$=4.2 to 5.5V, $V_{SS}=AV_{SS}$=0V at Topr=–20 to 85°C, f(BCLK) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTES:
1. Measurement when using one D/A converter. The DAi register (i=0, 1) of the D/A converter, not being used, is set to "00_{16}". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr=–20 to 85°C unless otherwise specified)

Table 5.11 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	100		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	40		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	40		ns

Table 5.12 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	400		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	200		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	200		ns

Table 5.13 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	200		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 5.14 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 5.15 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAiOUT Input High ("H") Width	1000		ns
$t_{w(UPL)}$	TAiOUT Input Low ("L") Width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAiOUT Input Hold Time	400		ns

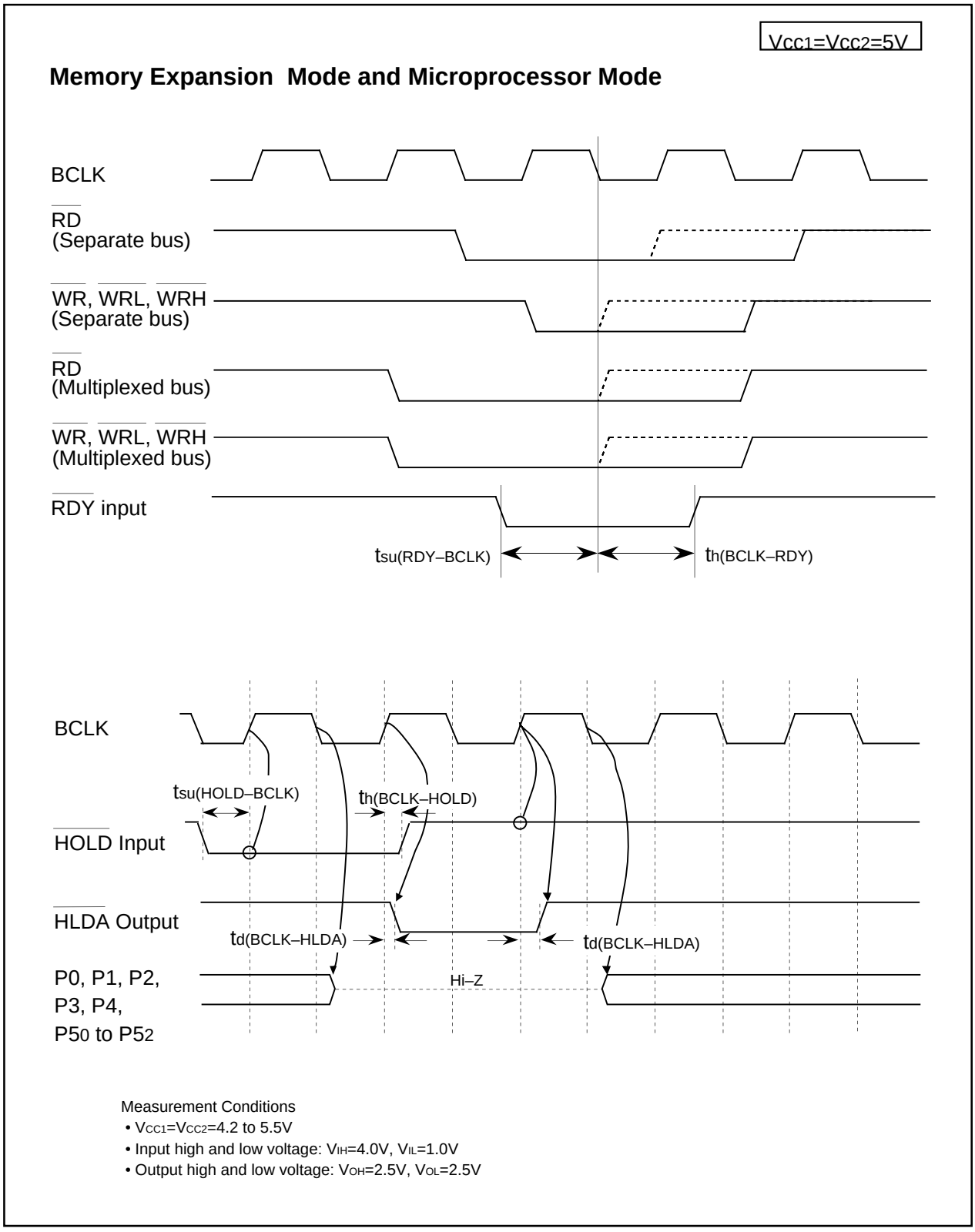


Figure 5.6 Vcc1=Vcc2=5V Timing Diagram (4)

$V_{CC1}=V_{CC2}=3.3V$

Timing Requirements

($V_{CC1}=V_{CC2}$= 3.0 to 3.6V, V_{SS}= 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.29 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	100		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	40		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	40		ns

Table 5.30 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	400		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	200		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	200		ns

Table 5.31 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	200		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	100		ns

Table 5.32 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	100		ns

Table 5.33 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAi_{OUT} Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAi_{OUT} Input High ("H") Width	1000		ns
$t_{w(UPL)}$	TAi_{OUT} Input Low ("L") Width	1000		ns
$t_{su(UP-TIN)}$	TAi_{OUT} Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAi_{OUT} Input Hold Time	400		ns

$V_{CC1}=V_{CC2}=3.3V$

Switching Characteristics

($V_{CC1}=V_{CC2}$=3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.40 Memory Expansion Mode and Microprocessor Mode (when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 5.2		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)(3)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)(3)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-Select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-Select Signal Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-CS)}$	Chip-Select Signal Output Hold Time (RD standard)(3)		0		ns
$t_{h(WR-CS)}$	Chip-Select Signal Output Hold Time (WR standard)(3)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-3		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		0		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 2)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard)(3)		(Note 1)		ns
$t_{w(WR)}$	WR Output Width		(Note 2)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 20 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles.

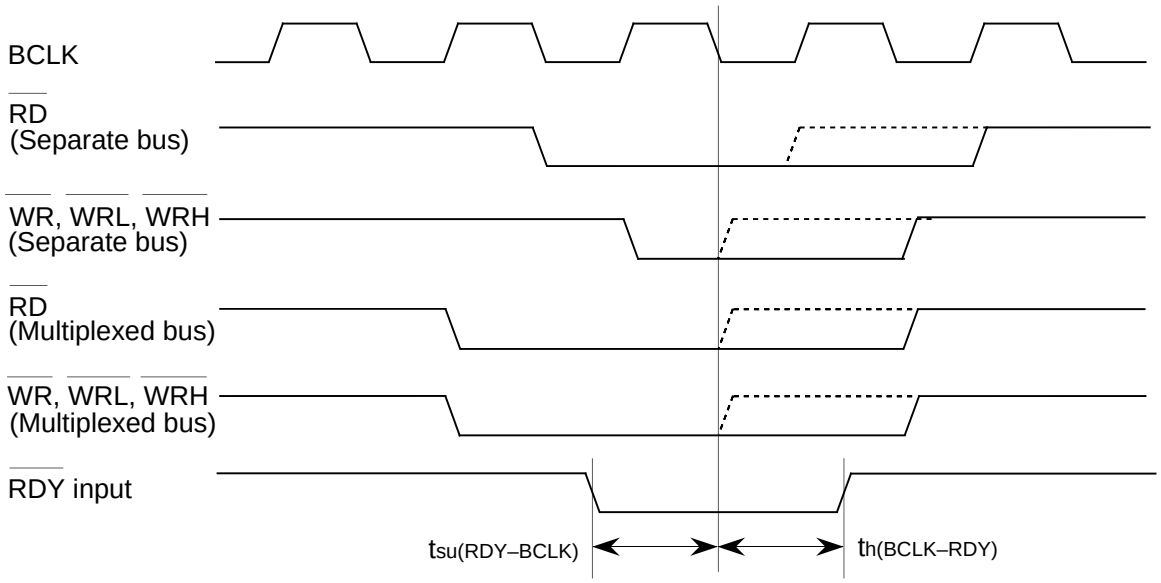
$$t_{w(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [ns] \quad \text{(if external bus cycle is } a\phi + b\phi\text{, n=(b x 2)-1)}$$

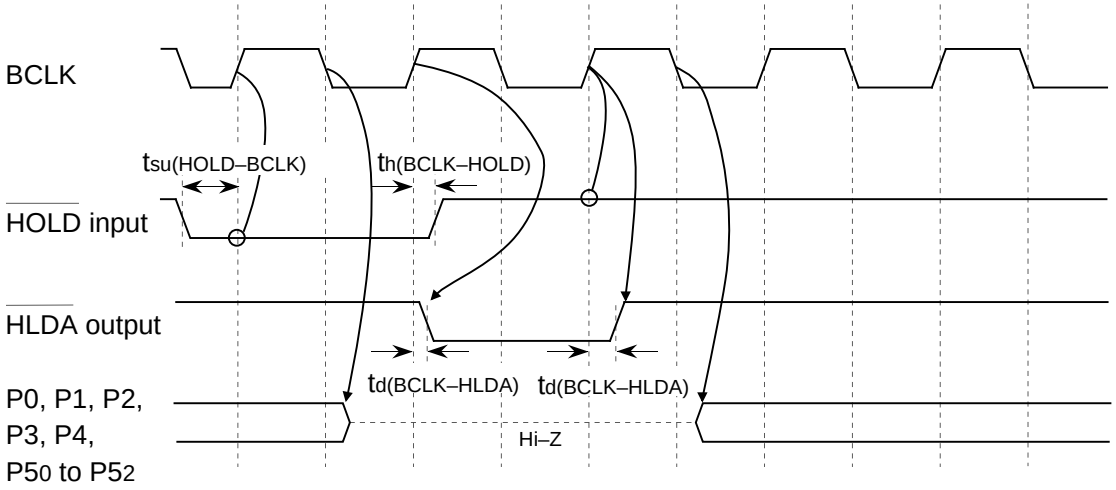
$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)}} - 20 \quad [ns] \quad \text{(if external bus cycle is } a\phi + b\phi\text{, m=b)}$$

3. *tc* ns is added when recovery cycle is inserted.

$V_{CC1}=V_{CC2}=3.3V$

Memory Expansion Mode and Microprocessor Mode





Measurement Conditions:
- $V_{CC1}=V_{CC2}=3.0$ to 3.6V
- Input high and low voltage: $V_{IH}=2.4V$, $V_{IL}=0.6V$
- Output high and low voltage: $V_{OH}=1.5V$, $V_{OL}=1.5V$

Figure 5.10 $V_{CC1}=V_{CC2}=3.3V$ Timing Diagram (4)

5.2 Electrical Characteristics (M32C/84T)

Table 5.42 Absolute Maximum Ratings

Symbol	Parameter		Condition	Value	Unit
V_{CC1}, V_{CC2}	Supply Voltage		V_{CC1}=V_{CC2}=AVcc	-0.3 to 6.0	V
AVcc	Analog Supply Voltage		V_{CC1}=V_{CC2}=AVcc	-0.3 to 6.0	V
V_I	Input Voltage	$\overline{RESET}$, CNVss, BYTE, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), V_{REF}, X_{IN}		-0.3 to V_{CC1}+0.3	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$(1)		-0.3 to V_{CC2}+0.3	
		$P7_0$, $P7_1$		-0.3 to 6.0	
V_O	Output Voltage	$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{OUT}		-0.3 to V_{CC1}+0.3	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$(1)		-0.3 to V_{CC2}+0.3	
		$P7_0$, $P7_1$		-0.3 to 6.0	
Pd	Power Dissipation		Topr=25° C	500	mW
Topr	Operating Ambient Temperature	during CPU operation	T version	-40 to 85	° C
		during flash memory program and erase operation		0 to 60	
Tstg	Storage Temperature			-65 to 150	° C

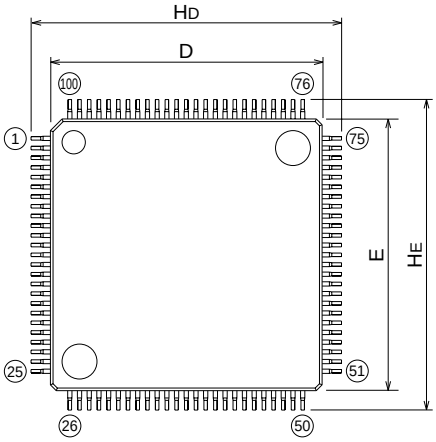
NOTES:

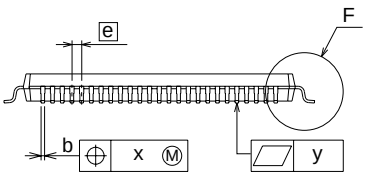
1. P11 to P15 are provided in the 144-pin package only.

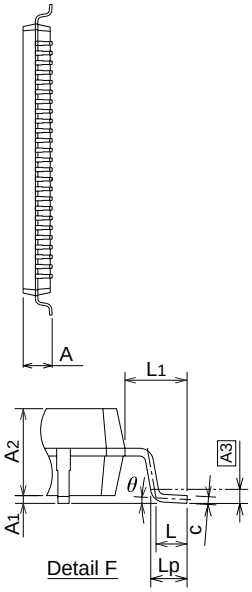
PLQP0100KB-A (100P6Q-A)

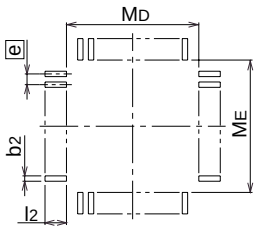
Plastic 100pin 14×14mm body LQFP

JEITA Package Code	RENESAS Code	Previous Code	Mass[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A	0.6g









Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	13.9	14.0	14.1
e	–	0.5	–
HD	15.8	16.0	16.2
HE	15.8	16.0	16.2
L	0.3	0.5	0.7
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	10°
b2	–	0.225	–
l2	0.9	–	–
MD	–	14.4	–
ME	–	14.4	–