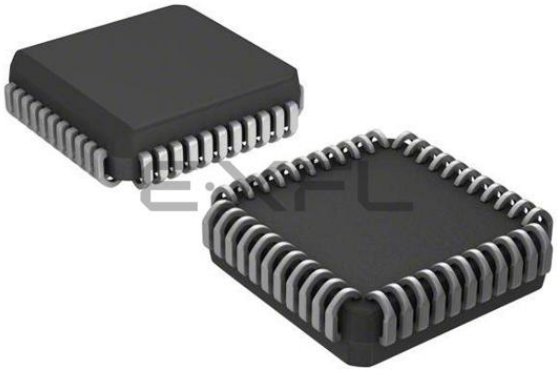

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	30/20MHz
Connectivity	UART/USART
Peripherals	POR
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at80c31x2-slrul

4. SFR Mapping

The Special Function Registers (SFRs) of the TS80C31X2 fall into the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP, AUXR1
- I/O port registers: P0, P1, P2, P3
- Timer registers: TCON, TH0, TH1, TMOD, TL0, TL1
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON
- Power and clock control registers: PCON
- Interrupt system registers: IE, IP, IPH
- Others: CKCON

Table 4-1. All SFRs with their address and their reset value

	Bit addressable	**Non Bit addressable**							
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h									FFh
F0h	B 0000 0000								F7h
E8h									EFh
E0h	ACC 0000 0000								E7h
D8h									DFh
D0h	PSW 0000 0000								D7h
C8h									CFh
C0h									C7h
B8h	IP XXX0 0000	SADEN 0000 0000							BFh
B0h	P3 1111 1111							IPH XXX0 0000	B7h
A8h	IE 0XX0 0000	SADDR 0000 0000							AFh
A0h	P2 1111 1111		AUXR1 XXXX XXX0						A7h
98h	SCON 0000 0000	SBUF XXXX XXXX							9Fh
90h	P1 1111 1111								97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000		CKCON XXXX XXX0	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Reserved

Mnemonic	Pin Number			Type	Name And Function
	DIL	LCC	VQFP 1.4		
V_{SS}	20	22	16	I	**Ground:** 0V reference
Vss1		1	39	I	Optional Ground: **Contact the Sales Office for ground connection.**
V_{CC}	40	44	38	I	**Power Supply:** This is the power supply voltage for normal, idle and power-down operation
P0.0-P0.7	39-32	43-36	37-30	I/O	**Port 0**: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. Port 0 pins must be polarized to Vcc or Vss in order to prevent any parasitic current consumption. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-up when emitting 1s.
P1.0-P1.7	1-8	2-9	40-44 1-3	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups.
P2.0-P2.7	21-28	24-31	18-25	I/O	**Port 2**: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR).In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 emits the contents of the P2 SFR.
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Port 3 also serves the special features of the 80C51 family, as listed below.
	10	11	5	I	**RXD (P3.0):** Serial input port
	11	13	7	O	**TXD (P3.1):** Serial output port
	12	14	8	I	**$\overline{\text{INT0}}$ (P3.2):** External interrupt 0
	13	15	9	I	**$\overline{\text{INT1}}$ (P3.3):** External interrupt 1
	14	16	10	I	**T0 (P3.4):** Timer 0 external input
	15	17	11	I	**T1 (P3.5):** Timer 1 external input
	16	18	12	O	**$\overline{\text{WR}}$ (P3.6):** External data memory write strobe
	17	19	13	O	**$\overline{\text{RD}}$ (P3.7):** External data memory read strobe
Reset	9	10	4	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC}.
ALE	30	33	27	O (I)	**Address Latch Enable:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory.
PSEN	29	32	26	O	**Program Store ENable:** The read strobe to external program memory. When executing code from the external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory.

EA	31	35	29	I	**External Access Enable:** $\overline{EA}$ must be externally held low to enable the device to fetch code from external program memory locations.
XTAL1	19	21	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	**Crystal 2:** Output from the inverting oscillator amplifier

6. TS80C31X2 Enhanced Features

In comparison to the original 80C31, the TS80C31X2 implements some new features, which are:

- The X2 option.
- The Dual Data Pointer.
- The 4 level interrupt priority system.
- The power-off flag.
- The ONCE mode.
- Enhanced UART

6.1 X2 Feature

The TS80C31X2 core needs only 6 clock periods per machine cycle. This feature called "X2" provides the following advantages:

- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power.
- Save power consumption while keeping same CPU power (oscillator power saving).
- Save power consumption by dividing dynamically operating frequency by 2 in operating and idle modes.
- Increase CPU power by 2 while keeping same crystal frequency.

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

6.1.1 Description

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 6-1. shows the clock generation block diagram. X2 bit is validated on XTAL1÷2 rising edge to avoid glitches when switching from X2 to STD mode. Figure 6-2. shows the mode switching waveforms.

Figure 6-1. Clock Generation Diagram

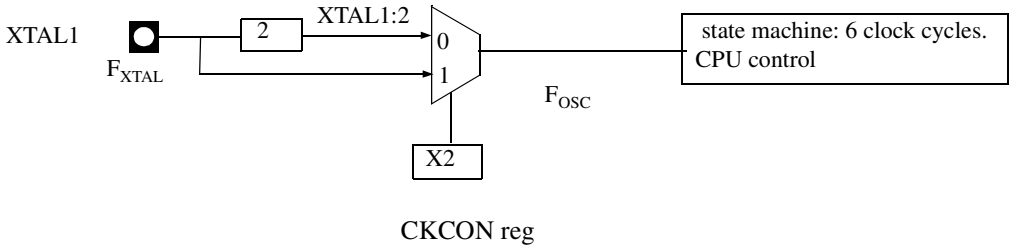
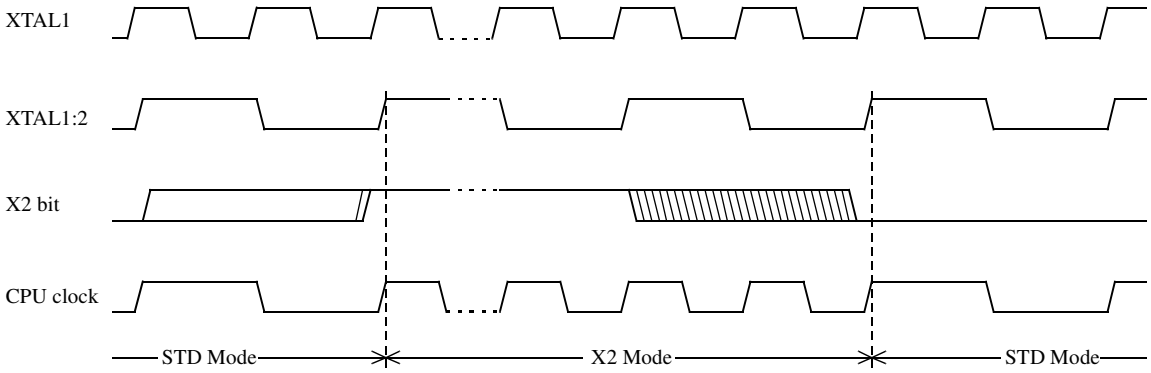


Figure 6-2. Mode Switching Waveforms



The X2 bit in the CKCON register (See Table 6-1.) allows to switch from 12 clock cycles per instruction to 6 clock cycles and vice versa. At reset, the standard speed is activated (STD mode). Setting this bit activates the X2 feature (X2 mode).

CAUTION

In order to prevent any incorrect operation while operating in X2 mode, user must be aware that all peripherals using clock frequency as time reference (UART, timers) will have their time reference divided by two. For example a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms. UART with 4800 baud rate will have 9600 baud rate.

Table 6-1. CKCON Register
CKCON - Clock Control Register (8Fh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	X2

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	X2	**CPU and peripheral clock bit** Clear to select 12 clock periods per machine cycle (STD mode, $F_{OSC}=F_{XTAL}/2$). Set to select 6 clock periods per machine cycle (X2 mode, $F_{OSC}=F_{XTAL}$).

Reset Value = XXXX XXX0b
Not bit addressable

For further details on the X2 feature, please refer to ANM072 available on the web (http://www.atmel-wm.com)

8. Application

Software can take advantage of the additional data pointers to both increase speed and reduce code size, for example, block operations (copy, compare, search ...) are well served by using one data pointer as a 'source' pointer and the other one as a "destination" pointer.

ASSEMBLY LANGUAGE

```
; Block move using dual data pointers
; Destroys DPTR0, DPTR1, A and PSW
; note: DPS exits opposite of entry state
; unless an extra INC AUXR1 is added
;
00A2                AUXR1 EQU 0A2H
;
0000 909000         MOV   DPTR,#SOURCE    ; address of SOURCE
0003 05A2           INC   AUXR1           ; switch data pointers
0005 90A000         MOV   DPTR,#DEST      ; address of DEST
0008                LOOP:
0008 05A2           INC   AUXR1           ; switch data pointers
000A E0             MOVX  A,@DPTR         ; get a byte from SOURCE
000B A3             INC   DPTR            ; increment SOURCE address
000C 05A2           INC   AUXR1           ; switch data pointers
000E F0             MOVX  @DPTR,A         ; write the byte to DEST
000F A3             INC   DPTR            ; increment DEST address
0010 70F6           JNZ   LOOP            ; check for 0 terminator
0012 05A2           INC   AUXR1           ; (optional) restore DPS
```

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.

Table 9-2. SADDR - Slave Address Register (A9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b
Not bit addressable

Table 9-3. SCON Register -- SCON - Serial Control Register (98h)

7	6	5	4	3	2	1	0
FE/SM0	**SM1**	**SM2**	**REN**	**TB8**	**RB8**	**TI**	**RI**

Bit Number	Bit Mnemonic	Description
7	FE	**Framing Error bit (SMOD0=1**) Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected. SMOD0 must be set to enable access to the FE bit
	SM0	**Serial port Mode bit 0** Refer to SM1 for serial port mode selection. SMOD0 must be cleared to enable access to the SM0 bit
6	SM1	**Serial port Mode bit 1** SM0 SM1 Mode Description Baud Rate 0 0 0 Shift Register F_{XTAL}/12 (/6 in X2 mode) 0 1 1 8-bit UART Variable 1 0 2 9-bit UART F_{XTAL}/64 or F_{XTAL}/32 (/32, /16 in X2 mode) 1 1 3 9-bit UART Variable
5	SM2	**Serial port Mode 2 bit / Multiprocessor Communication Enable bit** Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.
4	REN	**Reception Enable bit** Clear to disable serial reception. Set to enable serial reception.
3	TB8	Transmitter Bit 8 / Ninth bit to transmit in modes 2 and 3. Clear to transmit a logic 0 in the 9th bit. Set to transmit a logic 1 in the 9th bit.
2	RB8	**Receiver Bit 8 / Ninth bit received in modes 2 and 3** Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1. In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used.
1	TI	**Transmit Interrupt flag** Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.
0	RI	**Receive Interrupt flag** Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0, see Figure 9-2. and Figure 9-3. in the other modes.

Reset Value = 0000 0000b
Bit addressable

Table 9-4. PCON Register -- PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	**SMOD0**	**-**	**POF**	**GF1**	**GF0**	**PD**	**IDL**

Bit Number	Bit Mnemonic	Description
7	SMOD1	**Serial port Mode bit 1** Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	**Serial port Mode bit 0** Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	POF	**Power-Off Flag** Clear to recognize next reset type. Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	**Power-Down mode bit** Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	**Idle mode bit** Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

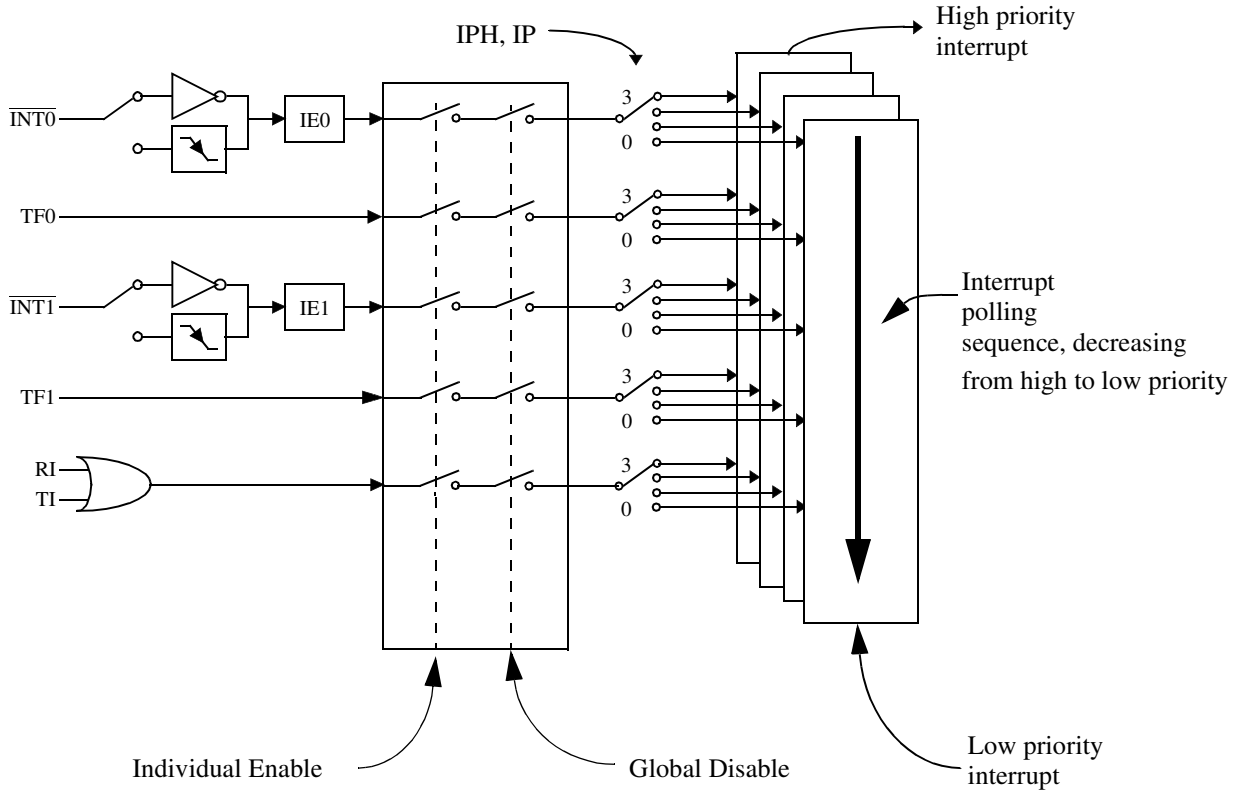
Reset Value = 00X1 0000b
Not bit addressable

Power-off flag reset value will be 1 only after a power on (cold reset). A warm reset doesn't affect the value of this bit.

10. Interrupt System

The TS80C31X2 has a total of 5 interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (timers 0 and 1) and the serial port interrupt. These interrupts are shown in Figure 10-1.

Figure 10-1. Interrupt Control System



Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 10-2.Table 10-3.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 10-3.) and in the Interrupt Priority High register (See Table 10-4.). shows the bit values and priority levels associated with each combination.

Table 10-1. Priority Level Bit Values

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

13. Power-Off Flag

The power-off flag allows the user to distinguish between a “cold start” reset and a “warm start” reset.

A cold start reset is the one induced by V_{CC} switch-on. A warm start reset occurs while V_{CC} is still applied to the device and could be generated for example by an exit from power-down.

The power-off flag (POF) is located in PCON register (See Table 13-1.). POF is set by hardware when V_{CC} rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

The POF value is only relevant with a Vcc range from 4.5V to 5.5V. For lower Vcc value, reading POF bit will return indeterminate value.

Table 13-1. PCON Register -- PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	**SMOD0**	**-**	**POF**	**GF1**	**GF0**	**PD**	**IDL**

Bit Number	Bit Mnemonic	Description
7	SMOD1	**Serial port Mode bit 1** Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	**Serial port Mode bit 0** Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	POF	**Power-Off Flag** Clear to recognize next reset type. Set by hardware when V_{CC} rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	**Power-Down mode bit** Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	**Idle mode bit** Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b
Not bit addressable

14. Electrical Characteristics

14.1 Absolute Maximum Ratings [1]

Ambiant Temperature Under Bias:
C = commercial0°C to 70°C
I = industrial -40°C to 85°C
Storage Temperature-65°C to + 150°C
Voltage on V_{CC} to V_{SS}-0.5 V to + 7 V
Voltage on V_{PP} to V_{SS}-0.5 V to + 13 V
Voltage on Any Pin to V_{SS}-0.5 V to V_{CC} + 0.5 V
Power Dissipation1 W[2]

Note:
1. Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
2. This value is based on the maximum allowable die temperature and the thermal resistance of the package.

14.2 Power consumption measurement

Since the introduction of the first C51 devices, every manufacturer made operating Icc measurements under reset, which made sense for the designs were the CPU was running under reset. In Atmel Wireless & Microcontrollers new devices, the CPU is no more active during reset, so the power consumption is very low but is not really representative of what will happen in the customer system. That's why, while keeping measurements under Reset, Atmel Wireless & Microcontrollers presents a new way to measure the operating Icc:

Using an internal test ROM, the following code is executed:

Label: SJMP Label (80 FE)

Ports 1, 2, 3 are disconnected, Port 0 is tied to FFh, EA = Vcc, RST = Vss, XTAL2 is not connected and XTAL1 is driven by the clock.

This is much more representative of the real operating Icc.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{CC} idle	Power Supply Current Maximum values, X1 mode: (7)			0.25+0.3 Freq (MHz) @12MHz 3.9 @16MHz 5.1	mA	V_{CC} = 5.5 V(2)

14.4 DC Parameters for Low Voltage

T_A = 0°C to +70°C; V_{SS} = 0 V; V_{CC} = 2.7 V to 5.5 V ± 10%; F = 0 to 30 MHz.
T_A = -40°C to +85°C; V_{SS} = 0 V; V_{CC} = 2.7 V to 5.5 V ± 10%; F = 0 to 30 MHz.

Table 14-2. DC Parameters for Low Voltage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		0.2 V_{CC} - 0.1	V	
V_{IH}	Input High Voltage except XTAL1, RST	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage, XTAL1, RST	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage, ports 1, 2, 3 (6)			0.45	V	I_{OL} = 0.8 mA(4)
V_{OL1}	Output Low Voltage, port 0, ALE, $\overline{PSEN}$ (6)			0.45	V	I_{OL} = 1.6 mA(4)
V_{OH}	Output High Voltage, ports 1, 2, 3	0.9 V_{CC}			V	I_{OH} = -10 µA
V_{OH1}	Output High Voltage, port 0, ALE, $\overline{PSEN}$	0.9 V_{CC}			V	I_{OH} = -40 µA
I_{IL}	Logical 0 Input Current ports 1, 2 and 3			-50	µA	Vin = 0.45 V
I_{LI}	Input Leakage Current			±10	µA	0.45 V < Vin < V_{CC}
I_{TL}	Logical 1 to 0 Transition Current, ports 1, 2, 3			-650	µA	Vin = 2.0 V
R_{RST}	RST Pulldown Resistor	50	90 (5)	200	kΩ	
CIO	Capacitance of I/O Buffer			10	pF	Fc = 1 MHz T_A = 25°C
I_{PD}	Power Down Current		20 (5) 10 (5)	50 30	µA	V_{CC} = 2.0 V to 5.5 V(3) V_{CC} = 2.0 V to 3.3 V(3)
I_{CC} under RESET	Power Supply Current Maximum values, X1 mode: (7)			1 + 0.2 Freq (MHz) @12MHz 3.4 @16MHz 4.2	mA	V_{CC} = 3.3 V(1)
I_{CC} operating	Power Supply Current Maximum values, X1 mode: (7)			1 + 0.3 Freq (MHz) @12MHz 4.6 @16MHz 5.8	mA	V_{CC} = 3.3 V(8)
I_{CC} idle	Power Supply Current Maximum values, X1 mode: (7)			0.15 Freq (MHz) + 0.2 @12MHz 2 @16MHz 2.6	mA	V_{CC} = 3.3 V(2)

Note: 1. I_{CC} under reset is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, T_{CHCL} = 5 ns (see Figure 14-5.), V_{IL} = V_{SS} + 0.5 V,

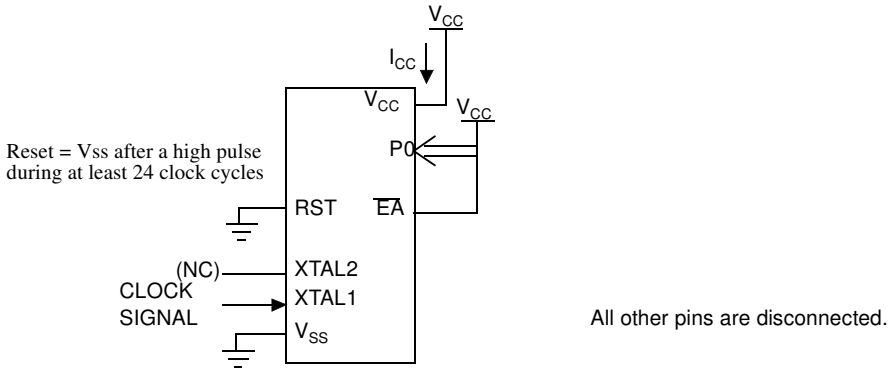


Figure 14-2. Operating I_{CC} Test Condition

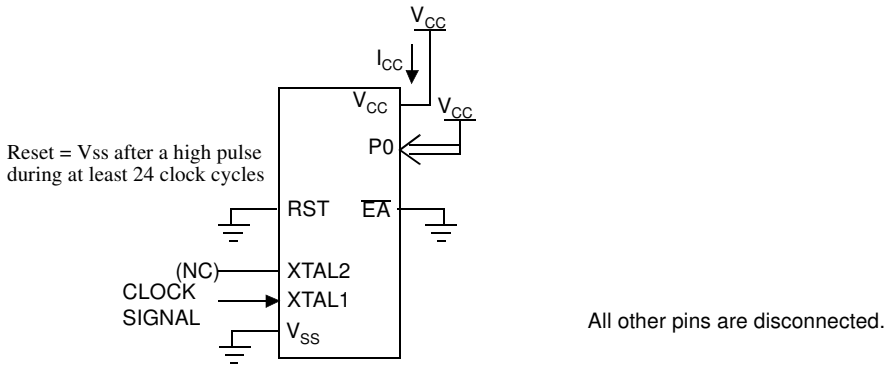


Figure 14-3. I_{CC} Test Condition, Idle Mode

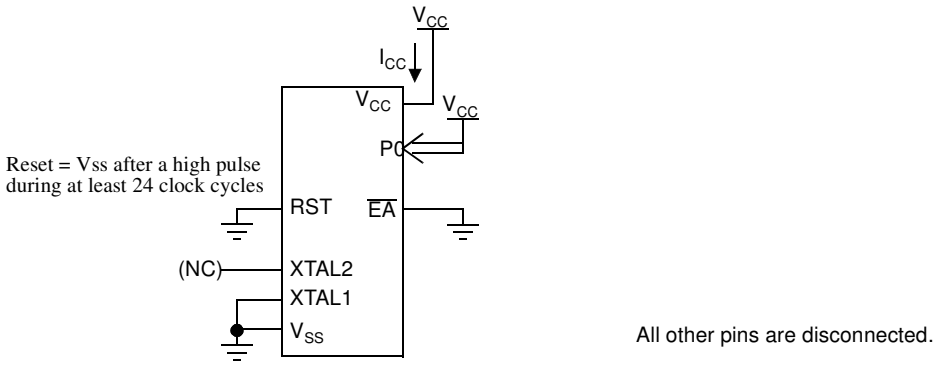


Figure 14-4. I_{CC} Test Condition, Power-Down Mode

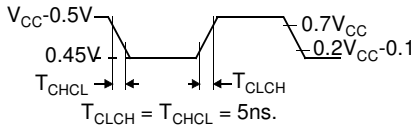


Figure 14-5. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes

14.5 AC Parameters

14.5.1 Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a “T” (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example:T_{AVLL} = Time for Address Valid to ALE Low.
T_{LLPL} = Time for ALE Low to $\overline{PSEN}$ Low.

T_A = 0 to +70°C (commercial temperature range); V_{SS} = 0 V; V_{CC} = 5 V ± 10%; -M and -V ranges.
T_A = -40°C to +85°C (industrial temperature range); V_{SS} = 0 V; V_{CC} = 5 V ± 10%; -M and -V ranges.
T_A = 0 to +70°C (commercial temperature range); V_{SS} = 0 V; 2.7 V < V_{CC} < 5.5 V; -L range.
T_A = -40°C to +85°C (industrial temperature range); V_{SS} = 0 V; 2.7 V < V_{CC} < 5.5 V; -L range.

Table 14-3. gives the maximum applicable load capacitance for Port 0, Port 1, 2 and 3, and ALE and $\overline{PSEN}$ signals. Timings will be guaranteed if these capacitances are respected. Higher capacitance values can be used, but timings will then be degraded.

Table 14-3. Load Capacitance versus speed range, in pF

	-M	-V	-L
Port 0	100	50	100
Port 1, 2, 3	80	50	80
ALE / $\overline{PSEN}$	100	30	100

Table 8-5., Table 8-8. and Table 8-11. give the description of each AC symbols.

Table 14-6., Table 14-9. and Table 14-12. give for each range the AC parameter.

Table 14-7., Table 14-10. and Table 14-13. give the frequency derating formula of the AC parameter. To calculate each AC symbols, take the x value corresponding to the speed grade you need (-M, -V or -L) and replace this value in the formula. Values of the frequency must be limited to the corresponding speed grade:

Table 14-4. Max frequency for derating formula regarding the speed grade

	-M X1 mode	-M X2 mode	-V X1 mode	-V X2 mode	-L X1 mode	-L X2 mode
Freq (MHz)	40	20	40	30	30	20
T (ns)	25	50	25	33.3	33.3	50

Example:

T_{LLIV} in X2 mode for a -V part at 20 MHz ($T = 1/20^{E6} = 50$ ns):

x= 25 (Table 14-7.)

T= 50ns

T_{LLIV}= 2T - x = 2 x 50 - 25 = 75ns

Table 14-5. External Program Memory Characteristics

Symbol	Parameter
T	Oscillator clock period
T_{LHLL}	ALE pulse width
T_{AVLL}	Address Valid to ALE
T_{LLAX}	Address Hold After ALE
T_{LLIV}	ALE to Valid Instruction In
T_{LLPL}	ALE to $\overline{PSEN}$
T_{PLPH}	$\overline{PSEN}$ Pulse Width
T_{PLIV}	$\overline{PSEN}$ to Valid Instruction In
T_{PXIX}	Input Instruction Hold After $\overline{PSEN}$
T_{PXIZ}	Input Instruction FloatAfter $\overline{PSEN}$
T_{PXAV}	$\overline{PSEN}$ to Address Valid
T_{AVIV}	Address to Valid Instruction In
T_{PLAZ}	$\overline{PSEN}$ Low to Address Float

14.5.2 External Program Memory Read Cycle

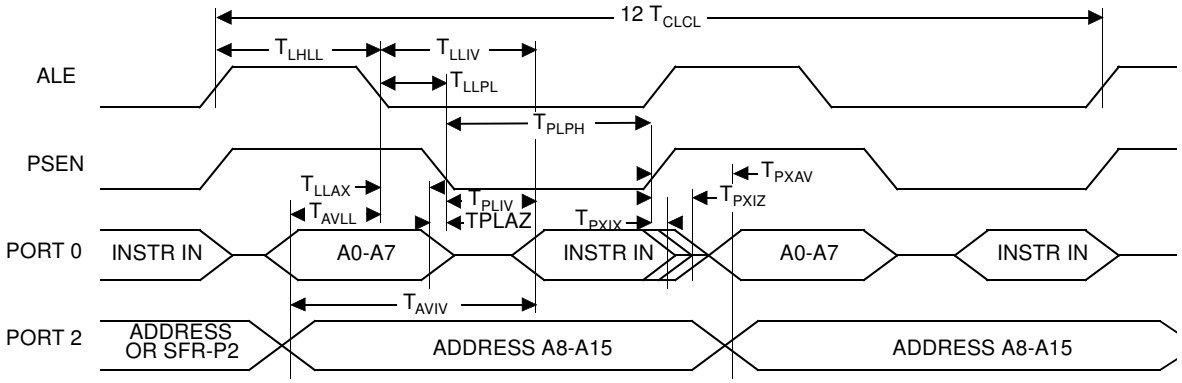


Figure 14-6. External Program Memory Read Cycle

Table 14-8. External Data Memory Characteristics

Symbol	Parameter
T_{RLRH}	$\overline{RD}$ Pulse Width
T_{WLWH}	$\overline{WR}$ Pulse Width
T_{RLDV}	$\overline{RD}$ to Valid Data In
T_{RHDX}	Data Hold After $\overline{RD}$
T_{RHDZ}	Data Float After $\overline{RD}$
T_{LLDV}	ALE to Valid Data In
T_{AVDV}	Address to Valid Data In
T_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$
T_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$
T_{QVWX}	Data Valid to $\overline{WR}$ Transition
T_{QVWH}	Data set-up to $\overline{WR}$ High
T_{WHQX}	Data Hold After $\overline{WR}$
T_{RLAZ}	$\overline{RD}$ Low to Address Float
T_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE high

14.5.6 External Clock Drive Waveforms

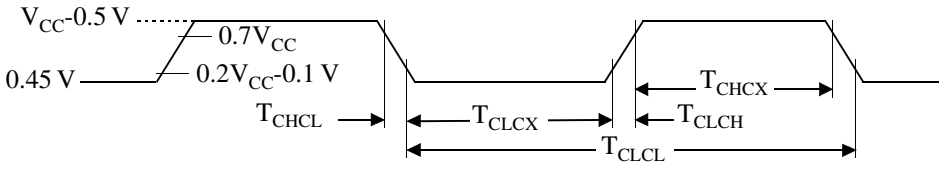


Figure 14-10. External Clock Drive Waveforms

14.5.7 AC Testing Input/Output Waveforms

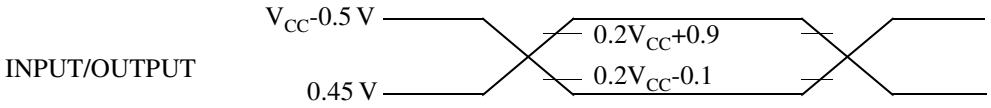


Figure 14-11. AC Testing Input/Output Waveforms

AC inputs during testing are driven at V_{CC} - 0.5 for a logic “1” and 0.45V for a logic “0”. Timing measurement are made at V_{IH} min for a logic “1” and V_{IL} max for a logic “0”.

14.5.8 Float Waveforms

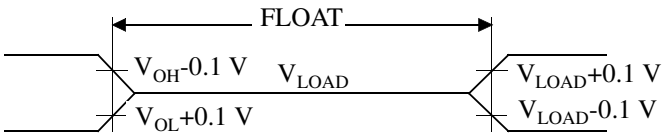


Figure 14-12. Float Waveforms

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm$ 20mA.

14.5.9 Clock Waveforms

Valid in normal clock mode. In X2 mode XTAL2 signal must be changed to XTAL2 divided by two.

15. Ordering Information

Part Number[3]	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
TS80C31X2-MCA	OBSOLETE					
TS80C31X2-MCB						
TS80C31X2-MCC						
TS80C31X2-MCE						
TS80C31X2-LCA						
TS80C31X2-LCB						
TS80C31X2-LCC						
TS80C31X2-LCE						
TS80C31X2-VCA						
TS80C31X2-VCB						
TS80C31X2-VCC						
TS80C31X2-VCE						
TS80C31X2-MIA						
TS80C31X2-MIB						
TS80C31X2-MIC						
TS80C31X2-MIE						
TS80C31X2-LIA						
TS80C31X2-LIB						
TS80C31X2-LIC						
TS80C31X2-LIE						
TS80C31X2-VIA						
TS80C31X2-VIB						
TS80C31X2-VIC						
TS80C31X2-VIE						
AT80C31X2-3CSUM	ROMLess	5V ±10%	Industrial & Green	40 MHz[1]	PDIL40	Stick
AT80C31X2-SLSUM	ROMLess	5V ±10%	Industrial & Green	40 MHz[1]	PLCC44	Stick
AT80C31X2-RLTUM	ROMLess	5V ±10%	Industrial & Green	40 MHz[1]	VQFP44	Tray
AT80C31X2-3CSUL	ROMLess	2.7 to 5.5V	Industrial & Green	30 MHz[1]	PDIL40	Stick
AT80C31X2-SLSUL	ROMLess	2.7 to 5.5V	Industrial & Green	30 MHz[1]	PLCC44	Stick
AT80C31X2-RLTUL	ROMLess	2.7 to 5.5V	Industrial & Green	30 MHz[1]	VQFP44	Tray

Part Number[3]	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
AT80C31X2-3CSUV	ROMLess	5V ±10%	Industrial & Green	60 MHz[3]	PDIL40	Stick
AT80C31X2-SLSUV	ROMLess	5V ±10%	Industrial & Green	60 MHz[3]	PLCC44	Stick
AT80C31X2-RLTUV	ROMLess	5V ±10%	Industrial & Green	60 MHz[3]	VQFP44	Tray

Notes: 1. 20 MHz in X2 Mode.
2. Tape and Reel available for SL, PQFP and RL packages.
3. 30 MHz in X2 Mode.