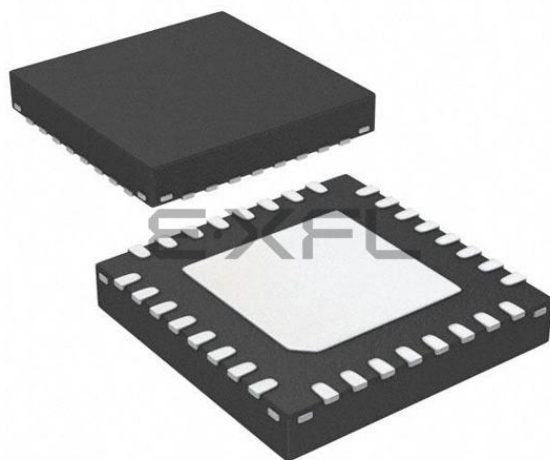




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	28
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VQFN Exposed Pad
Supplier Device Package	32-HVQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1111fhn33-201-5

Table 1. Ordering information ...continued

Type number	Package		
	Name	Description	Version
LPC1114FHI33/302	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC1114FHI33/303	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC1114JHI33/303	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC1114FHN33/203	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1114JHN33/203	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1114FHN33/303	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1114JHN33/303	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1114FHN33/333	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1114JHN33/333	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1113FBD48/301	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1113FBD48/302	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1113FBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1113JBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114FBD48/301	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114FBD48/302	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114FBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114JBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114FBD48/323	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114JBD48/323	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114FBD48/333	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114JBD48/333	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1115FBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

Table 2. Ordering options ...continued

Type number	Series	Flash	Total SRAM	Power profiles	UART	I ² C/ Fast+	SPI	ADC channel	GPIO	Package	Temp ^[1]
LPC1113											
LPC1113FHN33/201	LPC1100	24 kB	4 kB	no	1	1	1	8	28	HVQFN33	F
LPC1113FHN33/202	LPC1100L	24 kB	4 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1113FHN33/203	LPC1100XL	24 kB	4 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1113JHN33/203	LPC1100XL	24 kB	4 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1113FHN33/301	LPC1100	24 kB	8 kB	no	1	1	1	8	28	HVQFN33	F
LPC1113FHN33/302	LPC1100L	24 kB	8 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1113FHN33/303	LPC1100XL	24 kB	8 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1113JHN33/303	LPC1100XL	24 kB	8 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1113FBD48/301	LPC1100	24 kB	8 kB	no	1	1	2	8	42	LQFP48	F
LPC1113FBD48/302	LPC1100L	24 kB	8 kB	yes	1	1	2	8	42	LQFP48	F
LPC1113FBD48/303	LPC1100XL	24 kB	8 kB	yes	1	1	2	8	42	LQFP48	F
LPC1113JBD48/303	LPC1100XL	24 kB	8 kB	yes	1	1	2	8	42	LQFP48	J
LPC1114											
LPC1114FDH28/102	LPC1100L	32 kB	4 kB	yes	1	1	1	6	22	TSSOP28	F
LPC1114FN28/102	LPC1100L	32 kB	4 kB	yes	1	1	1	6	22	DIP28	F
LPC1114FHN33/201	LPC1100	32 kB	4 kB	no	1	1	1	8	28	HVQFN33	F
LPC1114FHN33/202	LPC1100L	32 kB	4 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1114FHN33/203	LPC1100XL	32 kB	4 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1114JHN33/203	LPC1100XL	32 kB	4 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1114FHN33/301	LPC1100	32 kB	8 kB	no	1	1	1	8	28	HVQFN33	F
LPC1114FHN33/302	LPC1100L	32 kB	8 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1114FHN33/303	LPC1100XL	32 kB	8 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1114JHN33/303	LPC1100XL	32 kB	8 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1114FHN33/333	LPC1100XL	56 kB	8 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1114JHN33/333	LPC1100XL	56 kB	8 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1114FHI33/302	LPC1100L	32 kB	8 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1114FHI33/303	LPC1100XL	32 kB	8 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1114JHI33/303	LPC1100XL	32 kB	8 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1114FBD48/301	LPC1100	32 kB	8 kB	no	1	1	2	8	42	LQFP48	F
LPC1114FBD48/302	LPC1100L	32 kB	8 kB	yes	1	1	2	8	42	LQFP48	F
LPC1114FBD48/303	LPC1100XL	32 kB	8 kB	yes	1	1	2	8	42	LQFP48	F
LPC1114JBD48/303	LPC1100XL	32 kB	8 kB	yes	1	1	2	8	42	LQFP48	J
LPC1114FBD48/323	LPC1100XL	48 kB	8 kB	yes	1	1	2	8	42	LQFP48	F
LPC1114JBD48/323	LPC1100XL	48 kB	8 kB	yes	1	1	2	8	42	LQFP48	J
LPC1114FBD48/333	LPC1100XL	56 kB	8 kB	yes	1	1	2	8	42	LQFP48	F
LPC1114JBD48/333	LPC1100XL	56 kB	8 kB	yes	1	1	2	8	42	LQFP48	J
LPC1115											
LPC1115FBD48/303	LPC1100XL	64 kB	8 kB	yes	1	1	2	8	42	LQFP48	F

6. Pinning information

6.1 Pinning

Table 3. Pin description overview

Part	Pin description table	Pinning diagram
LPC1110FD20	Table 4	Figure 8
LPC1111FDH20/002	Table 4	Figure 9
LPC1112FD20/102	Table 4	Figure 10
LPC1112FDH20/102	Table 5	Figure 9
LPC1112FHN24/202	Table 6	Figure 11
LPC1112FDH28/102	Table 7	Figure 12
LPC1114FDH28/102	Table 7	Figure 13
LPC1114FN28/102	Table 7	Figure 13
LPC1111FHN33/101	Table 9	Figure 6
LPC1111FHN33/102	Table 9	Figure 6
LPC1111JHN33/103	Table 11	Figure 7
LPC1111FHN33/103	Table 11	Figure 7
LPC1111FHN33/201	Table 9	Figure 6
LPC1111FHN33/202	Table 9	Figure 6
LPC1111FHN33/203	Table 11	Figure 7
LPC1111JHN33/203	Table 11	Figure 7
LPC1112FHN33/101	Table 9	Figure 6
LPC1112FHN33/102	Table 9	Figure 6
LPC1112FHN33/103	Table 11	Figure 7
LPC1112JHN33/103	Table 11	Figure 7
LPC1112FHN33/201	Table 9	Figure 6
LPC1112FHN33/202	Table 9	Figure 6
LPC1112FHN33/203	Table 11	Figure 7
LPC1112JHN33/203	Table 11	Figure 7
LPC1112FHI33/202	Table 9	Figure 6
LPC1112FHI33/203	Table 11	Figure 7
LPC1112JHI33/203	Table 11	Figure 7
LPC1113FHN33/201	Table 9	Figure 6
LPC1113FHN33/202	Table 9	Figure 6
LPC1113FHN33/203	Table 11	Figure 7
LPC1113JHN33/203	Table 11	Figure 7
LPC1113FHN33/301	Table 9	Figure 6
LPC1113FHN33/302	Table 9	Figure 6
LPC1113FHN33/303	Table 11	Figure 7
LPC1113JHN33/303	Table 11	Figure 7
LPC1114FHN33/201	Table 9	Figure 6
LPC1114FHN33/202	Table 9	Figure 6

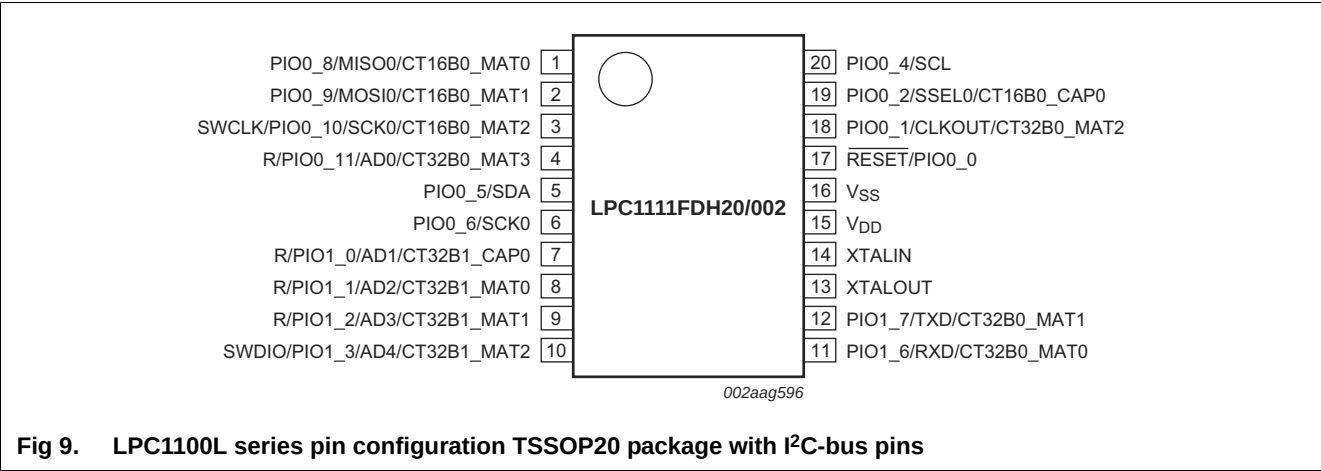


Fig 9. LPC1100L series pin configuration TSSOP20 package with I²C-bus pins

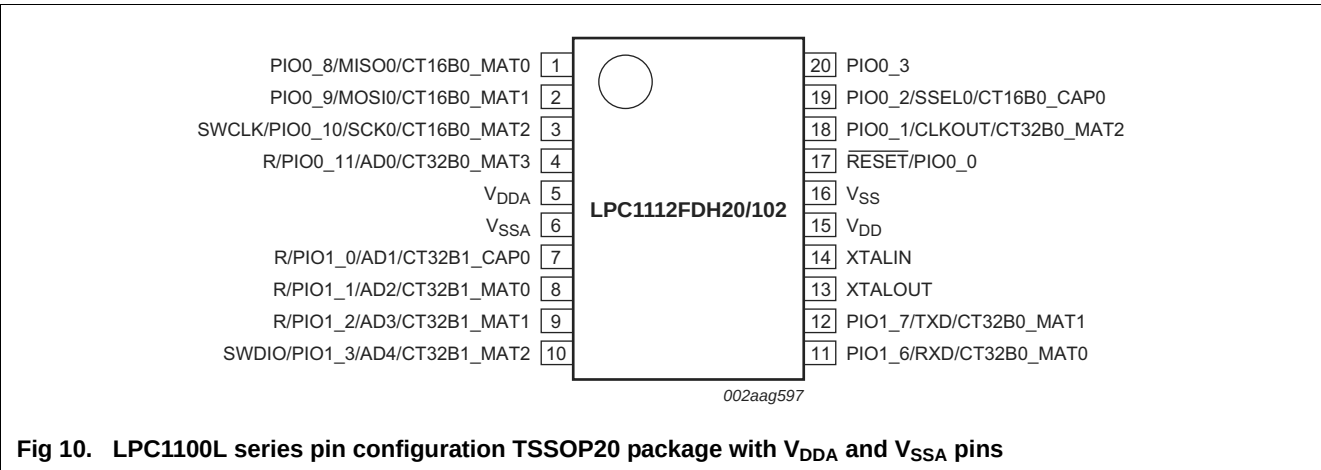


Fig 10. LPC1100L series pin configuration TSSOP20 package with V_{DDA} and V_{SSA} pins

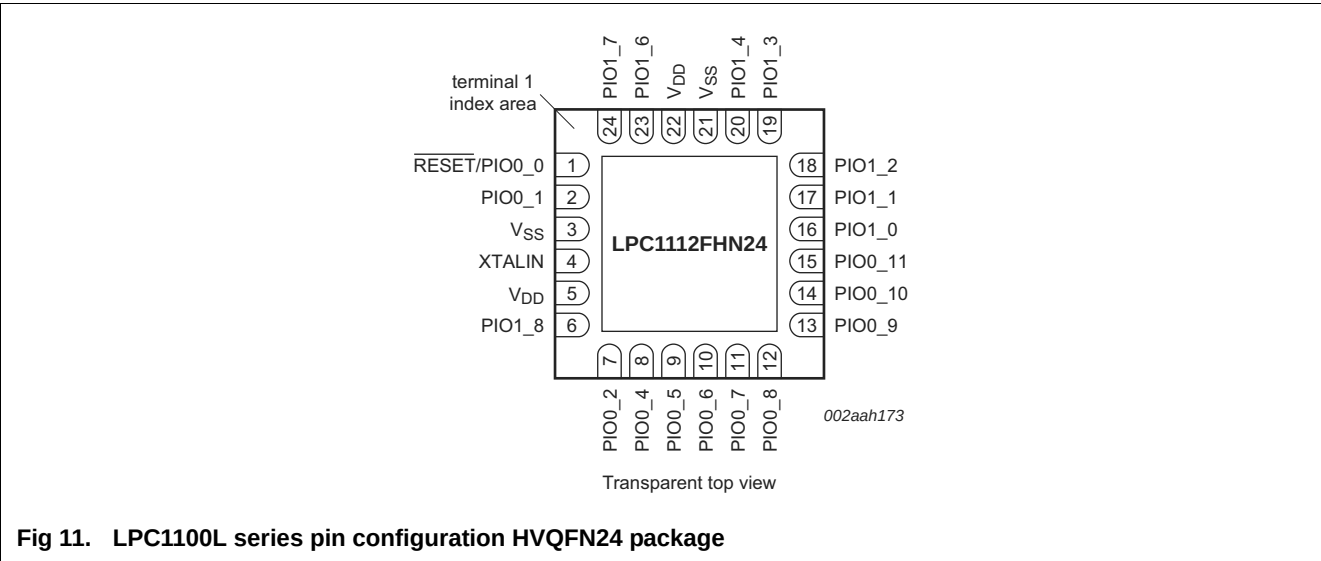


Fig 11. LPC1100L series pin configuration HVQFN24 package

- [1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level); IA = inactive, no pull-up/down enabled.
- [2] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode.
- [3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see [Figure 51](#)).
- [4] I²C-bus pin compliant with the I²C-bus specification for I²C standard mode and I²C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I²C lines. Open-drain configuration applies to all functions on this pin.
- [5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see [Figure 51](#)).
- [6] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

Table 5. LPC1100L series: LPC1112 pin description table (TSSOP20 with V_{DDA} and V_{SSA} pins)

Symbol	Pin TSSOP20	Start logic input	Type	Reset state [1]	Description
PIO0_0 to PIO0_11			I/O		Port 0 — Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.
$\overline{\text{RESET}}$ /PIO0_0	17 [2]	yes	I	I; PU	RESET — External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO pin if an external $\overline{\text{RESET}}$ function is not needed and Deep power-down mode is not used.
			I/O	-	PIO0_0 — General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/ CT32B0_MAT2	18 [3]	yes	I/O	I; PU	PIO0_1 — General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
			O	-	CLKOUT — Clockout pin.
			O	-	CT32B0_MAT2 — Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	19 [3]	yes	I/O	I; PU	PIO0_2 — General purpose digital input/output pin.
			I/O	-	SSEL0 — Slave Select for SPI0.
			I	-	CT16B0_CAP0 — Capture input 0 for 16-bit timer 0.
PIO0_3	20 [3]	yes	I/O	I; PU	PIO0_3 — General purpose digital input/output pin.
PIO0_8/MISO0/ CT16B0_MAT0	1 [3]	yes	I/O	I; PU	PIO0_8 — General purpose digital input/output pin.
			I/O	-	MISO0 — Master In Slave Out for SPI0.
			O	-	CT16B0_MAT0 — Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	2 [3]	yes	I/O	I; PU	PIO0_9 — General purpose digital input/output pin.
			I/O	-	MOSI0 — Master Out Slave In for SPI0.
			O	-	CT16B0_MAT1 — Match output 1 for 16-bit timer 0.

Table 7. LPC1100L series: LPC1112/14 pin description table (TSSOP28 and DIP28 packages)

Symbol	Pin TSSOP28/ DIP28	Start logic input	Type	Reset state ^[1]	Description
PIO0_0 to PIO0_11			I/O		Port 0 — Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.
RESET/PIO0_0	23 ^[2]	yes	I	I; PU	RESET — External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The RESET pin can be left unconnected or be used as a GPIO pin if an external RESET function is not needed and Deep power-down mode is not used.
			I/O	-	PIO0_0 — General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/ CT32B0_MAT2	24 ^[3]	yes	I/O	I; PU	PIO0_1 — General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
			O	-	CLKOUT — Clockout pin.
			O	-	CT32B0_MAT2 — Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	25 ^[3]	yes	I/O	I; PU	PIO0_2 — General purpose digital input/output pin.
			I/O	-	SSEL0 — Slave Select for SPI0.
			I	-	CT16B0_CAP0 — Capture input 0 for 16-bit timer 0.
PIO0_3	26 ^[3]	yes	I/O	I; PU	PIO0_3 — General purpose digital input/output pin.
PIO0_4/SCL	27 ^[4]	yes	I/O	I; IA	PIO0_4 — General purpose digital input/output pin (open-drain).
			I/O	-	SCL — I ² C-bus, open-drain clock input/output. High-current sink only if I ² C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	5 ^[4]	yes	I/O	I; IA	PIO0_5 — General purpose digital input/output pin (open-drain).
			I/O	-	SDA — I ² C-bus, open-drain data input/output. High-current sink only if I ² C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	6 ^[3]	yes	I/O	I; PU	PIO0_6 — General purpose digital input/output pin.
			I/O	-	SCK0 — Serial clock for SPI0.
PIO0_7/CTS	28 ^[3]	yes	I/O	I; PU	PIO0_7 — General purpose digital input/output pin (high-current output driver).
			I	-	CTS — Clear To Send input for UART.
PIO0_8/MISO0/ CT16B0_MAT0	1 ^[3]	yes	I/O	I; PU	PIO0_8 — General purpose digital input/output pin.
			I/O	-	MISO0 — Master In Slave Out for SPI0.
			O	-	CT16B0_MAT0 — Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	2 ^[3]	yes	I/O	I; PU	PIO0_9 — General purpose digital input/output pin.
			I/O	-	MOSI0 — Master Out Slave In for SPI0.
			O	-	CT16B0_MAT1 — Match output 1 for 16-bit timer 0.

Table 8. LPC1100 and LPC1100L series: LPC1113/14 pin description table (LQFP48 package) ...continued

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2	29 ^[3]	yes	I	I; PU	SWCLK — Serial wire clock.
			I/O	-	PIO0_10 — General purpose digital input/output pin.
			I/O	-	SCK0 — Serial clock for SPI0.
			O	-	CT16B0_MAT2 — Match output 2 for 16-bit timer 0.
R/PIO0_11/ AD0/CT32B0_MAT3	32 ^[5]	yes	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO0_11 — General purpose digital input/output pin.
			I	-	AD0 — A/D converter, input 0.
			O	-	CT32B0_MAT3 — Match output 3 for 32-bit timer 0.
PIO1_0 to PIO1_11			I/O		Port 1 — Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block.
R/PIO1_0/ AD1/CT32B1_CAP0	33 ^[5]	yes	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_0 — General purpose digital input/output pin.
			I	-	AD1 — A/D converter, input 1.
			I	-	CT32B1_CAP0 — Capture input 0 for 32-bit timer 1.
R/PIO1_1/ AD2/CT32B1_MAT0	34 ^[5]	no	O	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_1 — General purpose digital input/output pin.
			I	-	AD2 — A/D converter, input 2.
			O	-	CT32B1_MAT0 — Match output 0 for 32-bit timer 1.
R/PIO1_2/ AD3/CT32B1_MAT1	35 ^[5]	no	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_2 — General purpose digital input/output pin.
			I	-	AD3 — A/D converter, input 3.
			O	-	CT32B1_MAT1 — Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ AD4/CT32B1_MAT2	39 ^[5]	no	I/O	I; PU	SWDIO — Serial wire debug input/output.
			I/O	-	PIO1_3 — General purpose digital input/output pin.
			I	-	AD4 — A/D converter, input 4.
			O	-	CT32B1_MAT2 — Match output 2 for 32-bit timer 1.
PIO1_4/AD5/ CT32B1_MAT3/ WAKEUP	40 ^[5]	no	I/O	I; PU	PIO1_4 — General purpose digital input/output pin with 10 ns glitch filter. In Deep power-down mode, this pin serves as the Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
			I	-	AD5 — A/D converter, input 5.
			O	-	CT32B1_MAT3 — Match output 3 for 32-bit timer 1.
PIO1_5/RTS/ CT32B0_CAP0	45 ^[3]	no	I/O	I; PU	PIO1_5 — General purpose digital input/output pin.
			O	-	RTS — Request To Send output for UART.
			I	-	CT32B0_CAP0 — Capture input 0 for 32-bit timer 0.

Table 11. LPC1100XL series: LPC1111/12/13/14 pin description table (HVQFN33 package) ...continued

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
R/PIO0_11/AD0/ CT32B0_MAT3	21 ^[5]	yes	-	I;PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO0_11 — General purpose digital input/output pin.
			I	-	AD0 — A/D converter, input 0.
			O	-	CT32B0_MAT3 — Match output 3 for 32-bit timer 0.
PIO1_0 to PIO1_11					Port 1 — Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block.
R/PIO1_0/AD1/ CT32B1_CAP0	22 ^[5]	yes	-	I;PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_0 — General purpose digital input/output pin.
			I	-	AD1 — A/D converter, input 1.
			I	-	CT32B1_CAP0 — Capture input 0 for 32-bit timer 1.
R/PIO1_1/AD2/ CT32B1_MAT0	23 ^[5]	no	-	I;PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_1 — General purpose digital input/output pin.
			I	-	AD2 — A/D converter, input 2.
			O	-	CT32B1_MAT0 — Match output 0 for 32-bit timer 1.
R/PIO1_2/AD3/ CT32B1_MAT1	24 ^[5]	no	-	I;PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_2 — General purpose digital input/output pin.
			I	-	AD3 — A/D converter, input 3.
			O	-	CT32B1_MAT1 — Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ AD4/CT32B1_MAT2	25 ^[5]	no	I/O	I;PU	SWDIO — Serial wire debug input/output.
			I/O	-	PIO1_3 — General purpose digital input/output pin.
			I	-	AD4 — A/D converter, input 4.
			O	-	CT32B1_MAT2 — Match output 2 for 32-bit timer 1.
PIO1_4/AD5/ CT32B1_MAT3/ WAKEUP	26 ^[5]	no	I/O	I;PU	PIO1_4 — General purpose digital input/output pin with 10 ns glitch filter. In Deep power-down mode, this pin serves as the Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
			I	-	AD5 — A/D converter, input 5.
			O	-	CT32B1_MAT3 — Match output 3 for 32-bit timer 1.
PIO1_5/RTS/ CT32B0_CAP0	30 ^[3]	no	I/O	I;PU	PIO1_5 — General purpose digital input/output pin.
			O	-	RTS — Request To Send output for UART.
			I	-	CT32B0_CAP0 — Capture input 0 for 32-bit timer 0.
PIO1_6/RXD/ CT32B0_MAT0	31 ^[3]	no	I/O	I;PU	PIO1_6 — General purpose digital input/output pin.
			I	-	RXD — Receiver input for UART.
			O	-	CT32B0_MAT0 — Match output 0 for 32-bit timer 0.

Table 11. LPC1100XL series: LPC1111/12/13/14 pin description table (HVQFN33 package) ...continued

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
V _{DD}	6; 29	-	I	-	3.3 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	4[6]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	5[6]	-	O	-	Output from the oscillator amplifier.
V _{SS}	33	-	-	-	Thermal pad. Connect to ground.

- [1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level (V_{DD} = 3.3 V)); IA = inactive, no pull-up/down enabled.
- [2] 5 V tolerant pad. **RESET** functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See [Figure 52](#) for the reset pad configuration.
- [3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see [Figure 51](#)).
- [4] I²C-bus pads compliant with the I²C-bus specification for I²C standard mode and I²C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.
- [5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled, and the pin is not 5 V tolerant (see [Figure 51](#)).
- [6] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

10.3 ADC static characteristics

Table 18. ADC static characteristics

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$ unless otherwise specified; ADC frequency 4.5 MHz, $V_{DD} = 2.5\text{ V}$ to 3.6 V .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		0	-	V_{DD}	V
C_{ia}	analog input capacitance		-	-	1	pF
E_D	differential linearity error	[1][2]	-	-	± 1	LSB
$E_{L(adj)}$	integral non-linearity	[3]	-	-	± 1.5	LSB
E_O	offset error	[4]	-	-	± 3.5	LSB
E_G	gain error	[5]	-	-	0.6	%
E_T	absolute error	[6]	-	-	± 4	LSB
R_{vsi}	voltage source interface resistance		-	-	40	k Ω
R_i	input resistance	[7][8]	-	-	2.5	M Ω

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See [Figure 17](#).

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See [Figure 17](#).

[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See [Figure 17](#).

[5] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See [Figure 17](#).

[6] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See [Figure 17](#).

[7] $T_{amb} = 25\text{ }^{\circ}\text{C}$; maximum sampling frequency $f_s = 400\text{ kSamples/s}$ and analog input capacitance $C_{ia} = 1\text{ pF}$.

[8] Input resistance R_i depends on the sampling frequency f_s : $R_i = 1 / (f_s \times C_{ia})$.

10.4 BOD static characteristics

Table 19. BOD static characteristics^[1]

$T_{amb} = 25\text{ }^{\circ}\text{C}$.

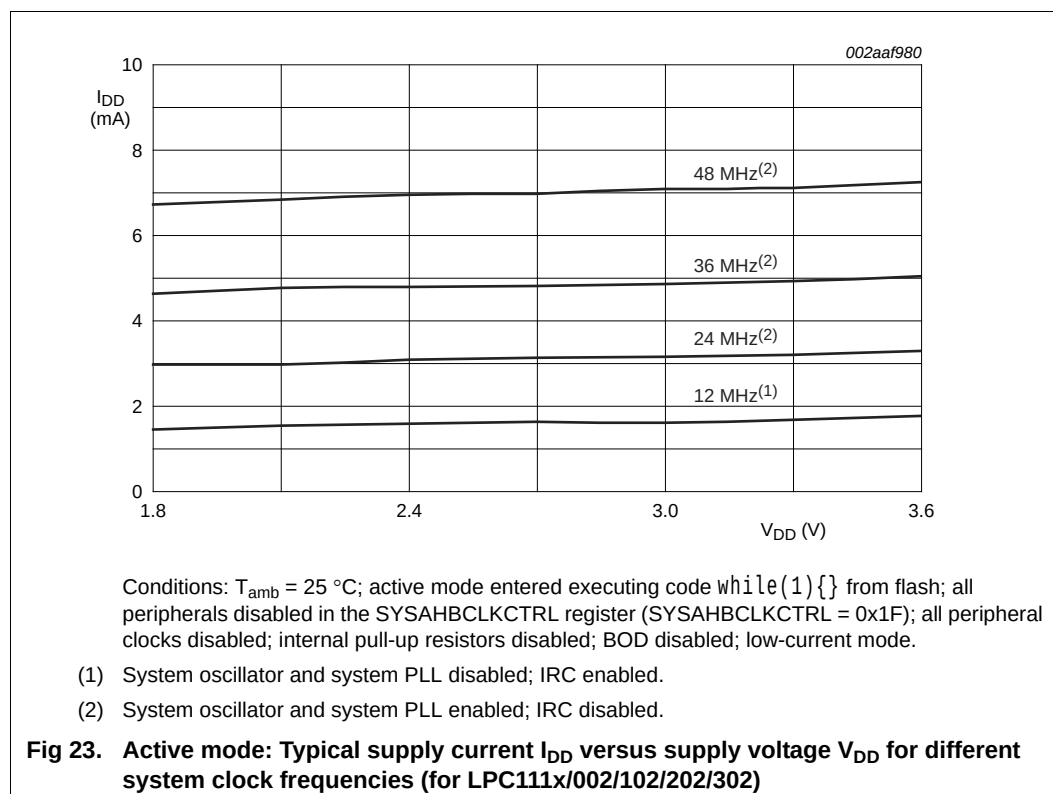
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 1				
		assertion	-	2.22	-	V
		de-assertion	-	2.35	-	V
		interrupt level 2				
		assertion	-	2.52	-	V
		de-assertion	-	2.66	-	V
		interrupt level 3				
		assertion	-	2.80	-	V
		de-assertion	-	2.90	-	V
		reset level 0				
		assertion	-	1.46	-	V
		de-assertion	-	1.63	-	V
		reset level 1				
		assertion	-	2.06	-	V
		de-assertion	-	2.15	-	V
		reset level 2				
		assertion	-	2.35	-	V
		de-assertion	-	2.43	-	V
		reset level 3				
		assertion	-	2.63	-	V
		de-assertion	-	2.71	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *LPC111x user manual*.

10.6 Power consumption LPC1100L series (LPC111x/002/102/202/302)

Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see *LPC111x user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCONFIG block.
- Configure GPIO pins as outputs using the GPIODIR registers.
- Write 0 to all GPIODATA registers to drive the outputs LOW.



10.7 Power consumption LPC1100XL series (LPC111x/103/203/303/323/333)

Table 20. Power consumption at very low frequencies using the watchdog oscillator

Symbol	Parameter	Conditions ^[1]	Min	Typ ^[2]	Max	Unit
I _{DD}	supply current	Active mode; code while(1){} executed from flash				
		system clock = 8.8 kHz	-	275	-	μA
		system clock = 257 kHz	-	305	-	μA
		system clock = 515 kHz	-	335	-	μA
		system clock = 784 kHz	-	368	-	μA
		system clock = 1028 kHz	-	396	-	μA
		system clock = 2230 kHz	-	538	-	μA
		Sleep mode;				
		system clock = 8.8 kHz	-	274	-	μA
		system clock = 257 kHz	-	285	-	μA
		system clock = 515 kHz	-	295	-	μA
		system clock = 784 kHz	-	309	-	μA
		system clock = 1028 kHz	-	317	-	μA
		system clock = 2230 kHz	-	368	-	μA

[1] WDT OSC enabled, V_{DD} = 3.3 V, Temp = 25 °C.

Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.

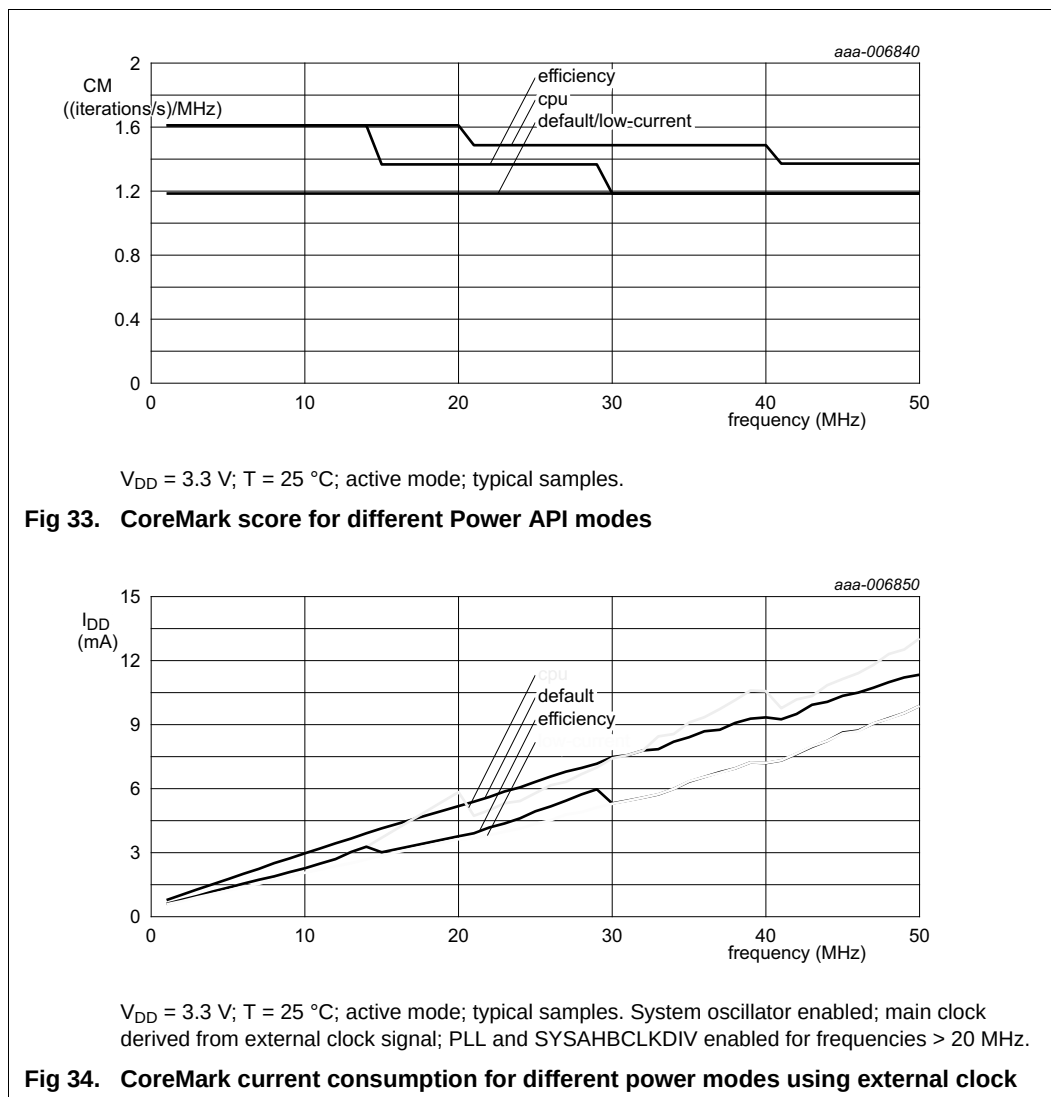
I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled, IRC disabled, System Oscillator disabled, System PLL disabled, BOD disabled.

All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks to UART and SPI0/1 disabled in system configuration block.

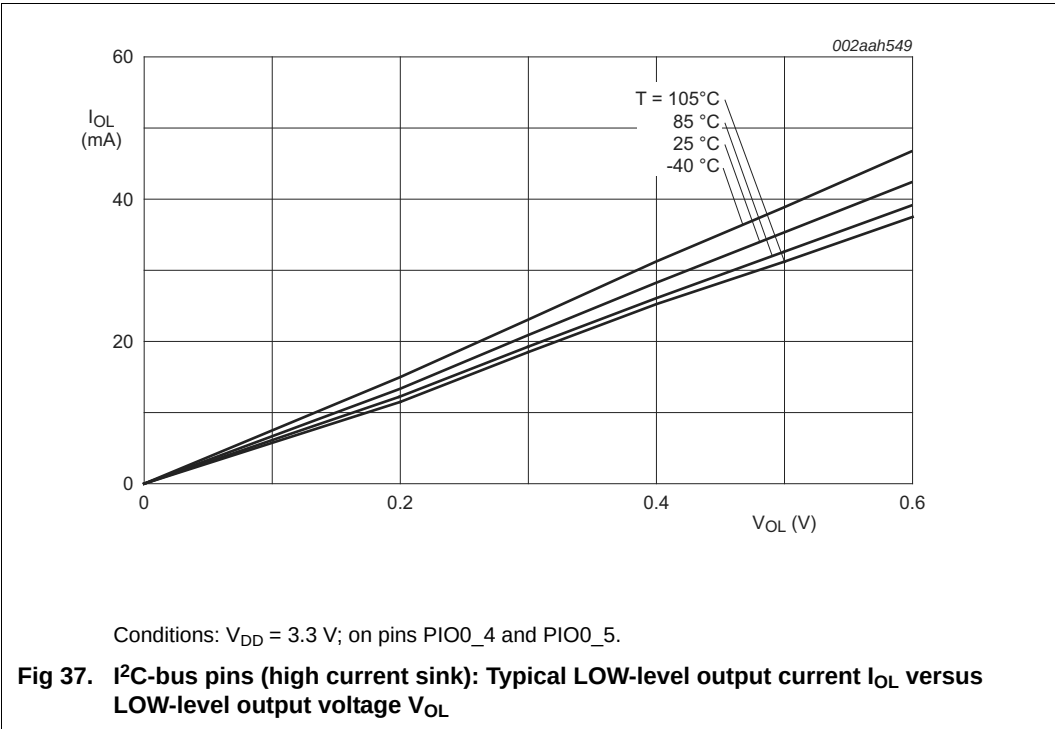
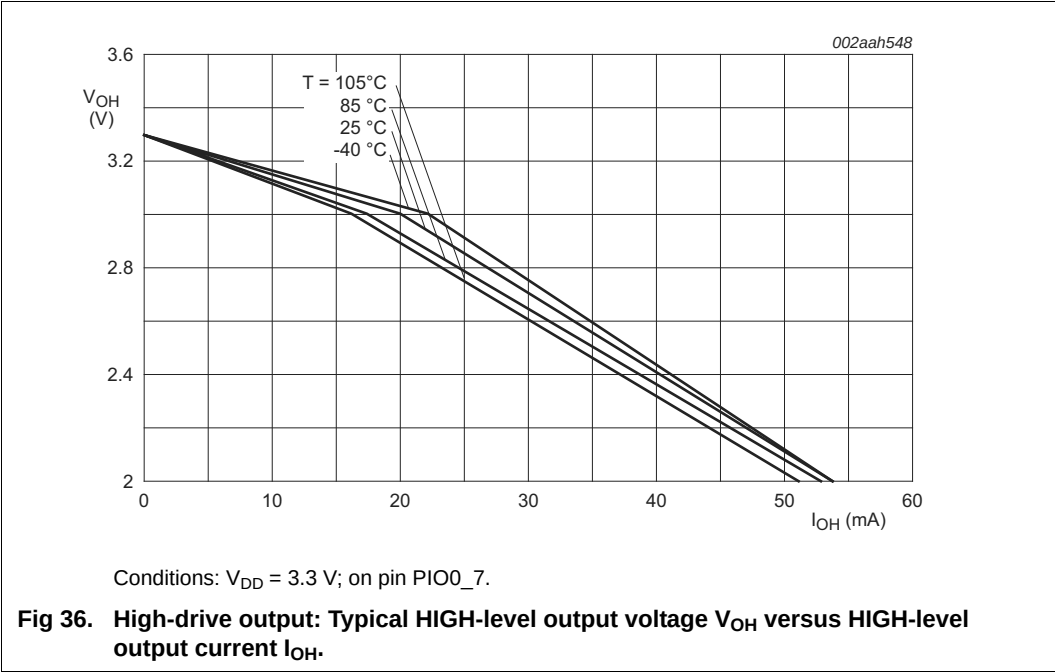
[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

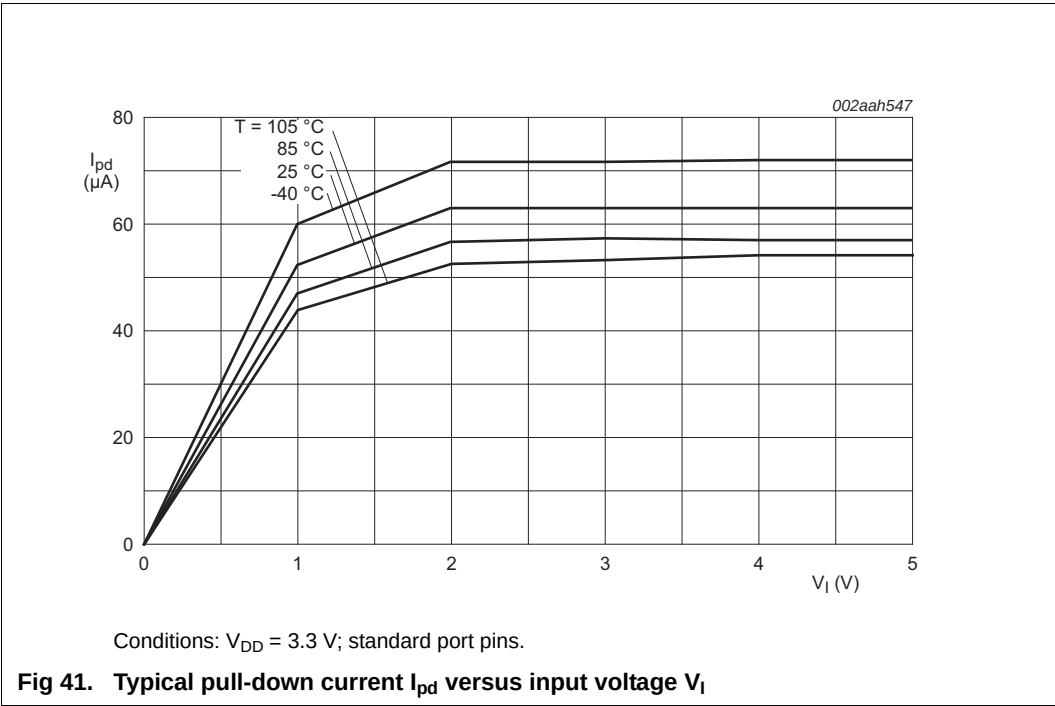
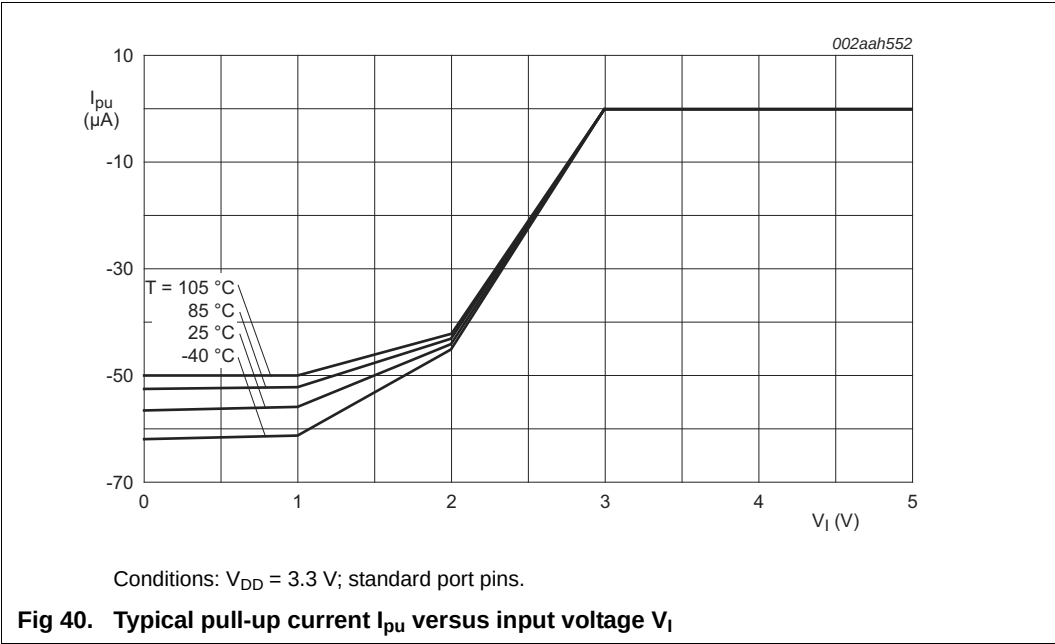
10.8 CoreMark data

Remark: All CoreMark data were taken with the Keil uVision v. 4.6 tool.



10.10 Electrical pin characteristics





11.6 I²C-bus

Table 28. Dynamic characteristic: I²C-bus pins^[1]

$T_{amb} = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$.^[2]

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency	Standard-mode	0	100	kHz
		Fast-mode	0	400	kHz
		Fast-mode Plus	0	1	MHz
t_f	fall time ^{[4][5][6][7]}	of both SDA and SCL signals Standard-mode	-	300	ns
		Fast-mode	$20 + 0.1 \times C_b$	300	ns
		Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock	Standard-mode	4.7	-	μs
		Fast-mode	1.3	-	μs
		Fast-mode Plus	0.5	-	μs
t_{HIGH}	HIGH period of the SCL clock	Standard-mode	4.0	-	μs
		Fast-mode	0.6	-	μs
		Fast-mode Plus	0.26	-	μs
$t_{HD;DAT}$	data hold time ^{[3][4][8]}	Standard-mode	0	-	μs
		Fast-mode	0	-	μs
		Fast-mode Plus	0	-	μs
$t_{SU;DAT}$	data set-up time ^{[9][10]}	Standard-mode	250	-	ns
		Fast-mode	100	-	ns
		Fast-mode Plus	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

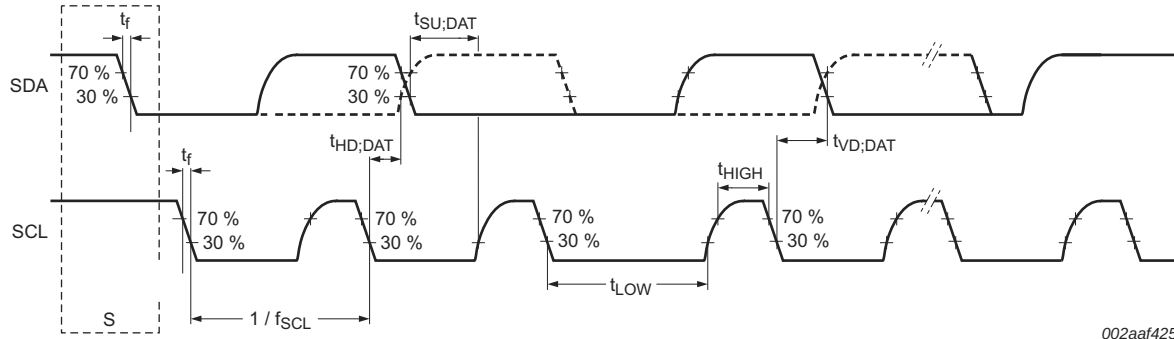
[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f .

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT} = 250\text{ ns}$ must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{f(max)} + t_{SU;DAT} = 1000 + 250 = 1250\text{ ns}$ (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

Fig 46. I²C-bus pins clock timing

11.7 SPI interfaces

Table 29. Dynamic characteristics of SPI pins in SPI mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPI master (in SPI mode)						
$T_{cy(clk)}$	clock cycle time	full-duplex mode ^[1]	50	-	-	ns
		when only transmitting ^[1]	40			ns
t_{DS}	data set-up time	in SPI mode ^[2]	15	-	-	ns
		$2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$				
		$2.0\text{ V} \leq V_{DD} < 2.4\text{ V}$ ^[2]	20			ns
		$1.8\text{ V} \leq V_{DD} < 2.0\text{ V}$ ^[2]	24	-	-	ns
t_{DH}	data hold time	in SPI mode ^[2]	0	-	-	ns
$t_{V(Q)}$	data output valid time	in SPI mode ^[2]	-	-	10	ns
$t_{h(Q)}$	data output hold time	in SPI mode ^[2]	0	-	-	ns
SPI slave (in SPI mode)						
$T_{cy(PCLK)}$	PCLK cycle time		20	-	-	ns
t_{DS}	data set-up time	in SPI mode ^{[3][4]}	0	-	-	ns
t_{DH}	data hold time	in SPI mode ^{[3][4]}	$3 \times T_{cy(PCLK)} + 4$	-	-	ns
$t_{V(Q)}$	data output valid time	in SPI mode ^{[3][4]}	-	-	$3 \times T_{cy(PCLK)} + 11$	ns
$t_{h(Q)}$	data output hold time	in SPI mode ^{[3][4]}	-	-	$2 \times T_{cy(PCLK)} + 5$	ns

[1] $T_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPSPVSR) / f_{main}$. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main} , the SPI peripheral clock divider (SSPCLKDIV), the SPI SCR parameter (specified in the SSP0CR0 register), and the SPI CPSPVSR parameter (specified in the SPI clock prescale register).

[2] $T_{amb} = -40\text{ °C to }105\text{ °C}$.

[3] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$.

[4] $T_{amb} = 25\text{ °C}$; for normal voltage supply range: $V_{DD} = 3.3\text{ V}$.

12.8 ADC effective input impedance

A simplified diagram of the ADC input channels can be used to determine the effective input impedance seen from an external voltage source. See [Figure 53](#).

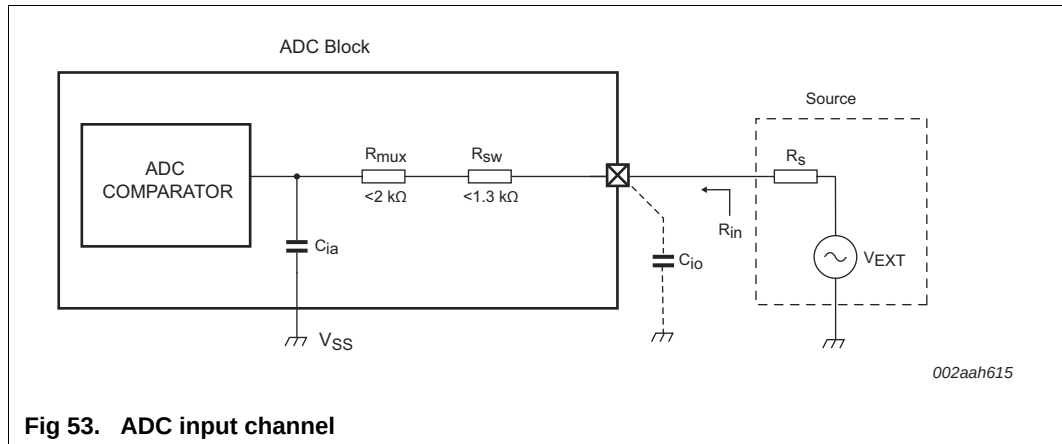


Fig 53. ADC input channel

The effective input impedance, R_{in} , seen by the external voltage source, V_{EXT} , is the parallel impedance of $((1/f_s \times C_{ia}) + R_{mux} + R_{sw})$ and $(1/f_s \times C_{io})$, and can be calculated using [Equation 2](#) with

f_s = sampling frequency

C_{ia} = ADC analog input capacitance

R_{mux} = analog mux resistance

R_{sw} = switch resistance

C_{io} = pin capacitance

$$R_{in} = \left(\frac{1}{f_s \times C_{ia}} + R_{mux} + R_{sw} \right) \parallel \left(\frac{1}{f_s \times C_{io}} \right) \quad (2)$$

Under nominal operating condition $V_{DD} = 3.3$ V and with the maximum sampling frequency $f_s = 400$ kHz, the parameters assume the following values:

$C_{ia} = 1$ pF (max)

$R_{mux} = 2$ kΩ (max)

$R_{sw} = 1.3$ kΩ (max)

$C_{io} = 7.1$ pF (max)

The effective input impedance with these parameters is $R_{in} = 308$ kΩ.

Footprint information for reflow soldering of HVQFN33 package

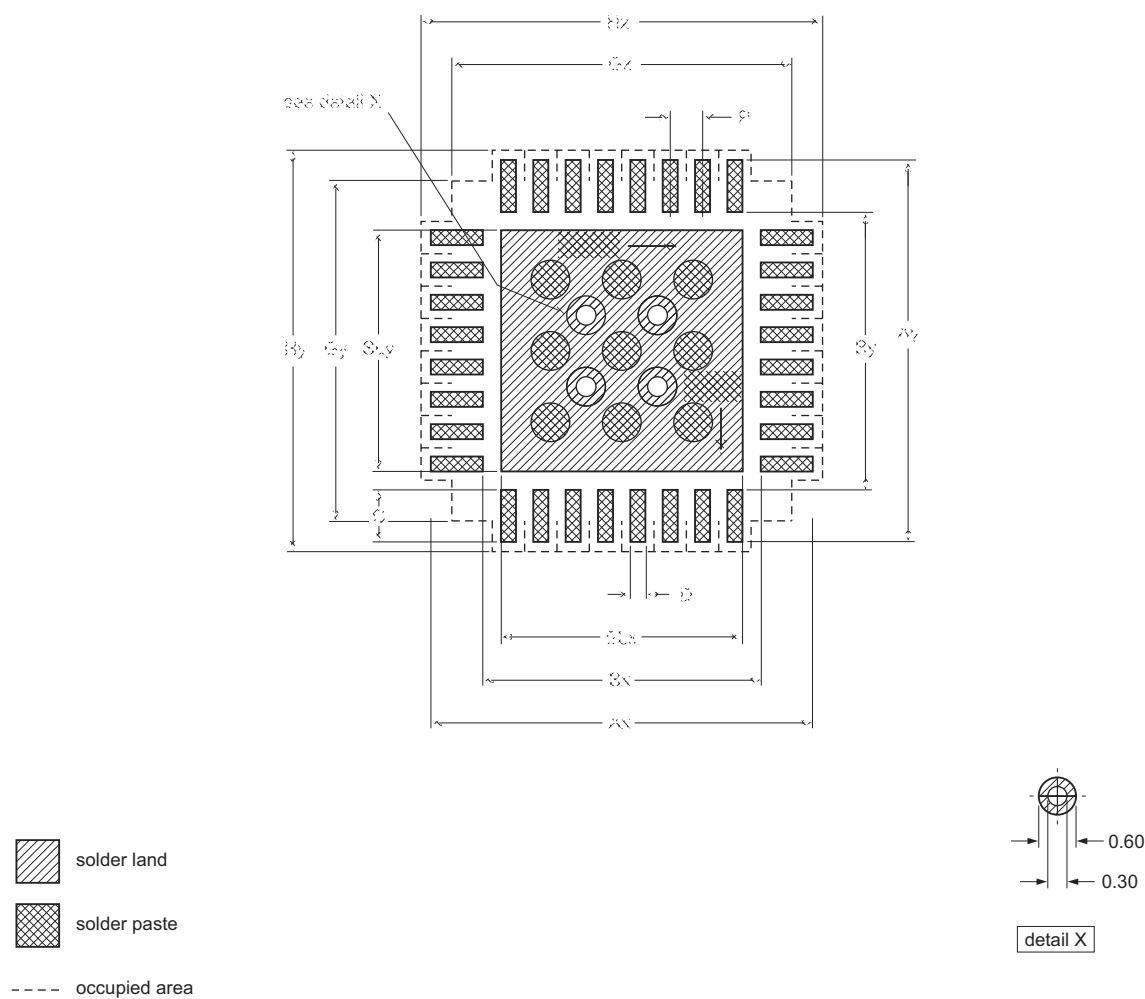


Fig 67. Reflow soldering of the HVQFN33 package (5x5)