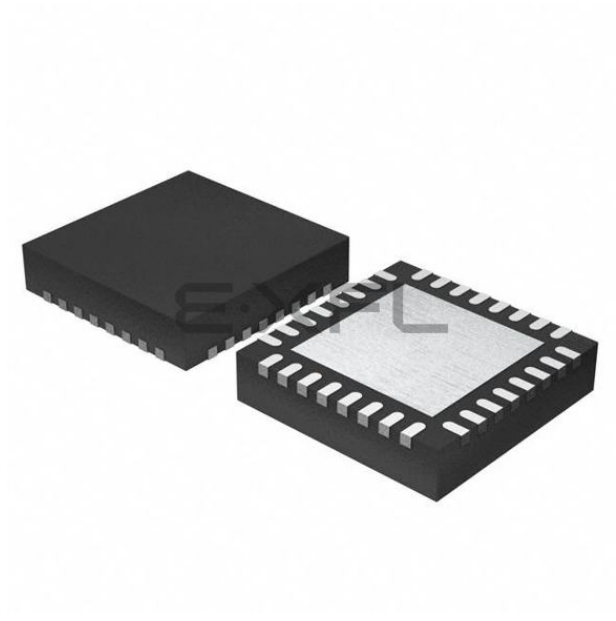

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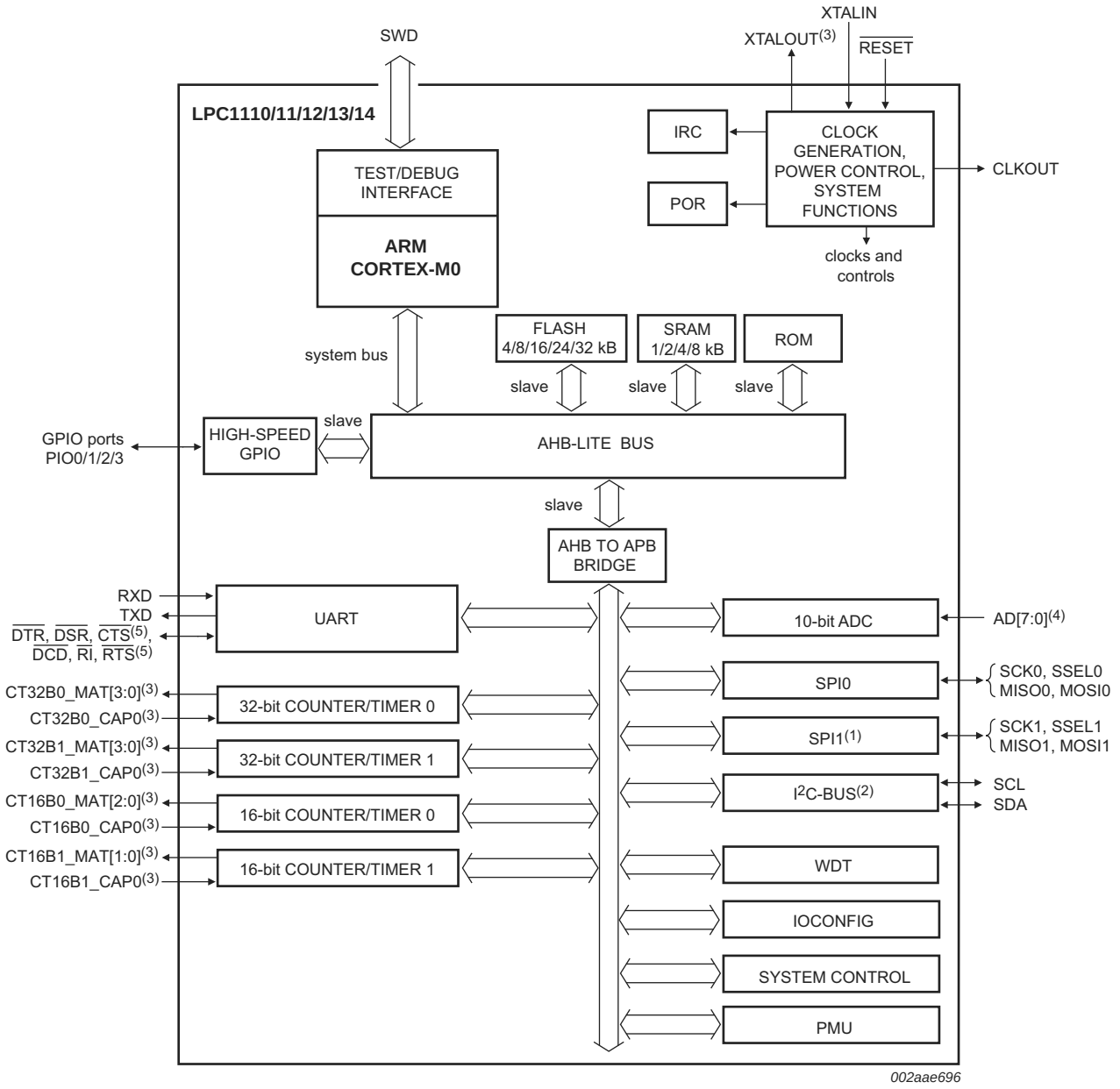
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	28
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-HVQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1112fhi33-102-5

5. Block diagram



(1) LQFP48 packages only.

(2) Not on LPC1112FDH20/102.

(3) All pins available on LQFP48 and HVQFN33 packages. CT16B1_MAT1 not available on TSSOP28/DIP28 packages. CT32B1_MAT3, CT16B1_CAP0, CT16B1_MAT[1:0], CT32B0_CAP0 not available on TSSOP20/SO20 packages. CT16B1_MAT[1:0], CT32B0_CAP0 not available on the HVQFN24 package. XTALOUT not available on LPC1112FHN24.

(4) AD[7:0] available on LQFP48 and HVQFN33 packages. AD[5:0] available on TSSOP28/DIP28 packages. AD[4:0] available on TSSOP20/SO20 packages.

(5) All pins available on LQFP48 packages. RXD, TXD, $\overline{\text{DTR}}$, $\overline{\text{CTS}}$, $\overline{\text{RTS}}$ available on HVQFN 33 packages. RXD, TXD, $\overline{\text{CTS}}$, $\overline{\text{RTS}}$ available on TSSOP28/DIP28 packages. RXD, TXD, $\overline{\text{CTS}}$ available on HVQFN24 packages. RXD, TXD available on TSSOP20/SO20 packages.

Fig 1. LPC1100/LPC1100L series block diagram

Table 7. LPC1100L series: LPC1112/14 pin description table (TSSOP28 and DIP28 packages)

Symbol	Pin TSSOP28/ DIP28	Start logic input	Type	Reset state [1]	Description
PIO0_0 to PIO0_11			I/O		**Port 0 —** Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.
$\overline{\text{RESET}}$/PIO0_0	23 [2]	yes	I	I; PU	**$\overline{\text{RESET}}$ —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO pin if an external $\overline{\text{RESET}}$ function is not needed and Deep power-down mode is not used.
			I/O	-	**PIO0_0 —** General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/ CT32B0_MAT2	24 [3]	yes	I/O	I; PU	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
			O	-	**CLKOUT —** Clockout pin.
			O	-	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	25 [3]	yes	I/O	I; PU	**PIO0_2 —** General purpose digital input/output pin.
			I/O	-	**SSEL0 —** Slave Select for SPI0.
			I	-	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO0_3	26 [3]	yes	I/O	I; PU	**PIO0_3 —** General purpose digital input/output pin.
PIO0_4/SCL	27 [4]	yes	I/O	I; IA	**PIO0_4 —** General purpose digital input/output pin (open-drain).
			I/O	-	**SCL —** I^2C-bus, open-drain clock input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	5 [4]	yes	I/O	I; IA	**PIO0_5 —** General purpose digital input/output pin (open-drain).
			I/O	-	**SDA —** I^2C-bus, open-drain data input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	6 [3]	yes	I/O	I; PU	**PIO0_6 —** General purpose digital input/output pin.
			I/O	-	**SCK0 —** Serial clock for SPI0.
PIO0_7/$\overline{\text{CTS}}$	28 [3]	yes	I/O	I; PU	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
			I	-	**$\overline{\text{CTS}}$ —** Clear To Send input for UART.
PIO0_8/MISO0/ CT16B0_MAT0	1 [3]	yes	I/O	I; PU	**PIO0_8 —** General purpose digital input/output pin.
			I/O	-	**MISO0 —** Master In Slave Out for SPI0.
			O	-	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	2 [3]	yes	I/O	I; PU	**PIO0_9 —** General purpose digital input/output pin.
			I/O	-	**MOSI0 —** Master Out Slave In for SPI0.
			O	-	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.

Table 7. LPC1100L series: LPC1112/14 pin description table (TSSOP28 and DIP28 packages) *…continued*

Symbol	Pin TSSOP28/ DIP28	Start logic input	Type	Reset state [1]	Description
SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2	3 [3]	yes	I	I; PU	**SWCLK —** Serial wire clock.
			I/O	-	**PIO0_10 —** General purpose digital input/output pin.
			I/O	-	**SCK0 —** Serial clock for SPI0.
			O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
R/PIO0_11/ AD0/CT32B0_MAT3	4 [5]	yes	I	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO0_11 —** General purpose digital input/output pin.
			I	-	**AD0 —** A/D converter, input 0.
			O	-	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
PIO1_0 to PIO1_9			I/O		**Port 1 —** Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block.
R/PIO1_0/ AD1/CT32B1_CAP0	9 [5]	yes	I	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO1_0 —** General purpose digital input/output pin.
			I	-	**AD1 —** A/D converter, input 1.
			I	-	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
R/PIO1_1/ AD2/CT32B1_MAT0	10 [5]	no	O	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO1_1 —** General purpose digital input/output pin.
			I	-	**AD2 —** A/D converter, input 2.
			O	-	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
R/PIO1_2/ AD3/CT32B1_MAT1	11 [5]	no	I	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO1_2 —** General purpose digital input/output pin.
			I	-	**AD3 —** A/D converter, input 3.
			O	-	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ AD4/CT32B1_MAT2	12 [5]	no	I/O	I; PU	**SWDIO —** Serial wire debug input/output.
			I/O	-	**PIO1_3 —** General purpose digital input/output pin.
			I	-	**AD4 —** A/D converter, input 4.
			O	-	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
PIO1_4/AD5/ CT32B1_MAT3/ WAKEUP	13 [5]	no	I/O	I; PU	**PIO1_4 —** General purpose digital input/output pin with 10 ns glitch filter. In Deep power-down mode, this pin serves as the Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
			I	-	**AD5 —** A/D converter, input 5.
			O	-	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.

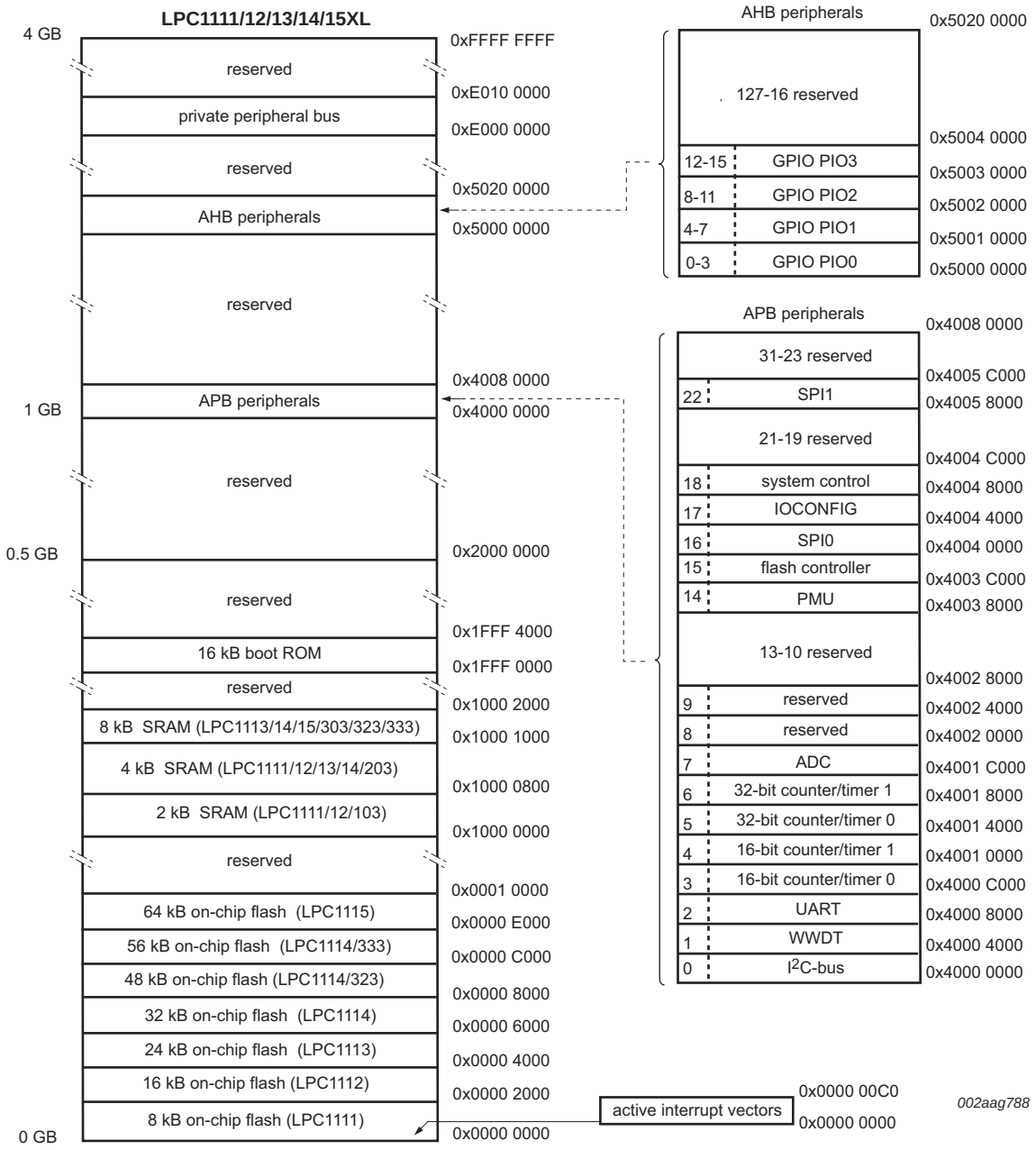


Fig 15. LPC1100XL series memory map

7.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.

- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

7.10 I²C-bus serial I/O controller

The LPC1110/11/12/13/14/15 contain one I²C-bus controller.

Remark: Part LPC1112FDH20/102 does not contain the I²C-bus controller.

The I²C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock Line (SCL) and a Serial DAta line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.10.1 Features

- The I²C-interface is a standard I²C-bus compliant interface with open-drain pins. The I²C-bus interface also supports Fast-mode Plus with bit rates up to 1 Mbit/s.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I²C-bus can be used for test and diagnostic purposes.
- The I²C-bus controller supports multiple address recognition and a bus monitor mode.

7.11 10-bit ADC

The LPC1110/11/12/13/14/15 contain one ADC. It is a single 10-bit successive approximation ADC with eight channels.

7.11.1 Features

- 10-bit successive approximation ADC.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 V to V_{DD}.
- 10-bit conversion time $\geq$ 2.44 μs (up to 400 kSamples/s).
- Burst conversion mode for single or multiple inputs.

10. Static characteristics

10.1 LPC1100, LPC1100L series

Table 16. Static characteristics (LPC1100, LPC1100L series)

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{DD}	supply voltage (core and external rail)		1.8	3.3	3.6	V
LPC1100 series (LPC111x/101/201/301) power consumption						
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash				
		system clock = 12 MHz; V_{DD} = 3.3 V [2][3][4][5][6]	-	3	-	mA
		system clock = 50 MHz; V_{DD} = 3.3 V [2][3][5][6][7]	-	9	-	mA
		Sleep mode; system clock = 12 MHz; V_{DD} = 3.3 V [2][3][4][5][6]	-	2	-	mA
		Deep-sleep mode; V_{DD} = 3.3 V [2][3][8]	-	6	-	μA
		Deep power-down mode; V_{DD} = 3.3 V [2][9]	-	220	-	nA
LPC1100L series (LPC111x/002/102/202/302) power consumption in low-current mode[11]						
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash				
		system clock = 1 MHz; V_{DD} = 3.3 V [2][3][5][6][10]	-	840	-	μA
		system clock = 6 MHz; V_{DD} = 3.3 V [2][3][5][6][10]	-	1	-	mA
		system clock = 12 MHz; V_{DD} = 3.3 V [2][3][4][5][6]	-	2	-	mA
		system clock = 50 MHz; V_{DD} = 3.3 V [2][3][5][6][7]	-	7	-	mA
		Sleep mode; system clock = 12 MHz; V_{DD} = 3.3 V [2][3][4][5][6]	-	1	-	mA
		system clock = 50 MHz; V_{DD} = 3.3 V [2][3][4][5][6]	-	5	-	mA
		Deep-sleep mode; V_{DD} = 3.3 V [2][3][8]	-	2	-	μA
		Deep power-down mode; V_{DD} = 3.3 V [2][9]	-	220	-	nA

Table 16. Static characteristics (LPC1100, LPC1100L series) *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled	-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function [12][13][14]	0	-	5.0	V
V_O	output voltage	output active	0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage		0.4	-	-	V
V_{OH}	HIGH-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OH} = −20 mA	V_{DD} − 0.4	-	-	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OH} = −12 mA	V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OL} = 4 mA	-	-	0.4	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OL} = 3 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V; 2.5 V ≤ V_{DD} ≤ 3.6 V	20	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V	12	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 2.5 V ≤ V_{DD} ≤ 3.6 V	4	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V	3	-	-	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD} [15]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V 2.0 V ≤ V_{DD} ≤ 3.6 V	−15	−50	−85	μA
		1.8 V ≤ V_{DD} < 2.0 V	−10	−50	−85	μA
		V_{DD} < V_I < 5 V	0	0	0	μA
I^2C-bus pins (PIO0_4 and PIO0_5)						
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage		-	0.05V_{DD}	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins 2.5 V ≤ V_{DD} ≤ 3.6 V	3.5	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V	3	-	-	

10.2 LPC1100XL series

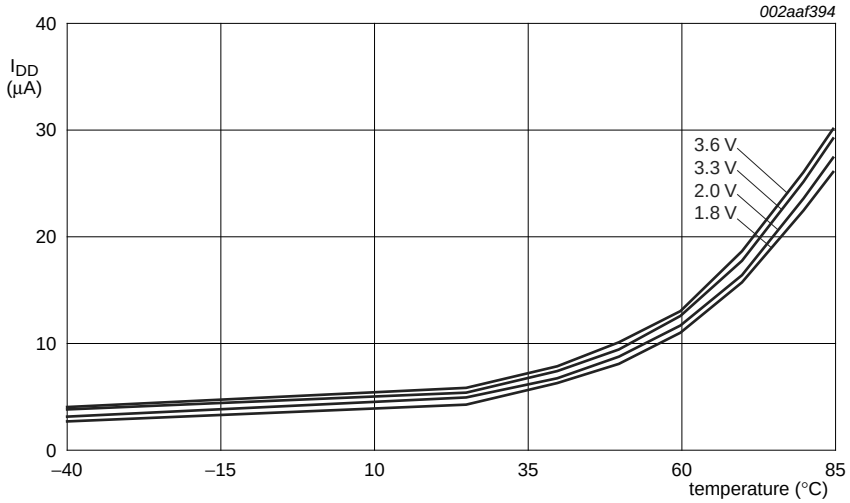
Table 17. Static characteristics (LPC1100XL series)

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{DD}	supply voltage (core and external rail)		1.8	3.3	3.6	V
LPC1100XL series (LPC111x/103/203/303/323/333) power consumption in low-current mode[2]						
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash				
		system clock = 3 MHz; V_{DD} = 3.3 V [3][4][5][6][7]	-	600	-	μA
		system clock = 6 MHz; V_{DD} = 3.3 V [3][4][5][6][7]	-	850	-	μA
		system clock = 12 MHz; V_{DD} = 3.3 V [3][4][6][7][8]	-	1.4	-	mA
		system clock = 50 MHz; V_{DD} = 3.3 V [3][4][6][7][9]	-	5.8	-	mA
		Sleep mode; system clock = 12 MHz; V_{DD} = 3.3 V [3][4][6][7][8]	-	700	-	μA
		system clock = 50 MHz; V_{DD} = 3.3 V [3][4][6][7][8]	-	2.2	-	mA
		Deep-sleep mode; V_{DD} = 3.3 V; 25 °C [3][4][10]	-	1.8	15	μA
		Deep-sleep mode; V_{DD} = 3.3 V; 105 °C [4][10][11]	-	-	50	μA
		Deep power-down mode; V_{DD} = 3.3 V; 25 °C [3][12]	-	220	1000	nA
		Deep power-down mode; V_{DD} = 3.3 V; 105 °C [11][12]	-	-	3	μA
Standard port pins, $\overline{\text{RESET}}$						
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled	-	0.5	10	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled	-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled	-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function [13][14][15]	0	-	5.0	V
V_O	output voltage	output active	0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	-	V

Table 17. Static characteristics (LPC1100XL series) *…continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage		-	0.4	-	V
V_{OH}	HIGH-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OH} = −4 mA	V_{DD} − 0.4	-	-	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OH} = −3 mA	V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OL} = 4 mA	-	-	0.4	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OL} = 3 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V; 2.5 V ≤ V_{DD} ≤ 3.6 V	−4	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V	−3	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 2.5 V ≤ V_{DD} ≤ 3.6 V	4	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V	3	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V [16]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD} [16]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V; 2.0 V ≤ V_{DD} ≤ 3.6 V	−15	−50	−85	µA
		1.8 V ≤ V_{DD} < 2.0 V	−10	−50	−85	µA
		V_{DD} < V_I < 5 V	0	0	0	µA
High-drive output pin (PIO0_7)						
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled	-	0.5	10	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled	-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled	-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function [13][14][15]	0	-	5.0	V
V_O	output voltage	output active	0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage		0.4	-	-	V



Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 21. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD} (for LPC111x/101/201/301)

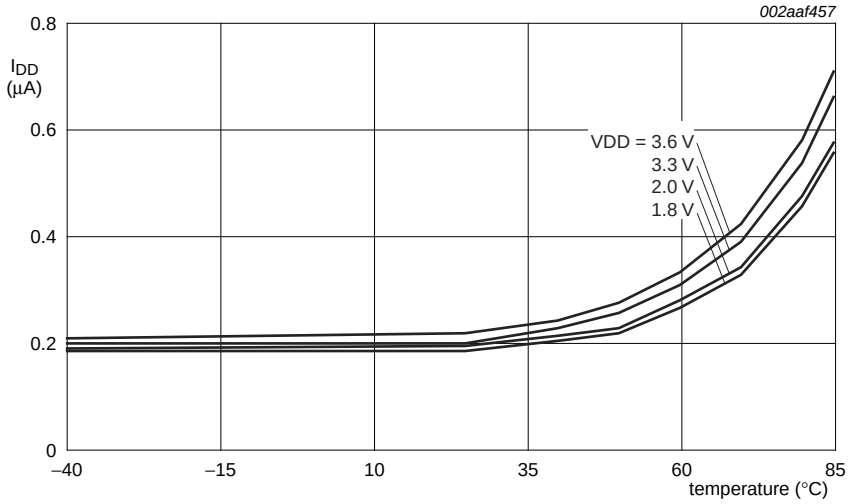
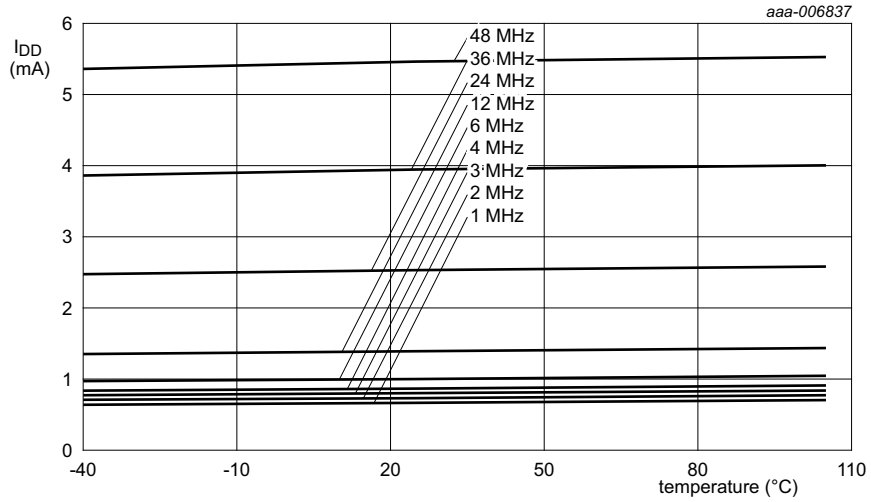


Fig 22. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD} (for LPC111x/101/201/301)



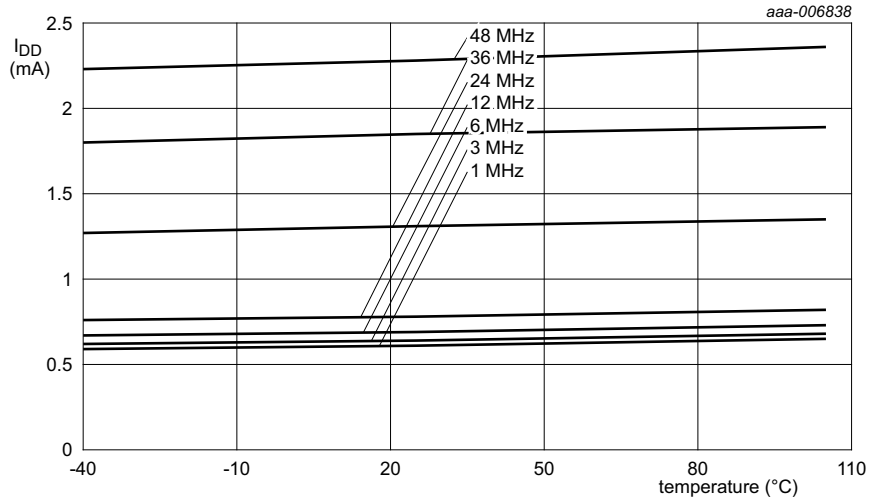
Conditions: V_{DD} = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz to 6 MHz: system oscillator enabled; PLL, IRC disabled.

12 MHz: IRC enabled; system oscillator, PLL disabled.

24 MHz to 48 MHz: IRC disabled; system oscillator, PLL enabled.

Fig 29. Active mode: Typical supply current I_{DD} versus temperature for different system clock frequencies (for LPC111xXL)



Conditions: V_{DD} = 3.3 V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz to 6 MHz: system oscillator enabled; PLL, IRC disabled.

12 MHz: IRC enabled; system oscillator, PLL disabled.

24 MHz to 48 MHz: IRC disabled; system oscillator, PLL enabled.

Fig 30. Sleep mode: Typical supply current I_{DD} versus temperature for different system clock frequencies (for LPC111xXL)

10.9 Peripheral power consumption

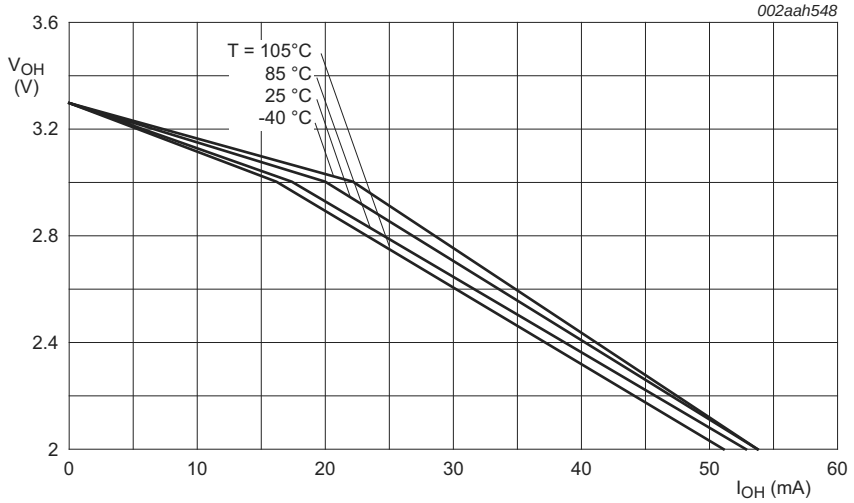
The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at T_{amb} = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 48 MHz.

Table 21. Power consumption for individual analog and digital blocks

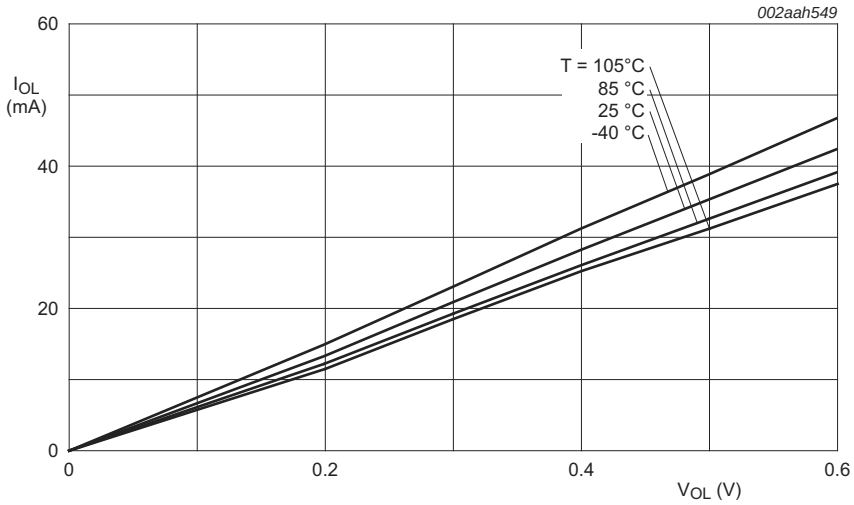
Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	48 MHz	
IRC	0.27	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	0.22	-	-	IRC running; PLL off; independent of main clock frequency.
Watchdog oscillator at 500 kHz/2	0.004	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	0.051	-	-	Independent of main clock frequency.
Main PLL	-	0.21	-	
ADC	-	0.08	0.29	
CLKOUT	-	0.12	0.47	Main clock divided by 4 in the CLKOUTDIV register.
CT16B0	-	0.02	0.06	
CT16B1	-	0.02	0.06	
CT32B0	-	0.02	0.07	
CT32B1	-	0.02	0.06	
GPIO	-	0.23	0.88	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
IOCONFIG	-	0.03	0.10	
I2C	-	0.04	0.13	
ROM	-	0.04	0.15	
SPI0	-	0.12	0.45	
SPI1	-	0.12	0.45	
UART	-	0.22	0.82	
WDT/WWDT	-	0.02	0.06	Main clock selected as clock source for the WDT.

10.10 Electrical pin characteristics



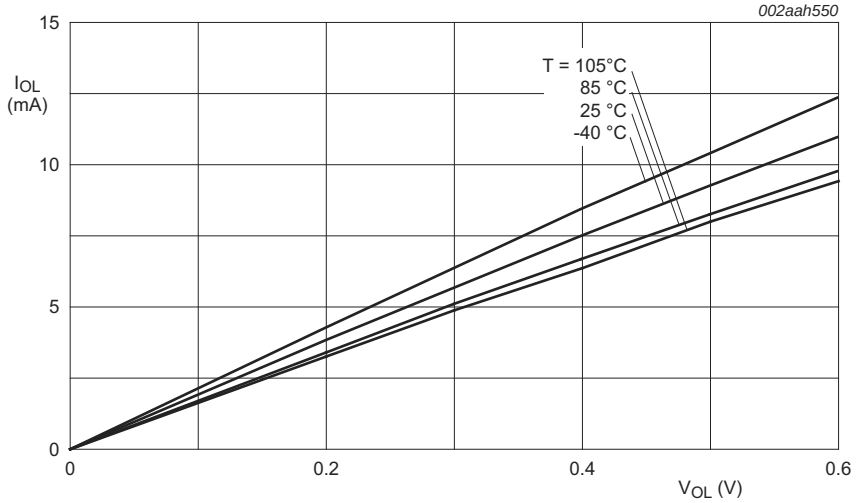
Conditions: V_{DD} = 3.3 V; on pin PIO0_7.

Fig 36. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}.



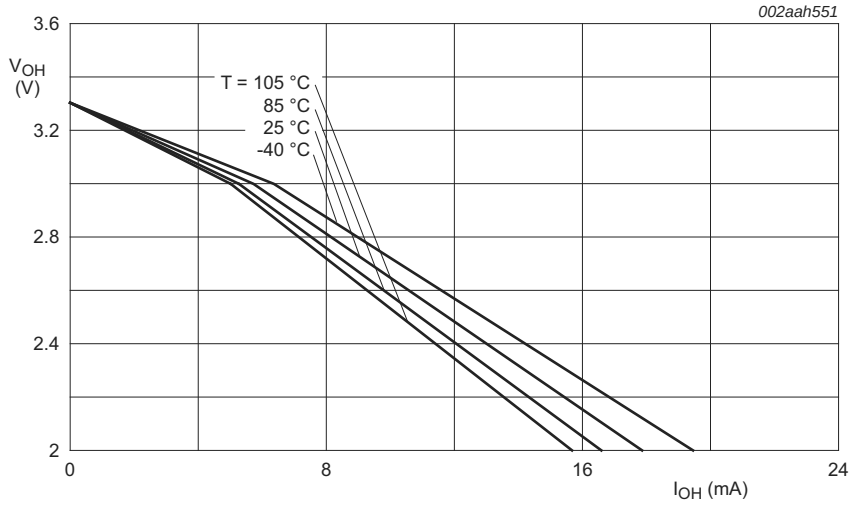
Conditions: V_{DD} = 3.3 V; on pins PIO0_4 and PIO0_5.

Fig 37. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



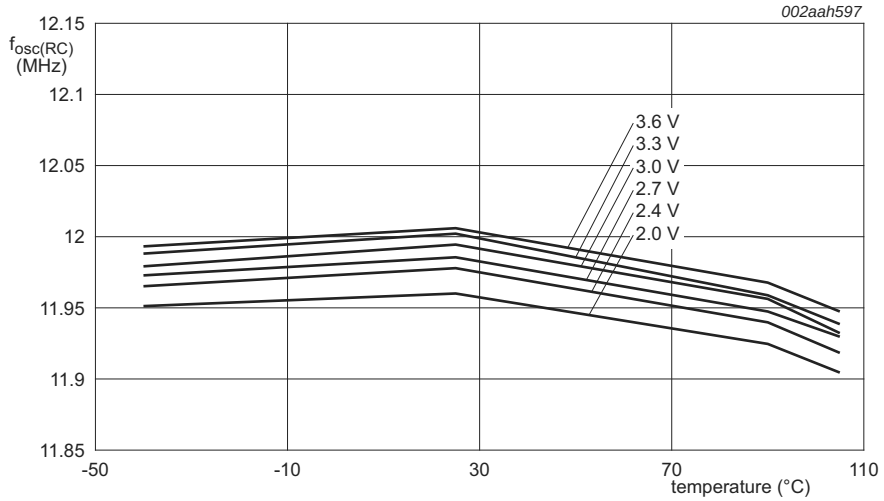
Conditions: V_{DD} = 3.3 V; standard port pins and PIO0_7.

Fig 38. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 39. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: Frequency values are typical values. 12 MHz ± 1 % accuracy is guaranteed for 2.7 V ≤ V_{DD} ≤ 3.6 V and T_{amb} = −40 °C to +105 °C. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1 % accuracy specification for voltages below 2.7 V.

Fig 45. Internal RC oscillator frequency versus temperature (J parts)

Table 26. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register; [2][3]	-	9.4	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register [2][3]	-	2300	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +105 °C) is ±40 %.

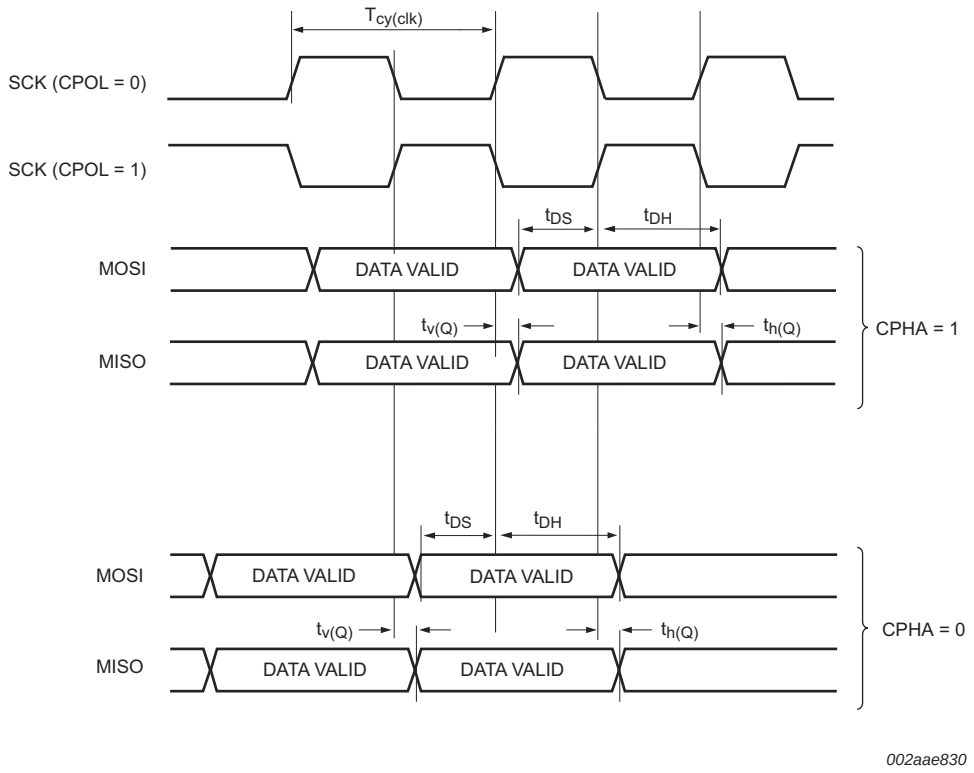
[3] See the LPC111x user manual.

11.5 I/O pins

Table 27. Dynamic characteristic: I/O pins[1]
T_{amb} = −40 °C to +105 °C; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	pin configured as output	3.0	-	5.0	ns
t_f	fall time	pin configured as output	2.5	-	5.0	ns

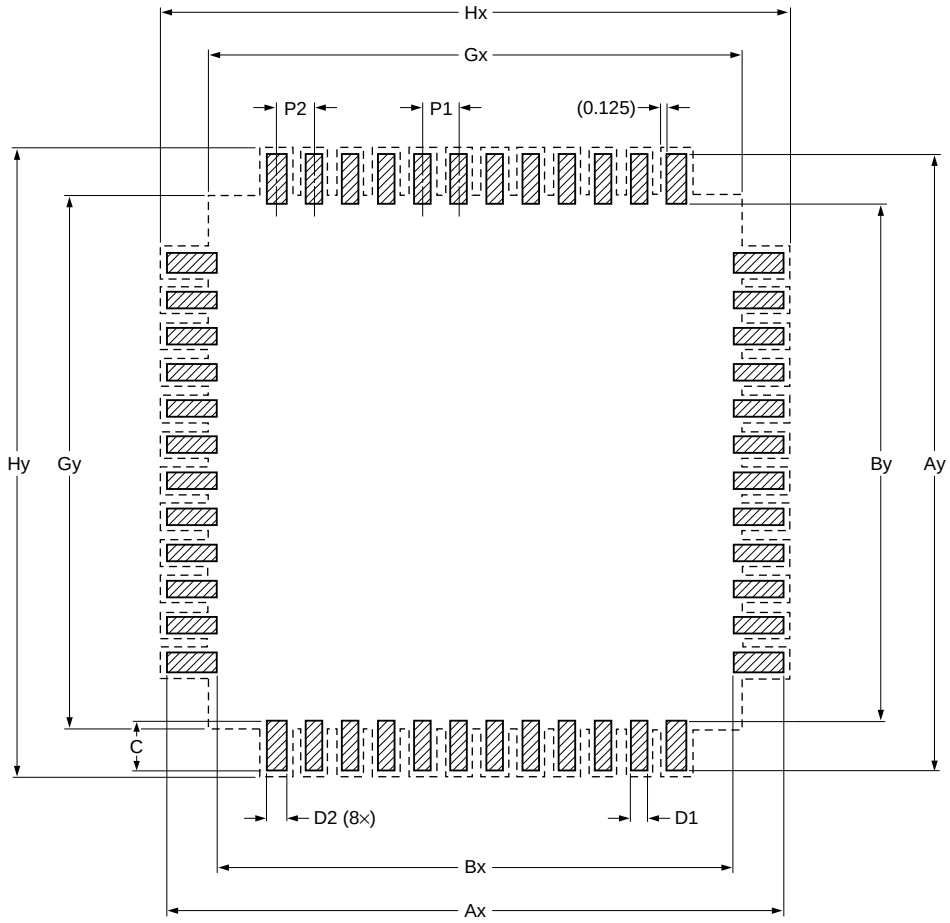
[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.



Pin names SCK, MISO, and MOSI refer to pins for both SPI peripherals, SPI0 and SPI1.

Fig 48. SPI slave timing in SPI mode

Footprint information for reflow soldering of LQFP48 package **SOT313-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	10.350	10.350	7.350	7.350	1.500	0.280	0.500	7.500	7.500	10.650	10.650

sot313-2_fr

Fig 69. Reflow soldering of the LQFP48 package

17. Revision history

Table 34. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC111X v.9.2	20140326	Product data sheet	-	LPC111X v.9.1
Modifications:	• Pin description tables for RESET/PIO0_0 updated: In deep power-down mode, this pin must be pulled HIGH externally. The RESET pin can be left unconnected or be used as a GPIO pin if an external RESET function is not needed. See Section 6.2. • Pin description notes relating to open-drain I2C-bus pins updated for clarity in Section 6.2. • Pin description of the WAKEUP pin updated for clarity. See Section 6.2. • Parts added: LPC1114JHI33/303, LPC1111JHN33/103, LPC1112JHN33/203, LPC1113JHN33/203, LPC1114JHN33/303, LPC1114JBD48/333, LPC1112FHI33/102, LPC1114JBD48/303, LPC1114JBD48/323, LPC1113JBD48/303, LPC1113JHN33/303, LPC1112JHN33/103, LPC1111JHN33/203, LPC1114JHN33/203.			
LPC111X v.9.1	20131213	Product data sheet	-	LPC111X v.9
Modifications:	• Table 17 “Static characteristics (LPC1100XL series)”: – Added I_{DD} max spec for Deep-sleep and Deep power-down modes @ 25 °C and 105 °C. – Added Table note 11 “105 °C spec applies only to the LPC1112JHI33, LPC1114JHN33, LPC1115JBD48, and LPC1115JET48 parts.” – Updated Table note 12 “WAKEUP pin and RESET pin are pulled HIGH externally.” • Table 16 “Static characteristics (LPC1100, LPC1100L series)”: – Updated Table note 9 “WAKEUP pin and RESET pin are pulled HIGH externally.”			
LPC111X v.9	20131029	Product data sheet	-	LPC111X v.8.2
Modifications:	• Added LPC1112JHI33/203, LPC1114JHN33/333, LPC1115JBD48/303, and LPC1115JET48/303 parts. • Removed $t_{clk(H)}$ and $t_{clk(L)}$ from Figure 47 “SPI master timing in SPI mode” and Figure 48 “SPI slave timing in SPI mode”; spec not characterized. • Table 22 “Power-up characteristics[1]”: Added table note “Does not apply to LPC1100XL series”.			
LPC111X v.8.2	20130805	Product data sheet	-	LPC111X v.8.1
Modifications:	• Added LPC1115FET48/303.			
LPC111X v.8.1	20130524	Product data sheet	-	LPC111X v.8
Modifications:	• Table 4 thru Table 11: Added “5 V tolerant pad” to RESET/PIO0_0 table note. • Added Section 9 “Thermal characteristics”. • SRAM size corrected for part LPC1112FHN24/202 (4 kB). See Table 2.			
LPC111X v.8	20130220	Product data sheet	-	LPC111X v.7.5
Modifications:	• Table 16 “Static characteristics” added Pin capacitance section. • Default pin state corrected for pins PIO0_4 and PIO0_5 (I; IA) in Table 11 “LPC1100XL series: LPC1111/12/13/14 pin description table (HVQFN33 package)”. • Table 12 “Limiting values” expanded for clarity. • Table 19 “ Power consumption at very low frequencies using the watchdog oscillator” added. • Added Section 12.2 “Use of ADC input trigger signals”. • Added Section 12.8 “ADC effective input impedance”.			
LPC111X v.7.5	20121002	Product data sheet	-	LPC111X v.7.4

Table 34. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	• Power consumption graphs added for parts LPC111x/102/202/302 (Figure 13 to Figure 17). • Parameter V_{hys} for I^2C bus pins: typical value corrected $V_{hys} = 0.05V_{DD}$ in Table 7. • Typical value for parameter N_{endu} added in Table 12 “Flash characteristics”. • I^2C-bus pins configured as standard mode pins, parameter I_{OL} changed to 3.5 mA (minimum) for $2.0\ V \leq V_{DD} \leq 3.6\ V$. • Section 11.6 “ElectroMagnetic Compatibility (EMC)” added. • Power-up characterization added (Section 10.1 “Power-up ramp conditions”).			
LPC1111_12_13_14 v.3	20101110	Product data sheet	-	LPC1111_12_13_14 v.2
Modifications:	• Parts LPC111x/102/202/302 added (LPC1100L series). • Power consumption data for parts LPC111x/102/202/302 added in Table 7. • PLL output frequency limited to 100 MHz in Section 7.15.2. • Description of $\overline{\text{RESET}}$ and WAKEUP functions updated in Section 6. • WDT description updated in Section 7.14. The WDT is a 24-bit timer. • Power profiles added to Section 2 and Section 7 for parts LPC111x/102/202/302.			
LPC1111_12_13_14 v.2	20100818	Product data sheet	-	LPC1111_12_13_14 v.1
Modifications:	• V_{ESD} limit changed to −6500 V (min) /+6500 V (max) in Table 6. • t_{DS} updated for SPI in master mode (Table 17). • Deep-sleep mode functionality changed to allow BOD and watchdog oscillator as the only analog blocks allowed to remain running in Deep-sleep mode (Section 7.15.5.3). • V_{DD} range changed to $3.0\ V \leq V_{DD} \leq 3.6\ V$ in Table 15. • Reset state of pins and start logic functionality added in Table 3 to Table 5. • Section 7.16.1 added. • Section “Memory mapping control” removed. • V_{OH} and I_{OH} specifications updated for high-drive pins in Table 7. • Section 9.4 added.			
LPC1111_12_13_14 v.1	20100416	Product data sheet	-	-