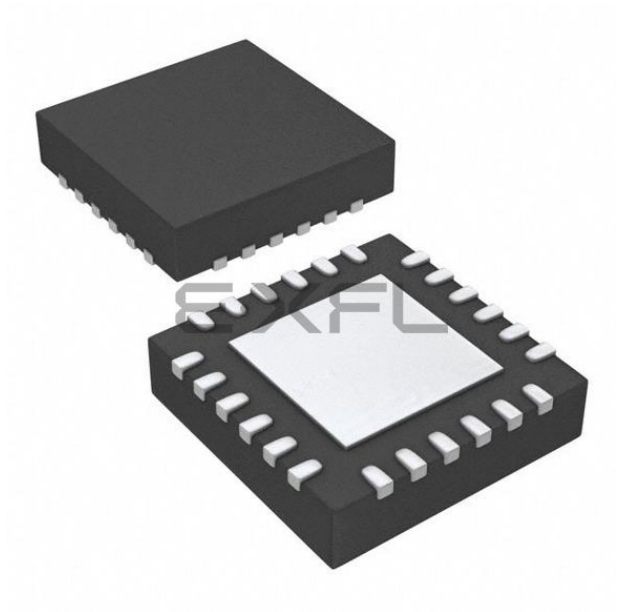

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	19
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VFQFN Exposed Pad
Supplier Device Package	24-HVQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1112fhn24-202-1

Table 3. Pin description overview

Part	Pin description table	Pinning diagram
LPC1114FHN33/203	Table 11	Figure 7
LPC1114JHN33/203	Table 11	Figure 7
LPC1114FHN33/301	Table 9	Figure 6
LPC1114FHN33/302	Table 9	Figure 6
LPC1114JHN33/303	Table 11	Figure 7
LPC1114FHN33/303	Table 11	Figure 7
LPC1114FHN33/333	Table 11	Figure 7
LPC1114JHN33/333	Table 11	Figure 7
LPC1114FHI33/302	Table 9	Figure 6
LPC1114FHI33/303	Table 11	Figure 7
LPC1114JHI33/303	Table 11	Figure 7
LPC1113FBD48/301	Table 8	Figure 3
LPC1113FBD48/302	Table 8	Figure 3
LPC1113FBD48/303	Table 10	Figure 4
LPC1113JBD48/303	Table 10	Figure 4
LPC1114FBD48/301	Table 8	Figure 3
LPC1114FBD48/302	Table 8	Figure 3
LPC1114FBD48/303	Table 10	Figure 4
LPC1114JBD48/303	Table 10	Figure 4
LPC1114FBD48/323	Table 10	Figure 4
LPC1114JBD48/323	Table 10	Figure 4
LPC1114FBD48/333	Table 10	Figure 4
LPC1114JBD48/333	Table 10	Figure 4
LPC1115FBD48/303	Table 10	Figure 4
LPC1115JBD48/303	Table 10	Figure 4
LPC1115FET48/303	Table 10	Figure 5
LPC1115JET48/303	Table 10	Figure 5

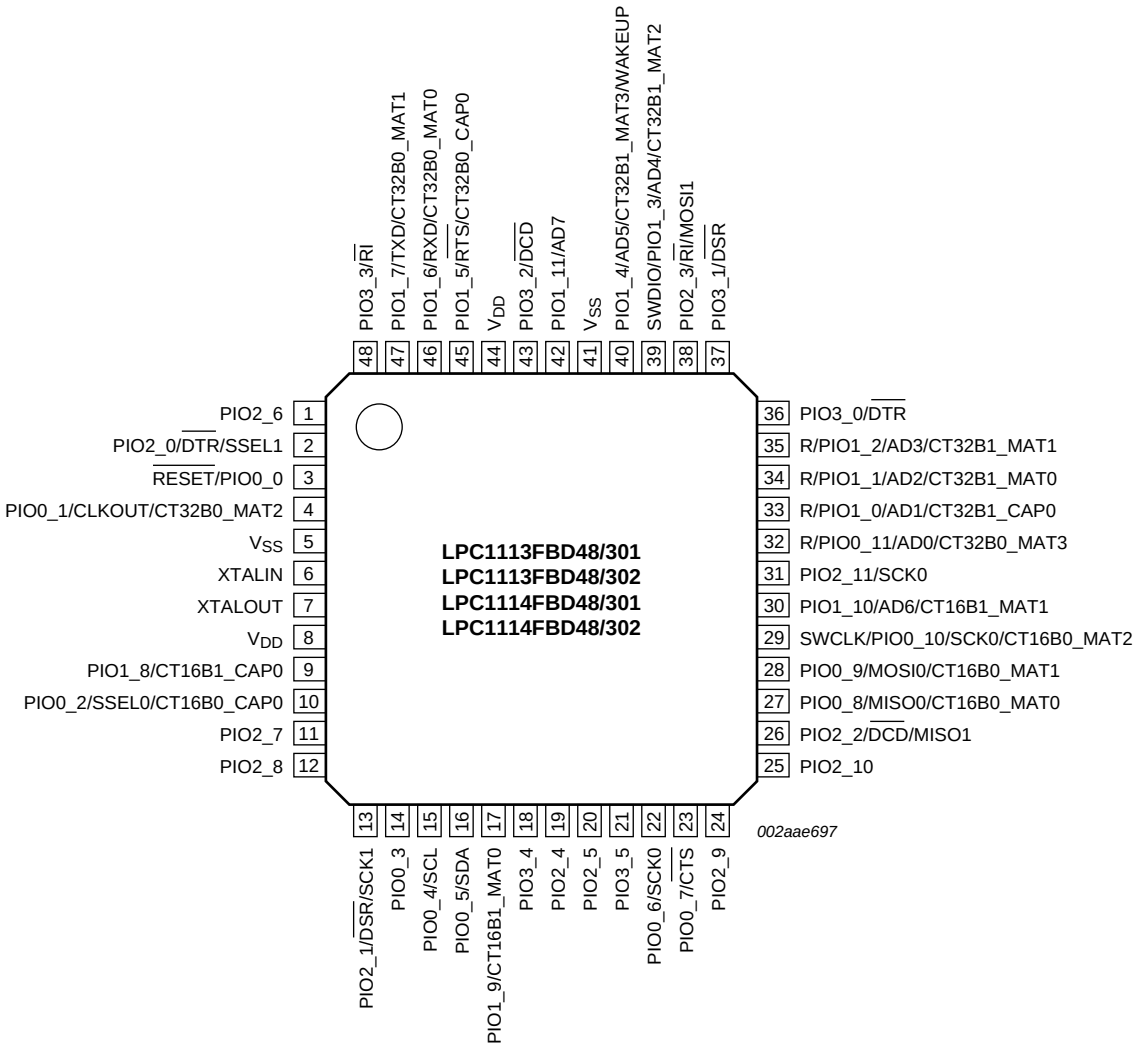


Fig 3. LPC1100 and LPC1100L series pin configuration LQFP48 package

Table 4. LPC1100L series: LPC1110/11/12 pin description table (SO20 and TSSOP20 package with I²C-bus pins) *…continued*

Symbol	Pin SO20/ TSSOP20	Start logic input	Type	Reset state [1]	Description
R/PIO0_11/ AD0/CT32B0_MAT3	4 [5]	yes	I	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO0_11 —** General purpose digital input/output pin.
			I	-	**AD0 —** A/D converter, input 0.
			O	-	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
PIO1_0 to PIO1_7			I/O		**Port 1 —** Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block.
R/PIO1_0/ AD1/CT32B1_CAP0	7 [5]	yes	I	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO1_0 —** General purpose digital input/output pin.
			I	-	**AD1 —** A/D converter, input 1.
			I	-	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
R/PIO1_1/ AD2/CT32B1_MAT0	8 [5]	no	O	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO1_1 —** General purpose digital input/output pin.
			I	-	**AD2 —** A/D converter, input 2.
			O	-	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
R/PIO1_2/ AD3/CT32B1_MAT1	9 [5]	no	I	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO1_2 —** General purpose digital input/output pin.
			I	-	**AD3 —** A/D converter, input 3.
			O	-	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ AD4/CT32B1_MAT2	10 [5]	no	I/O	I; PU	**SWDIO —** Serial wire debug input/output.
			I/O	-	**PIO1_3 —** General purpose digital input/output pin.
			I	-	**AD4 —** A/D converter, input 4.
			O	-	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
PIO1_6/RXD/ CT32B0_MAT0	11 [3]	no	I/O	I; PU	**PIO1_6 —** General purpose digital input/output pin.
			I	-	**RXD —** Receiver input for UART.
			O	-	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO1_7/TXD/ CT32B0_MAT1	12 [3]	no	I/O	I; PU	**PIO1_7 —** General purpose digital input/output pin.
			O	-	**TXD —** Transmitter output for UART.
			O	-	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
V_{DD}	15	-		-	3.3 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	14 [6]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	13 [6]	-	O	-	Output from the oscillator amplifier.
V_{SS}	16	-		-	Ground.

Table 9. LPC1100 and LPC1100L series: LPC1111/12/13/14 pin description table (HVQFN33 package) *…continued*

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO1_7/TXD/ CT32B0_MAT1	32[3]	no	I/O	I;PU	**PIO1_7 —** General purpose digital input/output pin.
			O	-	**TXD —** Transmitter output for UART.
			O	-	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO1_8/ CT16B1_CAP0	7[3]	no	I/O	I;PU	**PIO1_8 —** General purpose digital input/output pin.
			I	-	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
PIO1_9/ CT16B1_MAT0	12[3]	no	I/O	I;PU	**PIO1_9 —** General purpose digital input/output pin.
			O	-	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
PIO1_10/AD6/ CT16B1_MAT1	20[5]	no	I/O	I;PU	**PIO1_10 —** General purpose digital input/output pin.
			I	-	**AD6 —** A/D converter, input 6.
			O	-	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
PIO1_11/AD7	27[5]	no	I/O	I;PU	**PIO1_11 —** General purpose digital input/output pin.
			I	-	**AD7 —** A/D converter, input 7.
PIO2_0					**Port 2 —** Port 2 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 2 pins depends on the function selected through the IOCONFIG register block. Pins PIO2_1 to PIO2_11 are not available.
PIO2_0/$\overline{\text{DTR}}$	1[3]	no	I/O	I;PU	**PIO2_0 —** General purpose digital input/output pin.
			O	-	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for UART.
PIO3_0 to PIO3_5					**Port 3 —** Port 3 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 3 pins depends on the function selected through the IOCONFIG register block. Pins PIO3_0, PIO3_1, PIO3_3 and PIO3_6 to PIO3_11 are not available.
PIO3_2	28[3]	no	I/O	I;PU	**PIO3_2 —** General purpose digital input/output pin.
PIO3_4	13[3]	no	I/O	I;PU	**PIO3_4 —** General purpose digital input/output pin.
PIO3_5	14[3]	no	I/O	I;PU	**PIO3_5 —** General purpose digital input/output pin.
V_{DD}	6; 29	-	I	-	3.3 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	4[6]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	5[6]	-	O	-	Output from the oscillator amplifier.
V_{SS}	33	-	-	-	Thermal pad. Connect to ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to 2.6 V for LPC111x/101/201/301, pins pulled up to full V_{DD} level on LPC111x/002/102/202/302 (V_{DD} = 3.3 V)); IA = inactive, no pull-up/down enabled.

[2] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See Figure 52 for the reset pad configuration.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 51).

[4] I^2C-bus pads compliant with the I^2C-bus specification for I^2C standard mode and I^2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled, and the pin is not 5 V tolerant (see Figure 51).

Table 10. LPC1100XL series: LPC1113/14/15 pin description table (LQFP48 and TFBGA48 package) *…continued*

Symbol	LQFP48	TFBGA48	Start logic input	Type	Reset state [1]	Description
PIO3_2/$\overline{\text{DCD}}$/ CT16B0_MAT2/ SCK1	43[3]	A4[3]	no	I/O	I; PU	**PIO3_2 —** General purpose digital input/output pin.
				I	-	**$\overline{\text{DCD}}$ —** Data Carrier Detect input for UART.
				O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
				I/O	-	**SCK1 —** Serial clock for SPI1.
PIO3_3/$\overline{\text{RI}}$/ CT16B0_CAP0	48[3]	A2[3]	no	I/O	I; PU	**PIO3_3 —** General purpose digital input/output pin.
				I	-	**$\overline{\text{RI}}$ —** Ring Indicator input for UART.
				I	-	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO3_4/ CT16B0_CAP1/RXD	18[3]	H4[3]	no	I/O	I; PU	**PIO3_4 —** General purpose digital input/output pin.
				I	-	**CT16B0_CAP1 —** Capture input 1 for 16-bit timer 0.
				I	-	**RXD —** Receiver input for UART
PIO3_5/ CT16B1_CAP1/TXD	21[3]	G6[3]	no	I/O	I; PU	**PIO3_5 —** General purpose digital input/output pin.
				I	-	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
				O	-	**TXD —** Transmitter output for UART
V_{DD}	8; 44	E2; B4	-	I	-	3.3 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	6[6]	D1[6]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	7[6]	E1[6]	-	O	-	Output from the oscillator amplifier.
V_{SS}	5; 41	D2; B5	-	I	-	Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level (V_{DD} = 3.3 V)); IA = inactive, no pull-up/down enabled.

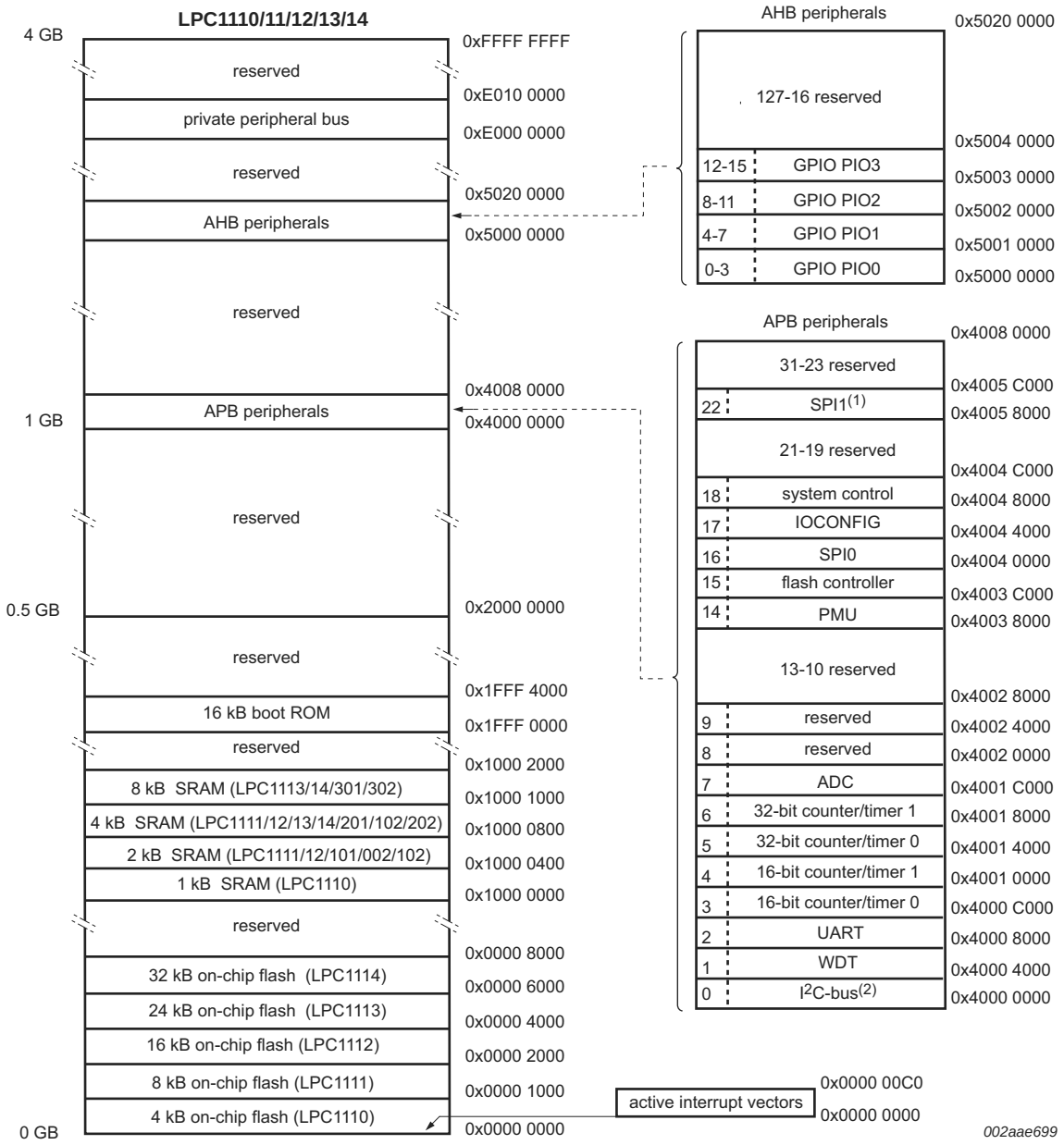
[2] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See Figure 52 for the reset pad configuration.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 51).

[4] I^2C-bus pads compliant with the I^2C-bus specification for I^2C standard mode and I^2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 51).

[6] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.



(1) LQFP48 package only.

(1) Not on part LPC1112FDH20/102.

Fig 14. LPC1100 and LPC1100L series memory map

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_1 for valid user code can be disabled. For details see the *LPC111x user manual*.

7.17.5 APB interface

The APB peripherals are located on one APB bus.

7.17.6 AHBLite

The AHBLite connects the CPU bus of the ARM Cortex-M0 to the flash memory, the main static RAM, and the Boot ROM.

7.17.7 External interrupt inputs

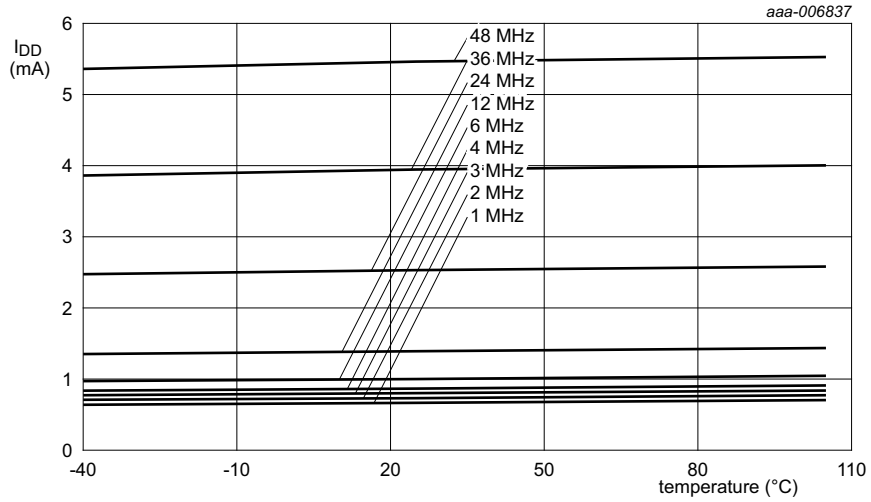
All GPIO pins can be level or edge sensitive interrupt inputs. In addition, start logic inputs serve as external interrupts (see Section 7.17.1).

7.18 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0. Serial wire debug with four breakpoints and two watchpoints is supported.

Table 16. Static characteristics (LPC1100, LPC1100L series) *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled	-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function [12][13][14]	0	-	5.0	V
V_O	output voltage	output active	0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage		0.4	-	-	V
V_{OH}	HIGH-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OH} = −20 mA	V_{DD} − 0.4	-	-	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OH} = −12 mA	V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OL} = 4 mA	-	-	0.4	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OL} = 3 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V; 2.5 V ≤ V_{DD} ≤ 3.6 V	20	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V	12	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 2.5 V ≤ V_{DD} ≤ 3.6 V	4	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V	3	-	-	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD} [15]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V 2.0 V ≤ V_{DD} ≤ 3.6 V	−15	−50	−85	μA
		1.8 V ≤ V_{DD} < 2.0 V	−10	−50	−85	μA
		V_{DD} < V_I < 5 V	0	0	0	μA
I^2C-bus pins (PIO0_4 and PIO0_5)						
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage		-	0.05V_{DD}	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins 2.5 V ≤ V_{DD} ≤ 3.6 V	3.5	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V	3	-	-	



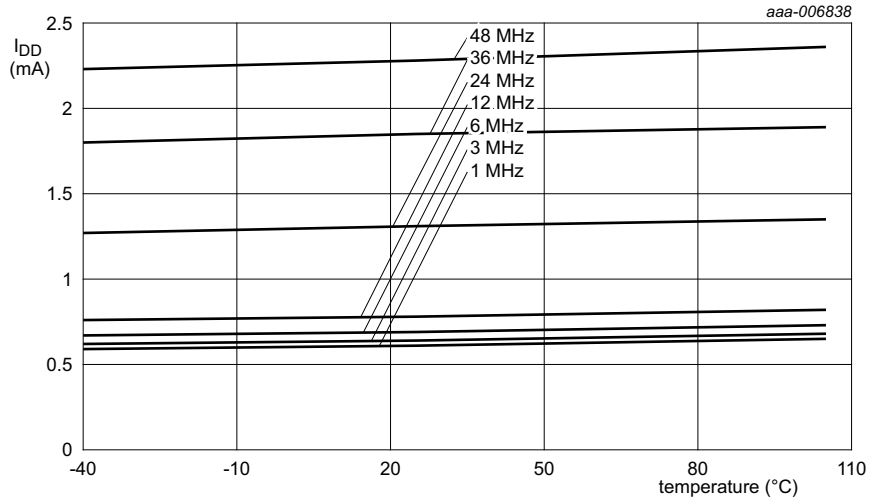
Conditions: V_{DD} = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz to 6 MHz: system oscillator enabled; PLL, IRC disabled.

12 MHz: IRC enabled; system oscillator, PLL disabled.

24 MHz to 48 MHz: IRC disabled; system oscillator, PLL enabled.

Fig 29. Active mode: Typical supply current I_{DD} versus temperature for different system clock frequencies (for LPC111xXL)



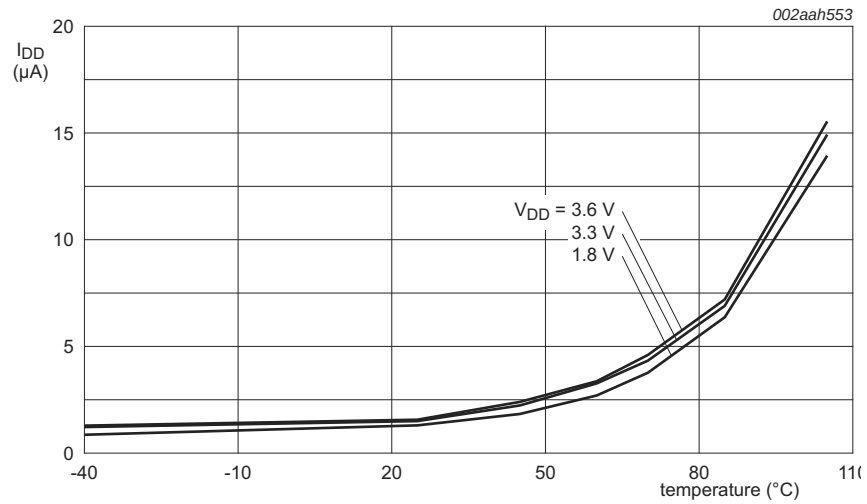
Conditions: V_{DD} = 3.3 V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz to 6 MHz: system oscillator enabled; PLL, IRC disabled.

12 MHz: IRC enabled; system oscillator, PLL disabled.

24 MHz to 48 MHz: IRC disabled; system oscillator, PLL enabled.

Fig 30. Sleep mode: Typical supply current I_{DD} versus temperature for different system clock frequencies (for LPC111xXL)



Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 31. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD} (for LPC111xXL)

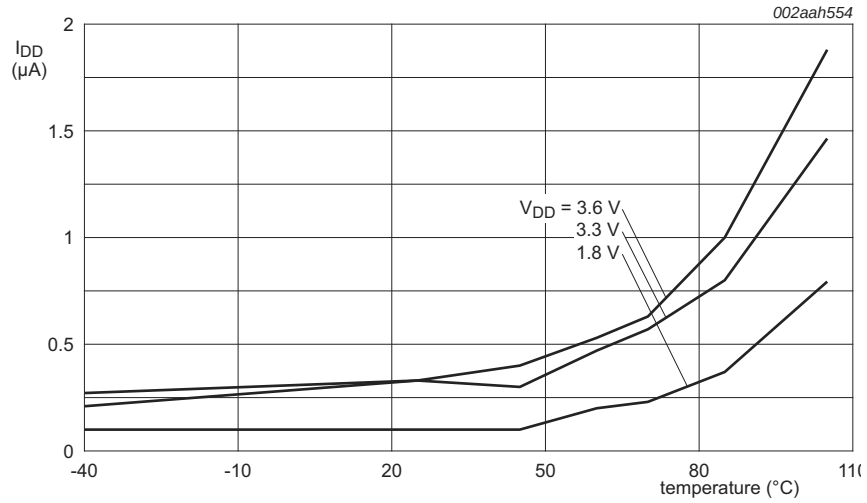


Fig 32. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD} (for LPC111xXL)

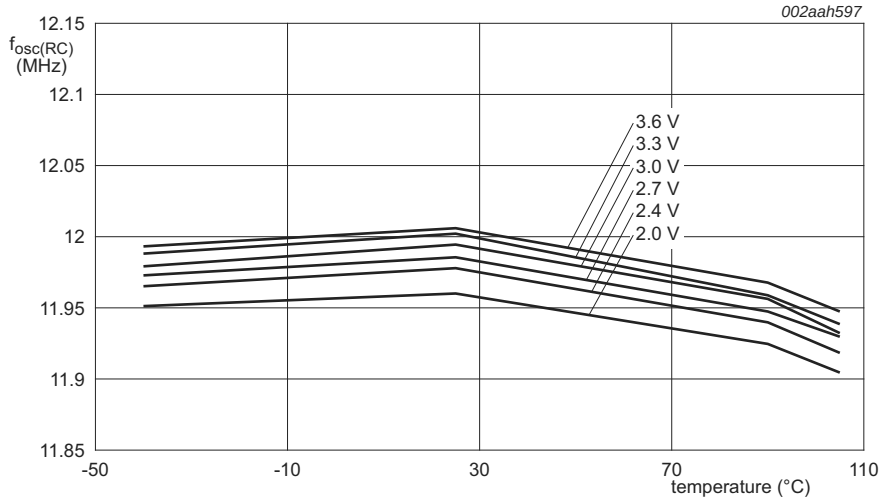
10.9 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at T_{amb} = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 48 MHz.

Table 21. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	48 MHz	
IRC	0.27	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	0.22	-	-	IRC running; PLL off; independent of main clock frequency.
Watchdog oscillator at 500 kHz/2	0.004	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	0.051	-	-	Independent of main clock frequency.
Main PLL	-	0.21	-	
ADC	-	0.08	0.29	
CLKOUT	-	0.12	0.47	Main clock divided by 4 in the CLKOUTDIV register.
CT16B0	-	0.02	0.06	
CT16B1	-	0.02	0.06	
CT32B0	-	0.02	0.07	
CT32B1	-	0.02	0.06	
GPIO	-	0.23	0.88	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
IOCONFIG	-	0.03	0.10	
I2C	-	0.04	0.13	
ROM	-	0.04	0.15	
SPI0	-	0.12	0.45	
SPI1	-	0.12	0.45	
UART	-	0.22	0.82	
WDT/WWDT	-	0.02	0.06	Main clock selected as clock source for the WDT.



Conditions: Frequency values are typical values. 12 MHz ± 1 % accuracy is guaranteed for 2.7 V ≤ V_{DD} ≤ 3.6 V and T_{amb} = −40 °C to +105 °C. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1 % accuracy specification for voltages below 2.7 V.

Fig 45. Internal RC oscillator frequency versus temperature (J parts)

Table 26. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register; [2][3]	-	9.4	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register [2][3]	-	2300	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +105 °C) is ±40 %.

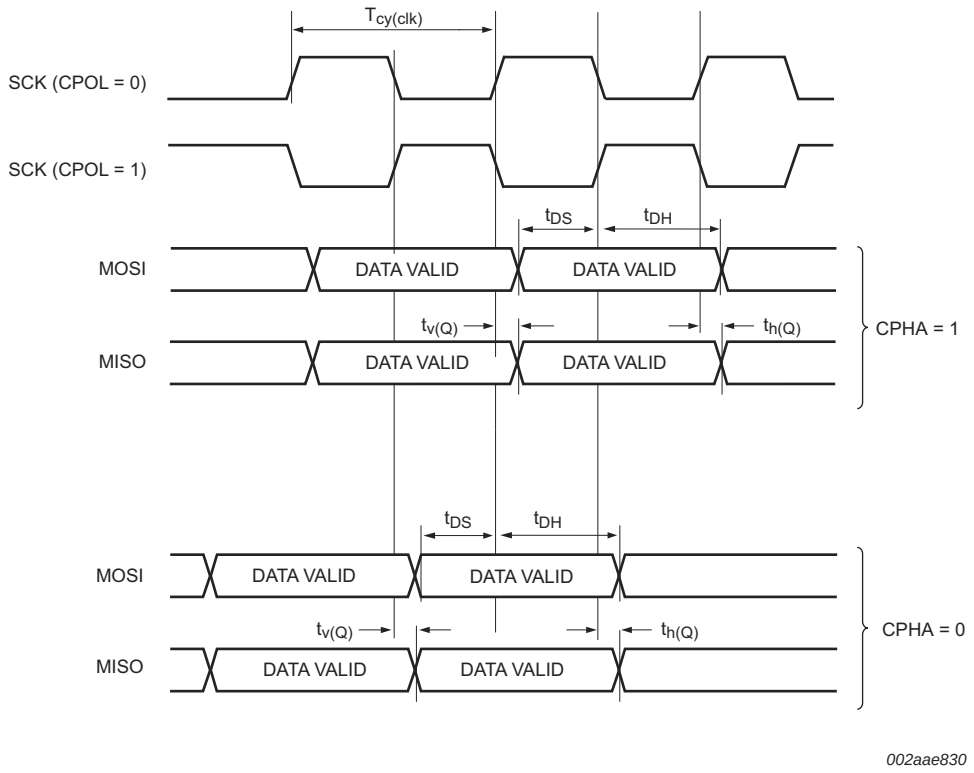
[3] See the LPC111x user manual.

11.5 I/O pins

Table 27. Dynamic characteristic: I/O pins[1]
T_{amb} = −40 °C to +105 °C; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	pin configured as output	3.0	-	5.0	ns
t_f	fall time	pin configured as output	2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.



Pin names SCK, MISO, and MOSI refer to pins for both SPI peripherals, SPI0 and SPI1.

Fig 48. SPI slave timing in SPI mode

12.7 ElectroMagnetic Compatibility (EMC)

Radiated emission measurements according to the IEC61967-2 standard using the TEM-cell method are shown for the LPC1114FBD48/302 in Table 32.

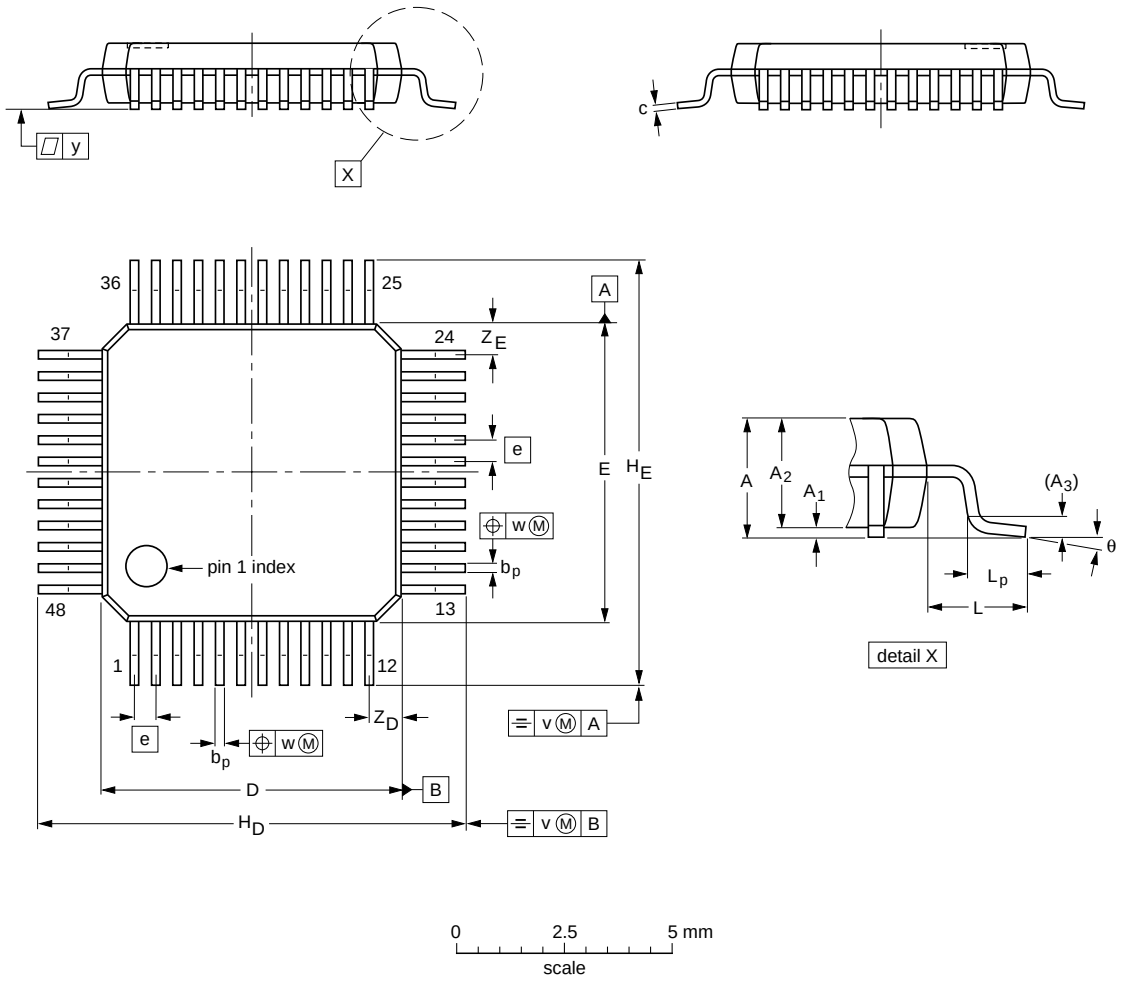
Table 32. ElectroMagnetic Compatibility (EMC) for part LPC1114FBD48/302 (TEM-cell method)

V_{DD} = 3.3 V; T_{amb} = 25 °C.

Parameter	Frequency band	System clock =			Unit
		12 MHz	24 MHz	48 MHz	
Input clock: IRC (12 MHz)					
maximum peak level	150 kHz to 30 MHz	−7	−5	−7	dBμV
	30 MHz to 150 MHz	−2	1	10	dBμV
	150 MHz to 1 GHz	4	8	16	dBμV
IEC level[1]	-	O	N	M	-
Input clock: crystal oscillator (12 MHz)					
maximum peak level	150 kHz to 30 MHz	−7	−7	−7	dBμV
	30 MHz to 150 MHz	−2	1	8	dBμV
	150 MHz to 1 GHz	4	7	14	dBμV
IEC level[1]	-	O	N	M	-

[1] IEC levels refer to Appendix D in the IEC61967-2 Specification.

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

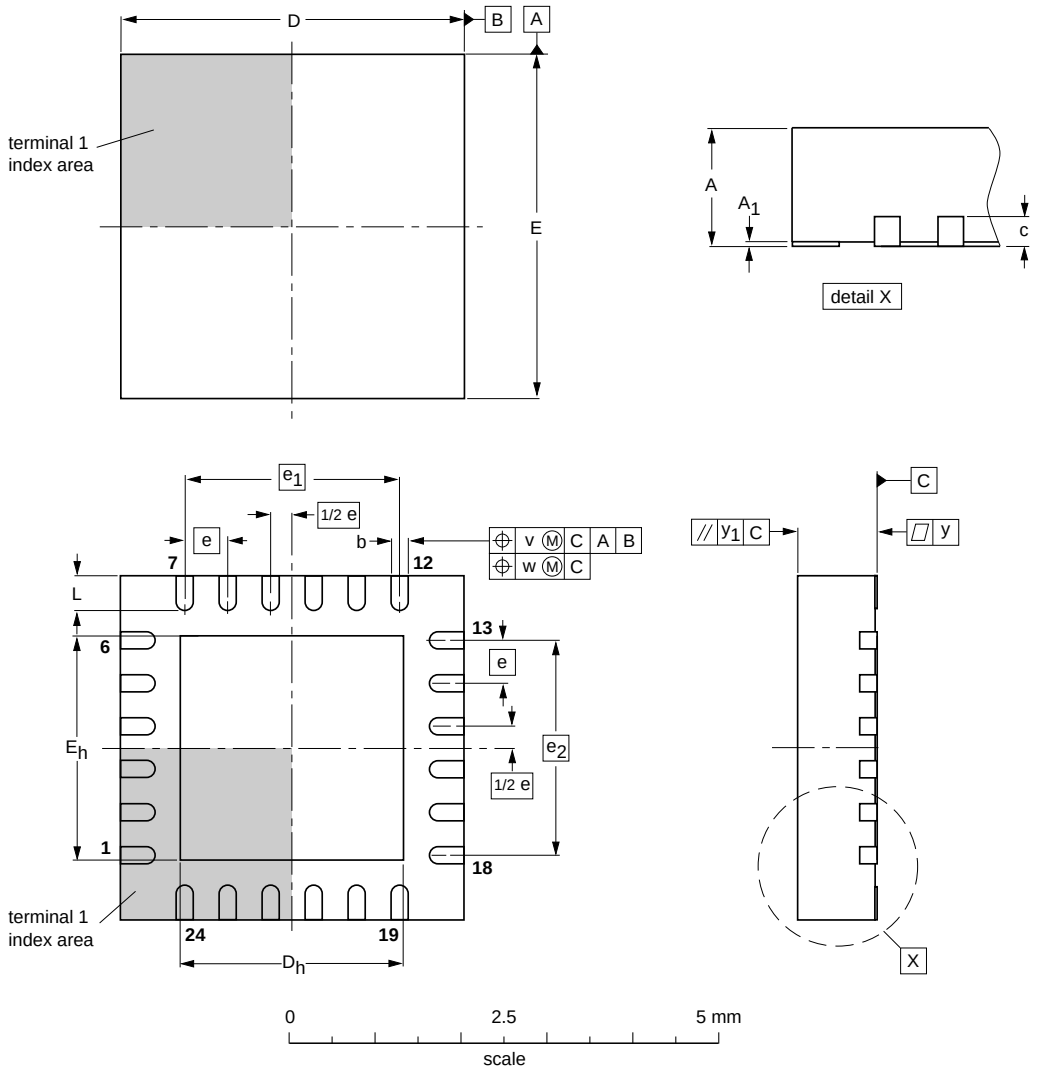
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 60. Package outline SOT313-2 (LQFP48)

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm **SOT616-3**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.75 2.45	4.1 3.9	2.75 2.45	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

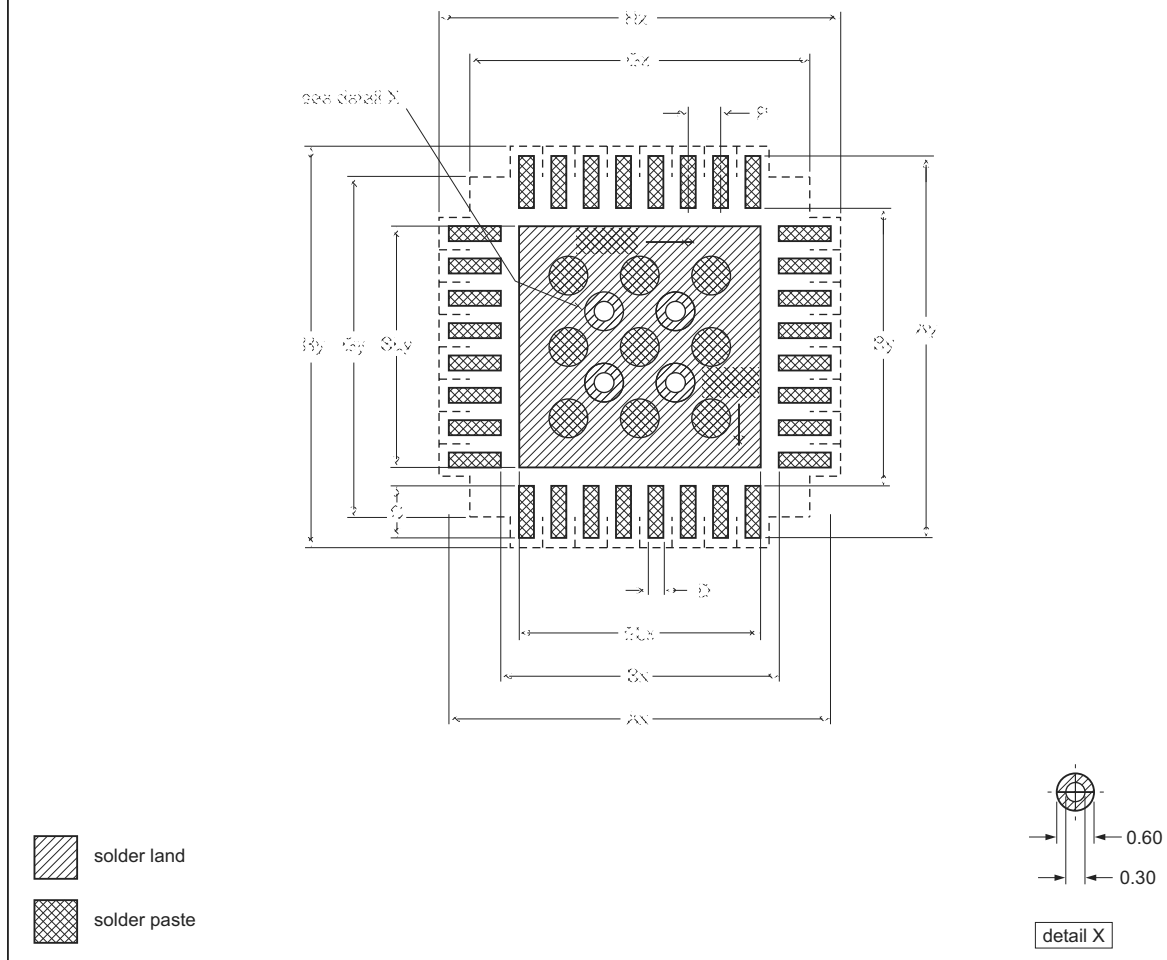
Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT616-3	- - -	MO-220	- - -			~~04-11-19~~ 05-03-10

Fig 61. Package outline SOT616-3 (HVQFN24)

Footprint information for reflow soldering of HVQFN33 package



Dimensions in mm

P	Ax	Ay	Bx	By	C	D	Gx	Gy	Hx	Hy	SLx	SLy	nSPx	nSPy
0.5	5.95	5.95	4.25	4.25	0.85	0.27	5.25	5.25	6.2	6.2	3.75	3.75	3	3

Issue date ~~11-11-15~~ 11-11-20

Fig 67. Reflow soldering of the HVQFN33 package (5x5)

Table 34. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	• Power consumption graphs added for parts LPC111x/102/202/302 (Figure 13 to Figure 17). • Parameter V_{hys} for I^2C bus pins: typical value corrected $V_{hys} = 0.05V_{DD}$ in Table 7. • Typical value for parameter N_{endu} added in Table 12 “Flash characteristics”. • I^2C-bus pins configured as standard mode pins, parameter I_{OL} changed to 3.5 mA (minimum) for $2.0\ V \leq V_{DD} \leq 3.6\ V$. • Section 11.6 “ElectroMagnetic Compatibility (EMC)” added. • Power-up characterization added (Section 10.1 “Power-up ramp conditions”).			
LPC1111_12_13_14 v.3	20101110	Product data sheet	-	LPC1111_12_13_14 v.2
Modifications:	• Parts LPC111x/102/202/302 added (LPC1100L series). • Power consumption data for parts LPC111x/102/202/302 added in Table 7. • PLL output frequency limited to 100 MHz in Section 7.15.2. • Description of $\overline{\text{RESET}}$ and WAKEUP functions updated in Section 6. • WDT description updated in Section 7.14. The WDT is a 24-bit timer. • Power profiles added to Section 2 and Section 7 for parts LPC111x/102/202/302.			
LPC1111_12_13_14 v.2	20100818	Product data sheet	-	LPC1111_12_13_14 v.1
Modifications:	• V_{ESD} limit changed to −6500 V (min) /+6500 V (max) in Table 6. • t_{DS} updated for SPI in master mode (Table 17). • Deep-sleep mode functionality changed to allow BOD and watchdog oscillator as the only analog blocks allowed to remain running in Deep-sleep mode (Section 7.15.5.3). • V_{DD} range changed to $3.0\ V \leq V_{DD} \leq 3.6\ V$ in Table 15. • Reset state of pins and start logic functionality added in Table 3 to Table 5. • Section 7.16.1 added. • Section “Memory mapping control” removed. • V_{OH} and I_{OH} specifications updated for high-drive pins in Table 7. • Section 9.4 added.			
LPC1111_12_13_14 v.1	20100416	Product data sheet	-	-

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