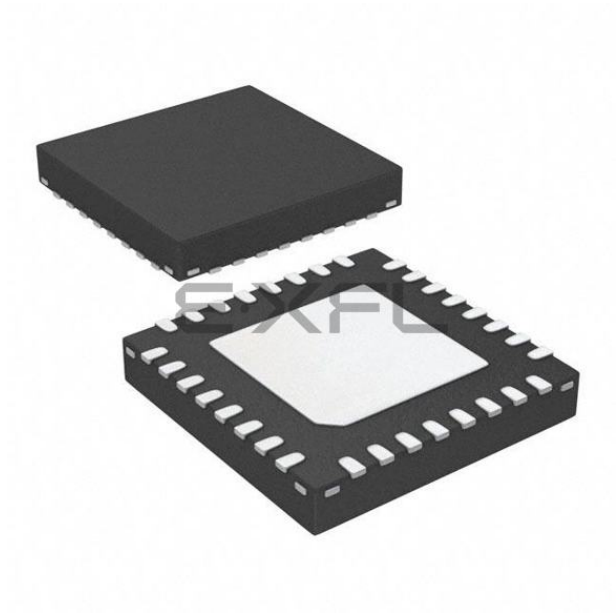

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Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	28
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VQFN Exposed Pad
Supplier Device Package	32-HVQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1112fhn33-103-5

6. Pinning information

6.1 Pinning

Table 3. Pin description overview

Part	Pin description table	Pinning diagram
LPC1110FD20	Table 4	Figure 8
LPC1111FDH20/002	Table 4	Figure 9
LPC1112FD20/102	Table 4	Figure 10
LPC1112FDH20/102	Table 5	Figure 9
LPC1112FHN24/202	Table 6	Figure 11
LPC1112FDH28/102	Table 7	Figure 12
LPC1114FDH28/102	Table 7	Figure 13
LPC1114FN28/102	Table 7	Figure 13
LPC1111FHN33/101	Table 9	Figure 6
LPC1111FHN33/102	Table 9	Figure 6
LPC1111JHN33/103	Table 11	Figure 7
LPC1111FHN33/103	Table 11	Figure 7
LPC1111FHN33/201	Table 9	Figure 6
LPC1111FHN33/202	Table 9	Figure 6
LPC1111FHN33/203	Table 11	Figure 7
LPC1111JHN33/203	Table 11	Figure 7
LPC1112FHN33/101	Table 9	Figure 6
LPC1112FHN33/102	Table 9	Figure 6
LPC1112FHN33/103	Table 11	Figure 7
LPC1112JHN33/103	Table 11	Figure 7
LPC1112FHN33/201	Table 9	Figure 6
LPC1112FHN33/202	Table 9	Figure 6
LPC1112FHN33/203	Table 11	Figure 7
LPC1112JHN33/203	Table 11	Figure 7
LPC1112FHI33/202	Table 9	Figure 6
LPC1112FHI33/203	Table 11	Figure 7
LPC1112JHI33/203	Table 11	Figure 7
LPC1113FHN33/201	Table 9	Figure 6
LPC1113FHN33/202	Table 9	Figure 6
LPC1113FHN33/203	Table 11	Figure 7
LPC1113JHN33/203	Table 11	Figure 7
LPC1113FHN33/301	Table 9	Figure 6
LPC1113FHN33/302	Table 9	Figure 6
LPC1113FHN33/303	Table 11	Figure 7
LPC1113JHN33/303	Table 11	Figure 7
LPC1114FHN33/201	Table 9	Figure 6
LPC1114FHN33/202	Table 9	Figure 6

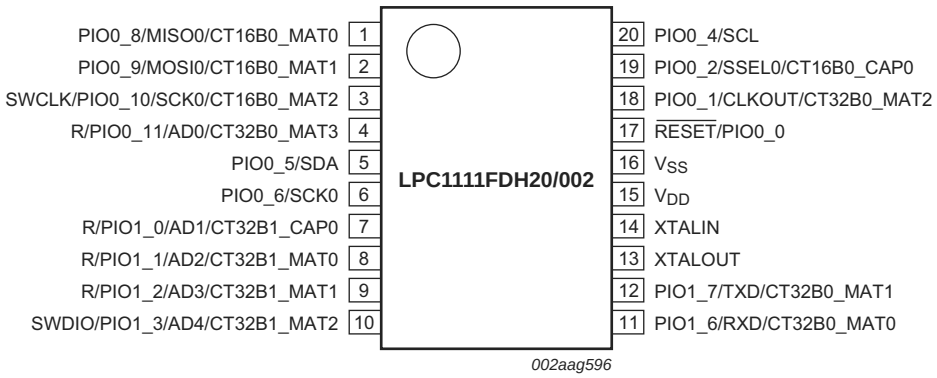


Fig 9. LPC1100L series pin configuration TSSOP20 package with I²C-bus pins

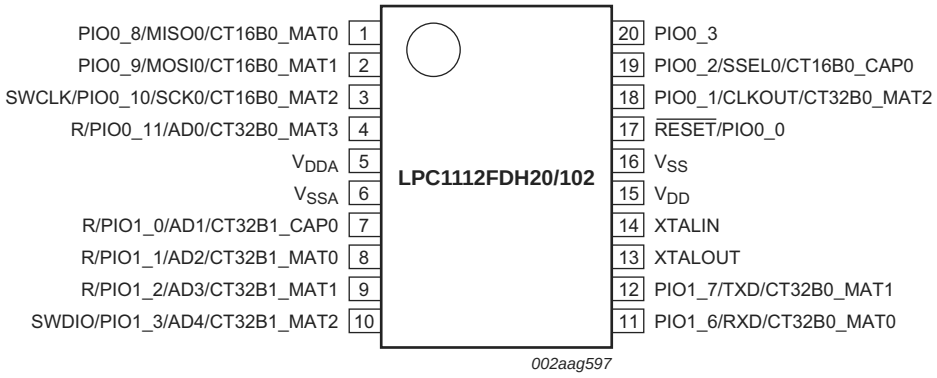


Fig 10. LPC1100L series pin configuration TSSOP20 package with V_{DDA} and V_{SSA} pins

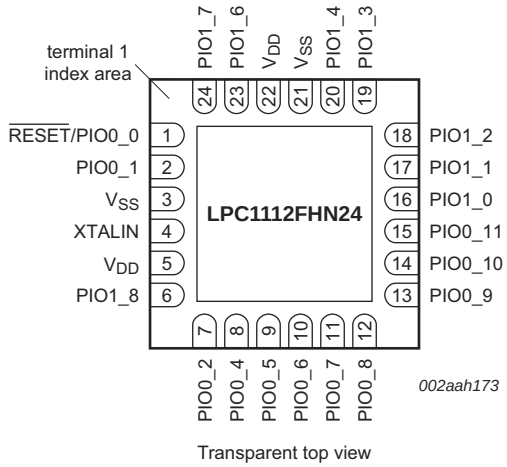


Fig 11. LPC1100L series pin configuration HVQFN24 package

Table 7. LPC1100L series: LPC1112/14 pin description table (TSSOP28 and DIP28 packages)

Symbol	Pin TSSOP28/ DIP28	Start logic input	Type	Reset state [1]	Description
PIO0_0 to PIO0_11			I/O		**Port 0 —** Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.
$\overline{\text{RESET}}$/PIO0_0	23 [2]	yes	I	I; PU	**$\overline{\text{RESET}}$ —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO pin if an external $\overline{\text{RESET}}$ function is not needed and Deep power-down mode is not used.
			I/O	-	**PIO0_0 —** General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/ CT32B0_MAT2	24 [3]	yes	I/O	I; PU	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
			O	-	**CLKOUT —** Clockout pin.
			O	-	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	25 [3]	yes	I/O	I; PU	**PIO0_2 —** General purpose digital input/output pin.
			I/O	-	**SSEL0 —** Slave Select for SPI0.
			I	-	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO0_3	26 [3]	yes	I/O	I; PU	**PIO0_3 —** General purpose digital input/output pin.
PIO0_4/SCL	27 [4]	yes	I/O	I; IA	**PIO0_4 —** General purpose digital input/output pin (open-drain).
			I/O	-	**SCL —** I^2C-bus, open-drain clock input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	5 [4]	yes	I/O	I; IA	**PIO0_5 —** General purpose digital input/output pin (open-drain).
			I/O	-	**SDA —** I^2C-bus, open-drain data input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	6 [3]	yes	I/O	I; PU	**PIO0_6 —** General purpose digital input/output pin.
			I/O	-	**SCK0 —** Serial clock for SPI0.
PIO0_7/$\overline{\text{CTS}}$	28 [3]	yes	I/O	I; PU	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
			I	-	**$\overline{\text{CTS}}$ —** Clear To Send input for UART.
PIO0_8/MISO0/ CT16B0_MAT0	1 [3]	yes	I/O	I; PU	**PIO0_8 —** General purpose digital input/output pin.
			I/O	-	**MISO0 —** Master In Slave Out for SPI0.
			O	-	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	2 [3]	yes	I/O	I; PU	**PIO0_9 —** General purpose digital input/output pin.
			I/O	-	**MOSI0 —** Master Out Slave In for SPI0.
			O	-	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.

Table 8. LPC1100 and LPC1100L series: LPC1113/14 pin description table (LQFP48 package)

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO0_0 to PIO0_11			I/O		**Port 0 —** Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.
$\overline{\text{RESET}}$/PIO0_0	3[2]	yes	I	I; PU	**$\overline{\text{RESET}}$ —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO pin if an external $\overline{\text{RESET}}$ function is not needed and Deep power-down mode is not used.
			I/O	-	**PIO0_0 —** General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/ CT32B0_MAT2	4[3]	yes	I/O	I; PU	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
			O	-	**CLKOUT —** Clockout pin.
			O	-	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	10[3]	yes	I/O	I; PU	**PIO0_2 —** General purpose digital input/output pin.
			I/O	-	**SSEL0 —** Slave Select for SPI0.
			I	-	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO0_3	14[3]	yes	I/O	I; PU	**PIO0_3 —** General purpose digital input/output pin.
PIO0_4/SCL	15[4]	yes	I/O	I; IA	**PIO0_4 —** General purpose digital input/output pin (open-drain).
			I/O	-	**SCL —** I^2C-bus, open-drain clock input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	16[4]	yes	I/O	I; IA	**PIO0_5 —** General purpose digital input/output pin (open-drain).
			I/O	-	**SDA —** I^2C-bus, open-drain data input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	22[3]	yes	I/O	I; PU	**PIO0_6 —** General purpose digital input/output pin.
			I/O	-	**SCK0 —** Serial clock for SPI0.
PIO0_7/$\overline{\text{CTS}}$	23[3]	yes	I/O	I; PU	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
			I	-	**$\overline{\text{CTS}}$ —** Clear To Send input for UART.
PIO0_8/MISO0/ CT16B0_MAT0	27[3]	yes	I/O	I; PU	**PIO0_8 —** General purpose digital input/output pin.
			I/O	-	**MISO0 —** Master In Slave Out for SPI0.
			O	-	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	28[3]	yes	I/O	I; PU	**PIO0_9 —** General purpose digital input/output pin.
			I/O	-	**MOSI0 —** Master Out Slave In for SPI0.
			O	-	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.

Table 9. LPC1100 and LPC1100L series: LPC1111/12/13/14 pin description table (HVQFN33 package)

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO0_0 to PIO0_11					**Port 0 —** Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.
$\overline{\text{RESET}}$/PIO0_0	2[2]	yes	I	I;PU	**$\overline{\text{RESET}}$ —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO pin if an external $\overline{\text{RESET}}$ function is not needed and Deep power-down mode is not used.
			I/O	-	**PIO0_0 —** General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/ CT32B0_MAT2	3[3]	yes	I/O	I;PU	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
			O	-	**CLKOUT —** Clock out pin.
			O	-	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	8[3]	yes	I/O	I;PU	**PIO0_2 —** General purpose digital input/output pin.
			I/O	-	**SSEL0 —** Slave select for SPI0.
			I	-	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO0_3	9[3]	yes	I/O	I;PU	**PIO0_3 —** General purpose digital input/output pin.
PIO0_4/SCL	10[4]	yes	I/O	I;IA	**PIO0_4 —** General purpose digital input/output pin (open-drain).
			I/O	-	**SCL —** I^2C-bus, open-drain clock input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	11[4]	yes	I/O	I;IA	**PIO0_5 —** General purpose digital input/output pin (open-drain).
			I/O	-	**SDA —** I^2C-bus, open-drain data input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	15[3]	yes	I/O	I;PU	**PIO0_6 —** General purpose digital input/output pin.
			I/O	-	**SCK0 —** Serial clock for SPI0.
PIO0_7/$\overline{\text{CTS}}$	16[3]	yes	I/O	I;PU	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
			I	-	**$\overline{\text{CTS}}$ —** Clear To Send input for UART.
PIO0_8/MISO0/ CT16B0_MAT0	17[3]	yes	I/O	I;PU	**PIO0_8 —** General purpose digital input/output pin.
			I/O	-	**MISO0 —** Master In Slave Out for SPI0.
			O	-	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	18[3]	yes	I/O	I;PU	**PIO0_9 —** General purpose digital input/output pin.
			I/O	-	**MOSI0 —** Master Out Slave In for SPI0.
			O	-	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2	19[3]	yes	I	I;PU	**SWCLK —** Serial wire clock.
			I/O	-	**PIO0_10 —** General purpose digital input/output pin.
			I/O	-	**SCK0 —** Serial clock for SPI0.
			O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.

Table 9. LPC1100 and LPC1100L series: LPC1111/12/13/14 pin description table (HVQFN33 package) *…continued*

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
R/PIO0_11/AD0/ CT32B0_MAT3	21[5]	yes	-	I;PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO0_11 —** General purpose digital input/output pin.
			I	-	**AD0 —** A/D converter, input 0.
			O	-	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
PIO1_0 to PIO1_11					**Port 1 —** Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block.
R/PIO1_0/AD1/ CT32B1_CAP0	22[5]	yes	-	I;PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO1_0 —** General purpose digital input/output pin.
			I	-	**AD1 —** A/D converter, input 1.
			I	-	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
R/PIO1_1/AD2/ CT32B1_MAT0	23[5]	no	-	I;PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO1_1 —** General purpose digital input/output pin.
			I	-	**AD2 —** A/D converter, input 2.
			O	-	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
R/PIO1_2/AD3/ CT32B1_MAT1	24[5]	no	-	I;PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO1_2 —** General purpose digital input/output pin.
			I	-	**AD3 —** A/D converter, input 3.
			O	-	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ AD4/CT32B1_MAT2	25[5]	no	I/O	I;PU	**SWDIO —** Serial wire debug input/output.
			I/O	-	**PIO1_3 —** General purpose digital input/output pin.
			I	-	**AD4 —** A/D converter, input 4.
			O	-	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
PIO1_4/AD5/ CT32B1_MAT3/ WAKEUP	26[5]	no	I/O	I;PU	**PIO1_4 —** General purpose digital input/output pin with 10 ns glitch filter. In Deep power-down mode, this pin serves as the Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
			I	-	**AD5 —** A/D converter, input 5.
			O	-	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
PIO1_5/$\overline{\text{RTS}}$/ CT32B0_CAP0	30[3]	no	I/O	I;PU	**PIO1_5 —** General purpose digital input/output pin.
			O	-	**$\overline{\text{RTS}}$ —** Request To Send output for UART.
			I	-	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
PIO1_6/RXD/ CT32B0_MAT0	31[3]	no	I/O	I;PU	**PIO1_6 —** General purpose digital input/output pin.
			I	-	**RXD —** Receiver input for UART.
			O	-	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.

Table 10. LPC1100XL series: LPC1113/14/15 pin description table (LQFP48 and TFBGA48 package) *…continued*

Symbol	LQFP48	TFBGA48	Start logic input	Type	Reset state [1]	Description
PIO3_2/$\overline{\text{DCD}}$/ CT16B0_MAT2/ SCK1	43[3]	A4[3]	no	I/O	I; PU	**PIO3_2 —** General purpose digital input/output pin.
				I	-	**$\overline{\text{DCD}}$ —** Data Carrier Detect input for UART.
				O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
				I/O	-	**SCK1 —** Serial clock for SPI1.
PIO3_3/$\overline{\text{RI}}$/ CT16B0_CAP0	48[3]	A2[3]	no	I/O	I; PU	**PIO3_3 —** General purpose digital input/output pin.
				I	-	**$\overline{\text{RI}}$ —** Ring Indicator input for UART.
				I	-	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO3_4/ CT16B0_CAP1/RXD	18[3]	H4[3]	no	I/O	I; PU	**PIO3_4 —** General purpose digital input/output pin.
				I	-	**CT16B0_CAP1 —** Capture input 1 for 16-bit timer 0.
				I	-	**RXD —** Receiver input for UART
PIO3_5/ CT16B1_CAP1/TXD	21[3]	G6[3]	no	I/O	I; PU	**PIO3_5 —** General purpose digital input/output pin.
				I	-	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
				O	-	**TXD —** Transmitter output for UART
V_{DD}	8; 44	E2; B4	-	I	-	3.3 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	6[6]	D1[6]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	7[6]	E1[6]	-	O	-	Output from the oscillator amplifier.
V_{SS}	5; 41	D2; B5	-	I	-	Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level (V_{DD} = 3.3 V)); IA = inactive, no pull-up/down enabled.

[2] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See Figure 52 for the reset pad configuration.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 51).

[4] I^2C-bus pads compliant with the I^2C-bus specification for I^2C standard mode and I^2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 51).

[6] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

Table 11. LPC1100XL series: LPC1111/12/13/14 pin description table (HVQFN33 package)

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO0_0 to PIO0_11					**Port 0 —** Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.
$\overline{\text{RESET}}$/PIO0_0	2[2]	yes	I	I;PU	**$\overline{\text{RESET}}$ —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO pin if an external $\overline{\text{RESET}}$ function is not needed and Deep power-down mode is not used.
			I/O	-	**PIO0_0 —** General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/ CT32B0_MAT2	3[3]	yes	I/O	I;PU	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
			O	-	**CLKOUT —** Clock out pin.
			O	-	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	8[3]	yes	I/O	I;PU	**PIO0_2 —** General purpose digital input/output pin.
			I/O	-	**SSEL0 —** Slave select for SPI0.
			I	-	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO0_3	9[3]	yes	I/O	I;PU	**PIO0_3 —** General purpose digital input/output pin.
PIO0_4/SCL	10[4]	yes	I/O	I;IA	**PIO0_4 —** General purpose digital input/output pin (open-drain).
			I/O	-	**SCL —** I^2C-bus, open-drain clock input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	11[4]	yes	I/O	I;IA	**PIO0_5 —** General purpose digital input/output pin (open-drain).
			I/O	-	**SDA —** I^2C-bus, open-drain data input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	15[3]	yes	I/O	I;PU	**PIO0_6 —** General purpose digital input/output pin.
			I/O	-	**SCK0 —** Serial clock for SPI0.
PIO0_7/$\overline{\text{CTS}}$	16[3]	yes	I/O	I;PU	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
			I	-	**$\overline{\text{CTS}}$ —** Clear To Send input for UART.
PIO0_8/MISO0/ CT16B0_MAT0	17[3]	yes	I/O	I;PU	**PIO0_8 —** General purpose digital input/output pin.
			I/O	-	**MISO0 —** Master In Slave Out for SPI0.
			O	-	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	18[3]	yes	I/O	I;PU	**PIO0_9 —** General purpose digital input/output pin.
			I/O	-	**MOSI0 —** Master Out Slave In for SPI0.
			O	-	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2	19[3]	yes	I	I;PU	**SWCLK —** Serial wire clock.
			I/O	-	**PIO0_10 —** General purpose digital input/output pin.
			I/O	-	**SCK0 —** Serial clock for SPI0.
			O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.

- On the LPC1100L and LPC1100XL series, all GPIO pins (except PIO0_4 and PIO0_5) are pulled up to 3.3 V (V_{DD} = 3.3 V) if their pull-up resistor is enabled in the IOCONFIG block.
- Programmable open-drain mode for series LPC1100L and LPC1100XL.

7.8 UART

The LPC1110/11/12/13/14/15 contain one UART.

Support for RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The UART includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.8.1 Features

- Maximum UART data bit rate of 3.125 MBit/s.
- 16 Byte Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Support for modem control.

7.9 SPI serial I/O controller

The LPC1100 and LPC1100L series contain two SPI controllers on the LQFP48 package and one SPI controller on the HVQFN33/TSSOP28/DIP28/TSSOP20/SO20 packages (SPI0).

The LPC1100XL series contain two SPI controllers.

Both SPI controllers support SSP features.

The SPI controller is capable of operation on a SSP, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SPI supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.9.1 Features

- Maximum SPI speed of 25 Mbit/s (master) or 4.17 Mbit/s (slave) (in SSP mode)
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication

- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the Internal RC oscillator (IRC), the Watchdog oscillator, or the main clock. This gives a wide range of potential timing choices of Watchdog operation under different power reduction conditions. It also provides the ability to run the WDT from an entirely internal source that is not dependent on an external crystal and its associated components and wiring for increased reliability.

7.15 Windowed WatchDog Timer (LPC1100L and LPC1100XL series)

Remark: The windowed watchdog timer is available on the LPC1100L and LPC1100XL series only.

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.15.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the IRC or the dedicated watchdog oscillator (WDO). This gives a wide range of potential timing choices of watchdog operation under different power conditions.

7.16 Clocking and power control

7.16.1 Crystal oscillators

The LPC1110/11/12/13/14/15 include three independent oscillators. These are the system oscillator, the Internal RC oscillator (IRC), and the Watchdog oscillator. Each oscillator can be used for more than one purpose as required in a particular application.

Table 15. LPC111x/x02 Thermal resistance value (C/W): ±15 %

HVQFN33		**LQFP48**	
θ**ja**		θ**ja**	
JEDEC (4.5 in × 4 in)		**JEDEC (4.5 in × 4 in)**	
0 m/s	40.8	0 m/s	83.3
1 m/s	33.1	1 m/s	74.9
2.5 m/s	28.7	2.5 m/s	69.4
Single-layer (4.5 in × 3 in)		**8-layer (4.5 in × 3 in)**	
0 m/s	85.2	0 m/s	116.3
1 m/s	62	1 m/s	96
2.5 m/s	53.5	2.5 m/s	87.5
θjc	17.9	θjc	28.3
θjb	1.5	θjb	35.5

10.3 ADC static characteristics

Table 18. ADC static characteristics

T_{amb} = −40 °C to +105 °C unless otherwise specified; ADC frequency 4.5 MHz, V_{DD} = 2.5 V to 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		0	-	V_{DD}	V
C_{ia}	analog input capacitance		-	-	1	pF
E_D	differential linearity error	[1][2]	-	-	± 1	LSB
$E_{L(adj)}$	integral non-linearity	[3]	-	-	± 1.5	LSB
E_O	offset error	[4]	-	-	± 3.5	LSB
E_G	gain error	[5]	-	-	0.6	%
E_T	absolute error	[6]	-	-	± 4	LSB
R_{vsi}	voltage source interface resistance		-	-	40	kΩ
R_i	input resistance	[7][8]	-	-	2.5	MΩ

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 17.

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 17.

[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 17.

[5] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 17.

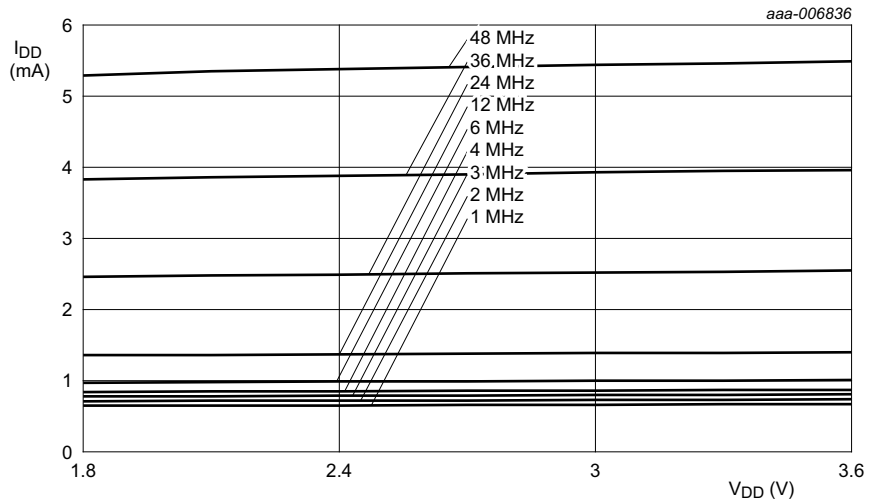
[6] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 17.

[7] T_{amb} = 25 °C; maximum sampling frequency f_s = 400 kSamples/s and analog input capacitance C_{ia} = 1 pF.

[8] Input resistance R_i depends on the sampling frequency f_s: $R_i = 1 / (f_s \times C_{ia})$.

Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see *LPC111x user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCONFIG block.
- Configure GPIO pins as outputs using the GPIOnDIR registers.
- Write 0 to all GPIOnDATA registers to drive the outputs LOW.



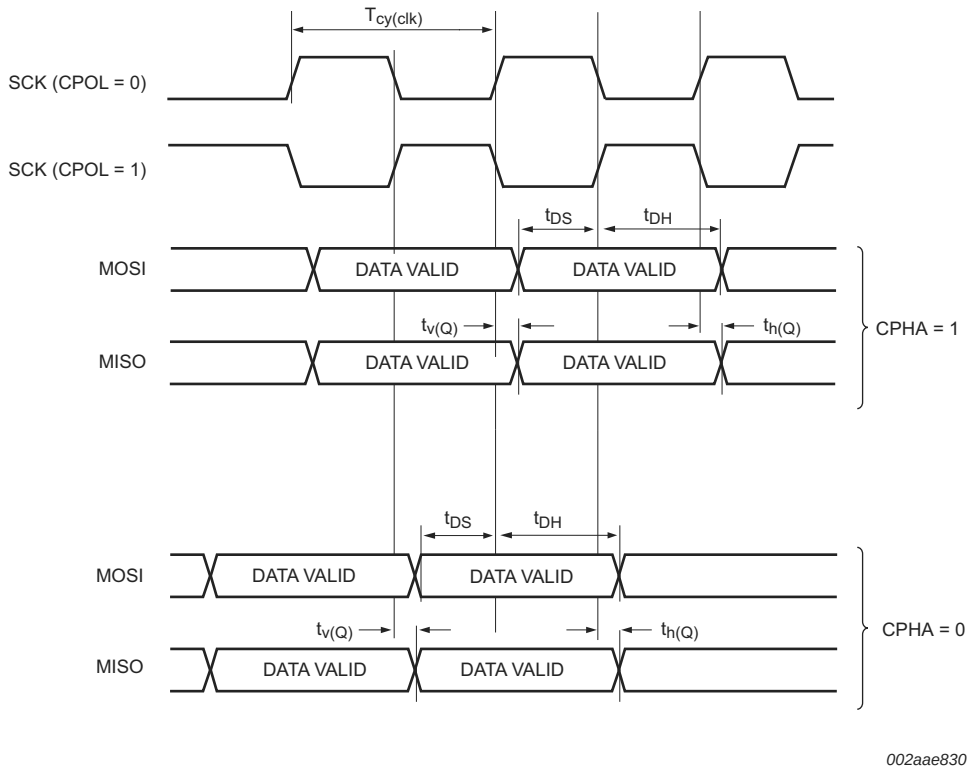
Conditions: T_{amb} = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz to 6 MHz: system oscillator enabled; PLL, IRC disabled.

12 MHz: IRC enabled; system oscillator, PLL disabled.

24 MHz to 48 MHz: IRC disabled; system oscillator, PLL enabled.

Fig 28. Active mode: Typical supply current I_{DD} versus supply voltage V_{DD} for different system clock frequencies (for LPC111xXL)



Pin names SCK, MISO, and MOSI refer to pins for both SPI peripherals, SPI0 and SPI1.

Fig 48. SPI slave timing in SPI mode

12. Application information

12.1 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 18:

- The ADC input trace must be short and as close as possible to the LPC1110/11/12/13/14/15 chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- Because the ADC and the digital core share the same power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

12.2 Use of ADC input trigger signals

For applications that use trigger signals to start conversions and require a precise sample frequency, ensure that the period of the trigger signal is an integral multiple of the period of the ADC clock.

12.3 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV (RMS) is needed.

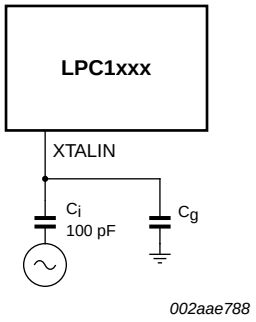


Fig 49. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 49), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 50 and in Table 30 and Table 31. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of

12.8 ADC effective input impedance

A simplified diagram of the ADC input channels can be used to determine the effective input impedance seen from an external voltage source. See Figure 53.

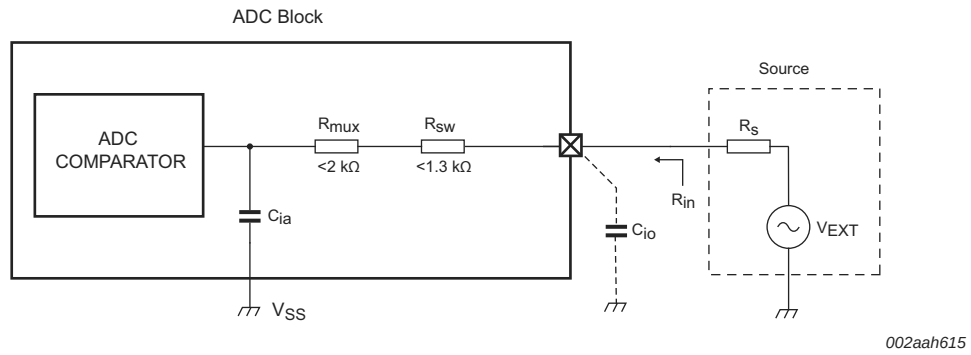


Fig 53. ADC input channel

The effective input impedance, R_{in}, seen by the external voltage source, V_{EXT}, is the parallel impedance of $((1/f_s \times C_{ia}) + R_{mux} + R_{sw})$ and $(1/f_s \times C_{io})$, and can be calculated using Equation 2 with

f_s = sampling frequency

C_{ia} = ADC analog input capacitance

R_{mux} = analog mux resistance

R_{sw} = switch resistance

C_{io} = pin capacitance

$$R_{in} = \left(\frac{1}{f_s \times C_{ia}} + R_{mux} + R_{sw}\right) \| \left(\frac{1}{f_s \times C_{io}}\right) \quad (2)$$

Under nominal operating condition V_{DD} = 3.3 V and with the maximum sampling frequency fs = 400 kHz, the parameters assume the following values:

C_{ia} = 1 pF (max)

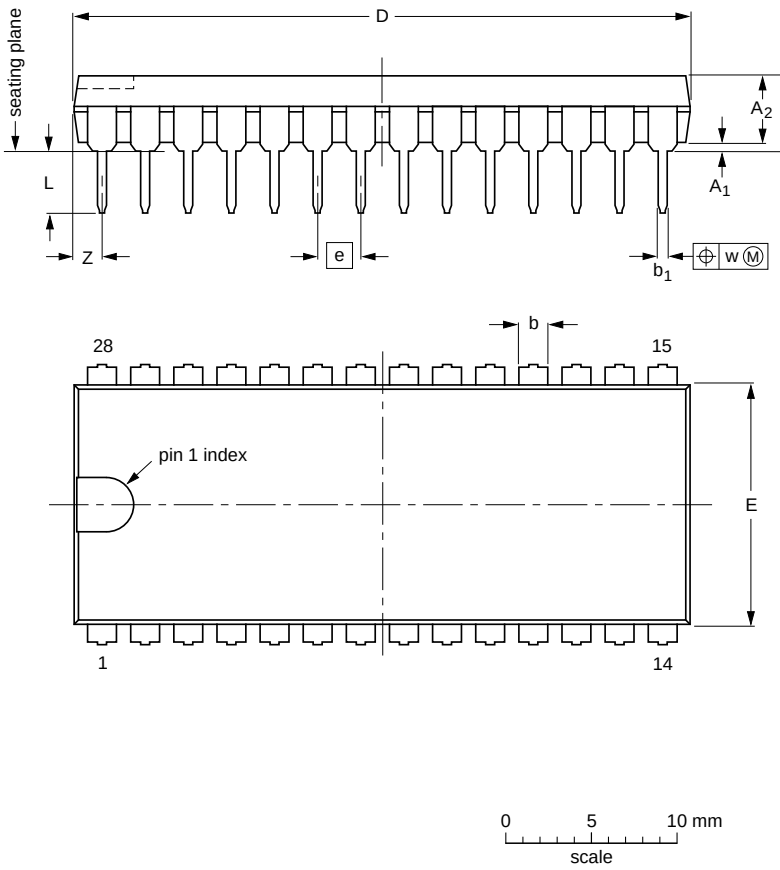
R_{mux} = 2 kΩ (max)

R_{sw} = 1.3 kΩ (max)

C_{io} = 7.1 pF (max)

The effective input impedance with these parameters is R_{in} = 308 kΩ.

DIP28: plastic dual in-line package; 28 leads (600 mil) **SOT117-1**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4	1.7 1.3	0.53 0.38	0.32 0.23	36 35	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.2	0.02	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.1	0.6	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

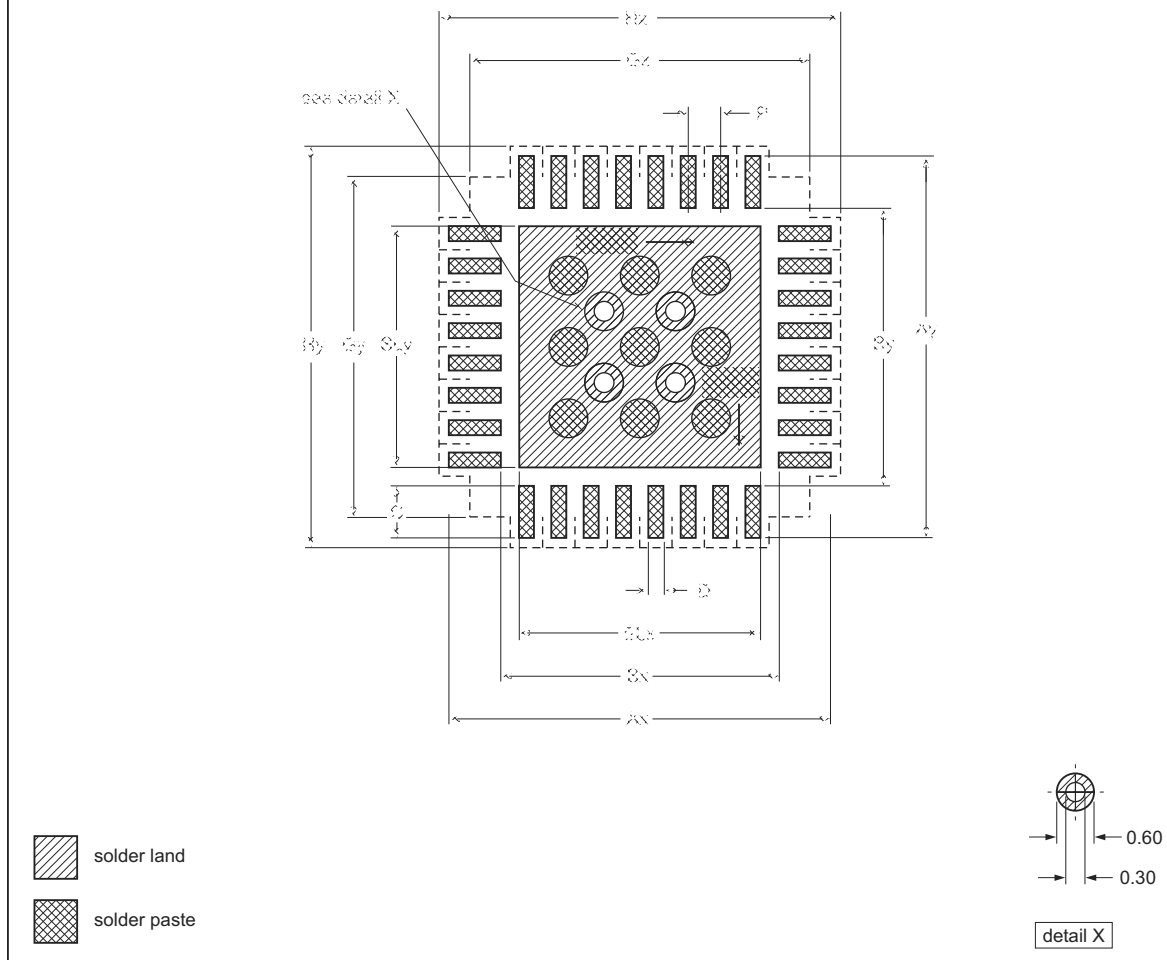
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT117-1	051G05	MO-015	SC-510-28			~~99-12-27~~ 03-02-13

Fig 57. Package outline SOT117-1 (DIP28)

Footprint information for reflow soldering of HVQFN33 package



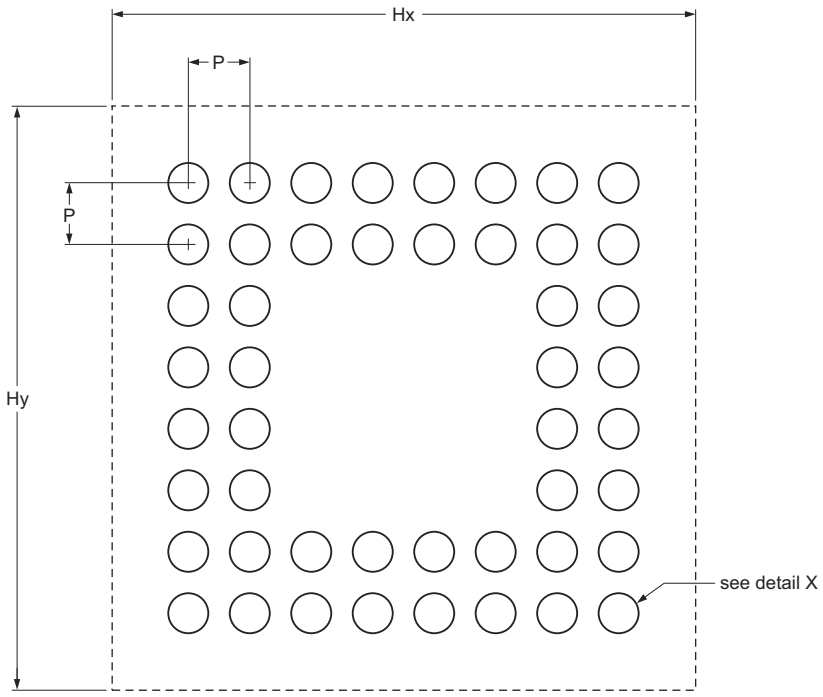
Dimensions in mm

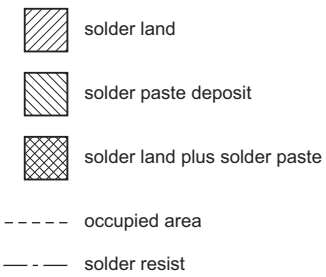
P	Ax	Ay	Bx	By	C	D	Gx	Gy	Hx	Hy	SLx	SLy	nSPx	nSPy
0.5	5.95	5.95	4.25	4.25	0.85	0.27	5.25	5.25	6.2	6.2	3.75	3.75	3	3

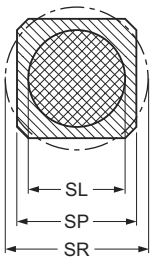
Issue date ~~11-11-15~~ 11-11-20

Fig 67. Reflow soldering of the HVQFN33 package (5x5)

Footprint information for reflow soldering of TFBGA48 package **SOT1155-2**







detail X

DIMENSIONS in mm

P	SL	SP	SR	Hx	Hy
0.50	0.225	0.275	0.325	4.75	4.75

sot1155-2_fr

Fig 70. Reflow soldering for the TFBGA48 package

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