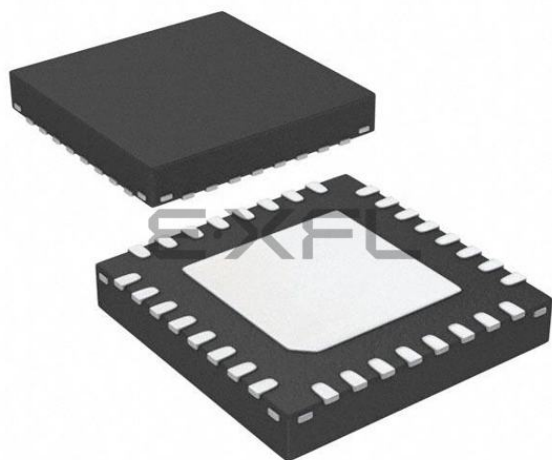




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Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	28
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VQFN Exposed Pad
Supplier Device Package	32-HVQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1112fhn33-201-5

- Digital peripherals:
 - ◆ Up to 42 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors. In addition, a configurable open-drain mode is supported on the LPC1100L and LPC1100XL series.
 - ◆ GPIO pins can be used as edge and level sensitive interrupt sources.
 - ◆ High-current output driver (20 mA) on one pin.
 - ◆ High-current sink drivers (20 mA) on two I²C-bus pins in Fast-mode Plus (not on LPC1112FDH20/102).
 - ◆ Four general purpose counter/timers with up to eight capture inputs and up to 13 match outputs.
 - ◆ Programmable WatchDog Timer (WDT) the LPC1100 series only.
 - ◆ Programmable windowed WDT on the LPC1100L and LPC1100XL series only.
- Analog peripherals:
 - ◆ 10-bit ADC with input multiplexing among 5, 6, or 8 pins depending on package size.
- Serial interfaces:
 - ◆ UART with fractional baud rate generation, internal FIFO, and RS-485 support.
 - ◆ Two SPI controllers with SSP features and with FIFO and multi-protocol capabilities (second SPI on LPC1100 and LPC1100L series LQFP48 package only).
 - ◆ I²C-bus interface supporting full I²C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode (not on LPC1112FDH20/102).
- Clock generation:
 - ◆ 12 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as a system clock.
 - ◆ Crystal oscillator with an operating range of 1 MHz to 25 MHz.
 - ◆ Programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.
 - ◆ PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator or the internal RC oscillator.
 - ◆ Clock output function with divider that can reflect the system oscillator clock, IRC clock, CPU clock, and the Watchdog clock.
- Power control:
 - ◆ Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, and Deep power-down modes.
 - ◆ Power profiles residing in boot ROM allowing to optimize performance and minimize power consumption for any given application through one simple function call. (LPC1100L and LPC1100XL series only.)
 - ◆ Three reduced power modes: Sleep, Deep-sleep, and Deep power-down.
 - ◆ Processor wake-up from Deep-sleep mode via a dedicated start logic using up to 13 of the functional pins.
 - ◆ Power-On Reset (POR).
 - ◆ Brownout detect with up to four separate thresholds for interrupt and forced reset.
- Unique device serial number for identification.
- Single power supply (1.8 V to 3.6 V).
- Available as LQFP48 package, HVQFN33 package, and TFBGA48 package.

Table 7. LPC1100L series: LPC1112/14 pin description table (TSSOP28 and DIP28 packages) ...continued

Symbol	Pin TSSOP28/ DIP28	Start logic input	Type	Reset state [1]	Description
SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2	3 [3]	yes	I	I; PU	SWCLK — Serial wire clock.
			I/O	-	PIO0_10 — General purpose digital input/output pin.
			I/O	-	SCK0 — Serial clock for SPI0.
			O	-	CT16B0_MAT2 — Match output 2 for 16-bit timer 0.
R/PIO0_11/ AD0/CT32B0_MAT3	4 [5]	yes	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO0_11 — General purpose digital input/output pin.
			I	-	AD0 — A/D converter, input 0.
			O	-	CT32B0_MAT3 — Match output 3 for 32-bit timer 0.
PIO1_0 to PIO1_9			I/O		Port 1 — Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block.
R/PIO1_0/ AD1/CT32B1_CAP0	9 [5]	yes	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_0 — General purpose digital input/output pin.
			I	-	AD1 — A/D converter, input 1.
			I	-	CT32B1_CAP0 — Capture input 0 for 32-bit timer 1.
R/PIO1_1/ AD2/CT32B1_MAT0	10 [5]	no	O	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_1 — General purpose digital input/output pin.
			I	-	AD2 — A/D converter, input 2.
			O	-	CT32B1_MAT0 — Match output 0 for 32-bit timer 1.
R/PIO1_2/ AD3/CT32B1_MAT1	11 [5]	no	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_2 — General purpose digital input/output pin.
			I	-	AD3 — A/D converter, input 3.
			O	-	CT32B1_MAT1 — Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ AD4/CT32B1_MAT2	12 [5]	no	I/O	I; PU	SWDIO — Serial wire debug input/output.
			I/O	-	PIO1_3 — General purpose digital input/output pin.
			I	-	AD4 — A/D converter, input 4.
			O	-	CT32B1_MAT2 — Match output 2 for 32-bit timer 1.
PIO1_4/AD5/ CT32B1_MAT3/ WAKEUP	13 [5]	no	I/O	I; PU	PIO1_4 — General purpose digital input/output pin with 10 ns glitch filter. In Deep power-down mode, this pin serves as the Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
			I	-	AD5 — A/D converter, input 5.
			O	-	CT32B1_MAT3 — Match output 3 for 32-bit timer 1.

Table 8. LPC1100 and LPC1100L series: LPC1113/14 pin description table (LQFP48 package) ...continued

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2	29 ^[3]	yes	I	I; PU	SWCLK — Serial wire clock.
			I/O	-	PIO0_10 — General purpose digital input/output pin.
			I/O	-	SCK0 — Serial clock for SPI0.
			O	-	CT16B0_MAT2 — Match output 2 for 16-bit timer 0.
R/PIO0_11/ AD0/CT32B0_MAT3	32 ^[5]	yes	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO0_11 — General purpose digital input/output pin.
			I	-	AD0 — A/D converter, input 0.
			O	-	CT32B0_MAT3 — Match output 3 for 32-bit timer 0.
PIO1_0 to PIO1_11			I/O		Port 1 — Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block.
R/PIO1_0/ AD1/CT32B1_CAP0	33 ^[5]	yes	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_0 — General purpose digital input/output pin.
			I	-	AD1 — A/D converter, input 1.
			I	-	CT32B1_CAP0 — Capture input 0 for 32-bit timer 1.
R/PIO1_1/ AD2/CT32B1_MAT0	34 ^[5]	no	O	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_1 — General purpose digital input/output pin.
			I	-	AD2 — A/D converter, input 2.
			O	-	CT32B1_MAT0 — Match output 0 for 32-bit timer 1.
R/PIO1_2/ AD3/CT32B1_MAT1	35 ^[5]	no	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_2 — General purpose digital input/output pin.
			I	-	AD3 — A/D converter, input 3.
			O	-	CT32B1_MAT1 — Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ AD4/CT32B1_MAT2	39 ^[5]	no	I/O	I; PU	SWDIO — Serial wire debug input/output.
			I/O	-	PIO1_3 — General purpose digital input/output pin.
			I	-	AD4 — A/D converter, input 4.
			O	-	CT32B1_MAT2 — Match output 2 for 32-bit timer 1.
PIO1_4/AD5/ CT32B1_MAT3/ WAKEUP	40 ^[5]	no	I/O	I; PU	PIO1_4 — General purpose digital input/output pin with 10 ns glitch filter. In Deep power-down mode, this pin serves as the Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
			I	-	AD5 — A/D converter, input 5.
			O	-	CT32B1_MAT3 — Match output 3 for 32-bit timer 1.
PIO1_5/RTS/ CT32B0_CAP0	45 ^[3]	no	I/O	I; PU	PIO1_5 — General purpose digital input/output pin.
			O	-	RTS — Request To Send output for UART.
			I	-	CT32B0_CAP0 — Capture input 0 for 32-bit timer 0.

Table 9. LPC1100 and LPC1100L series: LPC1111/12/13/14 pin description table (HVQFN33 package) ...continued

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO1_7/TXD/ CT32B0_MAT1	32 ^[3]	no	I/O	I;PU	PIO1_7 — General purpose digital input/output pin.
			O	-	TXD — Transmitter output for UART.
			O	-	CT32B0_MAT1 — Match output 1 for 32-bit timer 0.
PIO1_8/ CT16B1_CAP0	7 ^[3]	no	I/O	I;PU	PIO1_8 — General purpose digital input/output pin.
			I	-	CT16B1_CAP0 — Capture input 0 for 16-bit timer 1.
PIO1_9/ CT16B1_MAT0	12 ^[3]	no	I/O	I;PU	PIO1_9 — General purpose digital input/output pin.
			O	-	CT16B1_MAT0 — Match output 0 for 16-bit timer 1.
PIO1_10/AD6/ CT16B1_MAT1	20 ^[5]	no	I/O	I;PU	PIO1_10 — General purpose digital input/output pin.
			I	-	AD6 — A/D converter, input 6.
			O	-	CT16B1_MAT1 — Match output 1 for 16-bit timer 1.
PIO1_11/AD7	27 ^[5]	no	I/O	I;PU	PIO1_11 — General purpose digital input/output pin.
			I	-	AD7 — A/D converter, input 7.
PIO2_0					Port 2 — Port 2 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 2 pins depends on the function selected through the IOCONFIG register block. Pins PIO2_1 to PIO2_11 are not available.
PIO2_0/DTR	1 ^[3]	no	I/O	I;PU	PIO2_0 — General purpose digital input/output pin.
			O	-	DTR — Data Terminal Ready output for UART.
PIO3_0 to PIO3_5					Port 3 — Port 3 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 3 pins depends on the function selected through the IOCONFIG register block. Pins PIO3_0, PIO3_1, PIO3_3 and PIO3_6 to PIO3_11 are not available.
PIO3_2	28 ^[3]	no	I/O	I;PU	PIO3_2 — General purpose digital input/output pin.
PIO3_4	13 ^[3]	no	I/O	I;PU	PIO3_4 — General purpose digital input/output pin.
PIO3_5	14 ^[3]	no	I/O	I;PU	PIO3_5 — General purpose digital input/output pin.
V _{DD}	6; 29	-	I	-	3.3 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	4 ^[6]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	5 ^[6]	-	O	-	Output from the oscillator amplifier.
V _{SS}	33	-	-	-	Thermal pad. Connect to ground.

- [1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to 2.6 V for LPC111x/101/201/301, pins pulled up to full V_{DD} level on LPC111x/002/102/202/302 (V_{DD} = 3.3 V)); IA = inactive, no pull-up/down enabled.
- [2] 5 V tolerant pad. **RESET** functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See [Figure 52](#) for the reset pad configuration.
- [3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see [Figure 51](#)).
- [4] I²C-bus pads compliant with the I²C-bus specification for I²C standard mode and I²C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.
- [5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled, and the pin is not 5 V tolerant (see [Figure 51](#)).

Table 10. LPC1100XL series: LPC1113/14/15 pin description table (LQFP48 and TFBGA48 package) ...continued

Symbol	LQFP48	TFBGA48	Start logic input	Type	Reset state [4]	Description
PIO1_4/AD5/ CT32B1_MAT3/ WAKEUP	40 ^[5]	A6 ^[5]	no	I/O	I; PU	PIO1_4 — General purpose digital input/output pin with 10 ns glitch filter. In Deep power-down mode, this pin serves as the Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
				I	-	AD5 — A/D converter, input 5.
				O	-	CT32B1_MAT3 — Match output 3 for 32-bit timer 1.
PIO1_5/RTS/ CT32B0_CAP0	45 ^[3]	A3 ^[3]	no	I/O	I; PU	PIO1_5 — General purpose digital input/output pin.
				O	-	RTS — Request To Send output for UART.
				I	-	CT32B0_CAP0 — Capture input 0 for 32-bit timer 0.
PIO1_6/RXD/ CT32B0_MAT0	46 ^[3]	B3 ^[3]	no	I/O	I; PU	PIO1_6 — General purpose digital input/output pin.
				I	-	RXD — Receiver input for UART.
				O	-	CT32B0_MAT0 — Match output 0 for 32-bit timer 0.
PIO1_7/TXD/ CT32B0_MAT1	47 ^[3]	B2 ^[3]	no	I/O	I; PU	PIO1_7 — General purpose digital input/output pin.
				O	-	TXD — Transmitter output for UART.
				O	-	CT32B0_MAT1 — Match output 1 for 32-bit timer 0.
PIO1_8/ CT16B1_CAP0	9 ^[3]	F2 ^[3]	no	I/O	I; PU	PIO1_8 — General purpose digital input/output pin.
				I	-	CT16B1_CAP0 — Capture input 0 for 16-bit timer 1.
PIO1_9/ CT16B1_MAT0/ MOSI1	17 ^[3]	G4 ^[3]	no	I/O	I; PU	PIO1_9 — General purpose digital input/output pin.
				O	-	CT16B1_MAT0 — Match output 0 for 16-bit timer 1.
				I/O	-	MOSI1 — Master Out Slave In for SPI1.
PIO1_10/AD6/ CT16B1_MAT1/ MISO1	30 ^[5]	E8 ^[5]	no	I/O	I; PU	PIO1_10 — General purpose digital input/output pin.
				I	-	AD6 — A/D converter, input 6.
				O	-	CT16B1_MAT1 — Match output 1 for 16-bit timer 1.
				I/O	-	MISO1 — Master In Slave Out for SPI1.
PIO1_11/AD7/ CT32B1_CAP1	42 ^[5]	A5 ^[5]	no	I/O	I; PU	PIO1_11 — General purpose digital input/output pin.
				I	-	AD7 — A/D converter, input 7.
				I	-	CT32B1_CAP1 — Capture input 1 for 32-bit timer 1.
PIO2_0 to PIO2_11				I/O		Port 2 — Port 2 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 2 pins depends on the function selected through the IOCONFIG register block.
PIO2_0/DTR/SSEL1	2 ^[3]	B1 ^[3]	no	I/O	I; PU	PIO2_0 — General purpose digital input/output pin.
				O	-	DTR — Data Terminal Ready output for UART.
				I/O	-	SSEL1 — Slave Select for SPI1.
PIO2_1/DSR/SCK1	13 ^[3]	H1 ^[3]	no	I/O	I; PU	PIO2_1 — General purpose digital input/output pin.
				I	-	DSR — Data Set Ready input for UART.
				I/O	-	SCK1 — Serial clock for SPI1.

Table 11. LPC1100XL series: LPC1111/12/13/14 pin description table (HVQFN33 package) ...continued

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
R/PIO0_11/AD0/ CT32B0_MAT3	21 ^[5]	yes	-	I;PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO0_11 — General purpose digital input/output pin.
			I	-	AD0 — A/D converter, input 0.
			O	-	CT32B0_MAT3 — Match output 3 for 32-bit timer 0.
PIO1_0 to PIO1_11					Port 1 — Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block.
R/PIO1_0/AD1/ CT32B1_CAP0	22 ^[5]	yes	-	I;PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_0 — General purpose digital input/output pin.
			I	-	AD1 — A/D converter, input 1.
			I	-	CT32B1_CAP0 — Capture input 0 for 32-bit timer 1.
R/PIO1_1/AD2/ CT32B1_MAT0	23 ^[5]	no	-	I;PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_1 — General purpose digital input/output pin.
			I	-	AD2 — A/D converter, input 2.
			O	-	CT32B1_MAT0 — Match output 0 for 32-bit timer 1.
R/PIO1_2/AD3/ CT32B1_MAT1	24 ^[5]	no	-	I;PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_2 — General purpose digital input/output pin.
			I	-	AD3 — A/D converter, input 3.
			O	-	CT32B1_MAT1 — Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ AD4/CT32B1_MAT2	25 ^[5]	no	I/O	I;PU	SWDIO — Serial wire debug input/output.
			I/O	-	PIO1_3 — General purpose digital input/output pin.
			I	-	AD4 — A/D converter, input 4.
			O	-	CT32B1_MAT2 — Match output 2 for 32-bit timer 1.
PIO1_4/AD5/ CT32B1_MAT3/ WAKEUP	26 ^[5]	no	I/O	I;PU	PIO1_4 — General purpose digital input/output pin with 10 ns glitch filter. In Deep power-down mode, this pin serves as the Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
			I	-	AD5 — A/D converter, input 5.
			O	-	CT32B1_MAT3 — Match output 3 for 32-bit timer 1.
PIO1_5/RTS/ CT32B0_CAP0	30 ^[3]	no	I/O	I;PU	PIO1_5 — General purpose digital input/output pin.
			O	-	RTS — Request To Send output for UART.
			I	-	CT32B0_CAP0 — Capture input 0 for 32-bit timer 0.
PIO1_6/RXD/ CT32B0_MAT0	31 ^[3]	no	I/O	I;PU	PIO1_6 — General purpose digital input/output pin.
			I	-	RXD — Receiver input for UART.
			O	-	CT32B0_MAT0 — Match output 0 for 32-bit timer 0.

9. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD} . The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 13. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{j(max)}$	maximum junction temperature		-	-	125	°C

Table 14. LPC111x/x01 Thermal resistance value (°C/W): ±15 %

HVQFN33		LQFP48	
θ_{ja}		θ_{ja}	
JEDEC (4.5 in × 4 in)		JEDEC (4.5 in × 4 in)	
0 m/s	40.4	0 m/s	82.1
1 m/s	32.7	1 m/s	73.7
2.5 m/s	28.3	2.5 m/s	68.2
Single-layer (4.5 in × 3 in)		8-layer (4.5 in × 3 in)	
0 m/s	84.8	0 m/s	115.2
1 m/s	61.6	1 m/s	94.7
2.5 m/s	53.1	2.5 m/s	86.3
θ_{jc}	20.3	θ_{jc}	29.6
θ_{jb}	1.1	θ_{jb}	34.2

Table 16. Static characteristics (LPC1100, LPC1100L series) ...continued $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
I _{OL}	LOW-level output current	V _{OL} = 0.4 V; I ² C-bus pins configured as Fast-mode Plus pins 2.5 V ≤ V _{DD} ≤ 3.6 V	20	-	-	mA
		1.8 V ≤ V _{DD} < 2.5 V	16	-	-	
I _{LI}	input leakage current	V _I = V _{DD} ^[16]	-	2	4	μA
		V _I = 5 V	-	10	22	μA
Oscillator pins						
V _{i(xtal)}	crystal input voltage		−0.5	1.8	1.95	V
V _{o(xtal)}	crystal output voltage		−0.5	1.8	1.95	V
Pin capacitance						
C _{io}	input/output capacitance	pins configured for analog function	-	-	7.1	pF
		I ² C-bus pins (PIO0_4 and PIO0_5)	-	-	2.5	pF
		pins configured as GPIO	-	-	2.8	pF

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] $T_{amb} = 25\text{ }^{\circ}\text{C}$.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] IRC enabled; system oscillator disabled; system PLL disabled.

[5] BOD disabled.

[6] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks to UART and SPI0/1 disabled in system configuration block.

[7] IRC disabled; system oscillator enabled; system PLL enabled.

[8] All oscillators and analog blocks turned off in the PDSLEEPCFG register; PDSLEEPCFG = 0x0000 18FF.

[9] WAKEUP pin and RESET pin are pulled HIGH externally.

[10] System oscillator enabled; IRC disabled; system PLL disabled.

[11] Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.

[12] Including voltage on outputs in 3-state mode.

[13] V_{DD} supply voltage must be present.

[14] 3-state outputs go into 3-state mode in Deep power-down mode.

[15] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[16] To V_{SS} .

10.2 LPC1100XL series

Table 17. Static characteristics (LPC1100XL series)

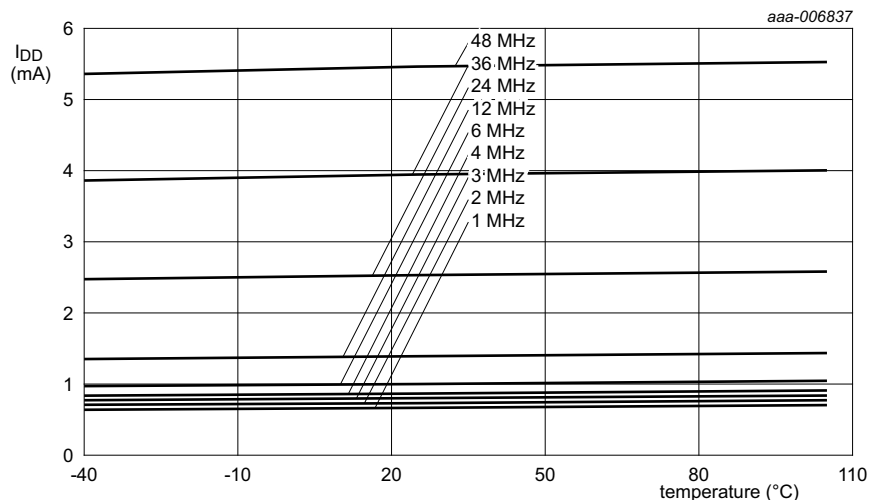
 $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
V _{DD}	supply voltage (core and external rail)		1.8	3.3	3.6	V
LPC1100XL series (LPC111x/103/203/303/323/333) power consumption in low-current mode ^[2]						
I _{DD}	supply current	Active mode; code while(1){} executed from flash				
		system clock = 3 MHz ^{[3][4][5]} V _{DD} = 3.3 V ^{[6][7]}	-	600	-	μA
		system clock = 6 MHz ^{[3][4][5]} V _{DD} = 3.3 V ^{[6][7]}	-	850	-	μA
		system clock = 12 MHz ^{[3][4][6]} V _{DD} = 3.3 V ^{[7][8]}	-	1.4	-	mA
		system clock = 50 MHz ^{[3][4][6]} V _{DD} = 3.3 V ^{[7][9]}	-	5.8	-	mA
		Sleep mode; ^{[3][4][6]} system clock = 12 MHz ^{[7][8]} V _{DD} = 3.3 V	-	700	-	μA
		system clock = 50 MHz ^{[3][4][6]} V _{DD} = 3.3 V ^{[7][8]}	-	2.2	-	mA
		Deep-sleep mode; ^{[3][4]} V _{DD} = 3.3 V; 25 °C ^[10]	-	1.8	15	μA
		Deep-sleep mode; ^{[4][10]} V _{DD} = 3.3 V; 105 °C ^[11]	-	-	50	μA
		Deep power-down mode; ^{[3][12]} V _{DD} = 3.3 V; 25 °C	-	220	1000	nA
		Deep power-down mode; ^{[11][12]} V _{DD} = 3.3 V; 105 °C	-	-	3	μA
Standard port pins, RESET						
I _{IL}	LOW-level input current	V _I = 0 V; on-chip pull-up resistor disabled	-	0.5	10	nA
I _{IH}	HIGH-level input current	V _I = V _{DD} ; on-chip pull-down resistor disabled	-	0.5	10	nA
I _{OZ}	OFF-state output current	V _O = 0 V; V _O = V _{DD} ; on-chip pull-up/down resistors disabled	-	0.5	10	nA
V _I	input voltage	pin configured to provide a digital function ^{[13][14]} 				

Table 17. Static characteristics (LPC1100XL series) ...continued

 $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
V _{IL}	LOW-level input voltage		-	-	0.3V _{DD}	V
V _{hys}	hysteresis voltage		-	0.4	-	V
V _{OH}	HIGH-level output voltage	2.5 V ≤ V _{DD} ≤ 3.6 V; I _{OH} = −4 mA	V _{DD} − 0.4	-	-	V
		1.8 V ≤ V _{DD} < 2.5 V; I _{OH} = −3 mA	V _{DD} − 0.4	-	-	V
V _{OL}	LOW-level output voltage	2.5 V ≤ V _{DD} ≤ 3.6 V; I _{OL} = 4 mA	-	-	0.4	V
		1.8 V ≤ V _{DD} < 2.5 V; I _{OL} = 3 mA	-	-	0.4	V
I _{OH}	HIGH-level output current	V _{OH} = V _{DD} − 0.4 V; 2.5 V ≤ V _{DD} ≤ 3.6 V	−4	-	-	mA
		1.8 V ≤ V _{DD} < 2.5 V	−3	-	-	mA
I _{OL}	LOW-level output current	V _{OL} = 0.4 V 2.5 V ≤ V _{DD} ≤ 3.6 V	4	-	-	mA
		1.8 V ≤ V _{DD} < 2.5 V	3	-	-	mA
I _{OHS}	HIGH-level short-circuit output current	V _{OH} = 0 V ^[16]	-	-	−45	mA
I _{OLS}	LOW-level short-circuit output current	V _{OL} = V _{DD} ^[16]	-	-	50	mA
I _{pd}	pull-down current	V _I = 5 V	10	50	150	μA
I _{pu}	pull-up current	V _I = 0 V; 2.0 V ≤ V _{DD} ≤ 3.6 V	−15	−50	−85	μA
		1.8 V ≤ V _{DD} < 2.0 V	−10	−50	−85	μA
		V _{DD} < V _I < 5 V	0	0	0	μA
High-drive output pin (PIO0_7)						
I _{IL}	LOW-level input current	V _I = 0 V; on-chip pull-up resistor disabled	-	0.5	10	nA
I _{IH}	HIGH-level input current	V _I = V _{DD} ; on-chip pull-down resistor disabled	-	0.5	10	nA
I _{OZ}	OFF-state output current	V _O = 0 V; V _O = V _{DD} ; on-chip pull-up/down resistors disabled	-	0.5	10	nA
V _I	input voltage	pin configured to provide a digital function ^{[13][14][15]}	0	-	5.0	V
V _O	output voltage	output active	0	-	V _{DD}	V
V _{IH}	HIGH-level input voltage		0.7V _{DD}	-	-	V
V _{IL}	LOW-level input voltage		-	-	0.3V _{DD}	V
V _{hys}	hysteresis voltage		0.4	-	-	V



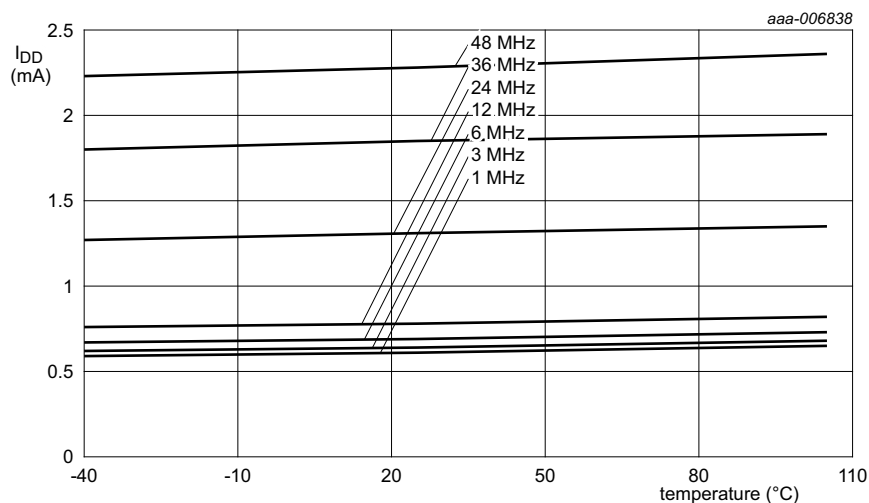
Conditions: $V_{DD} = 3.3$ V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz to 6 MHz: system oscillator enabled; PLL, IRC disabled.

12 MHz: IRC enabled; system oscillator, PLL disabled.

24 MHz to 48 MHz: IRC disabled; system oscillator, PLL enabled.

Fig 29. Active mode: Typical supply current I_{DD} versus temperature for different system clock frequencies (for LPC111xXL)



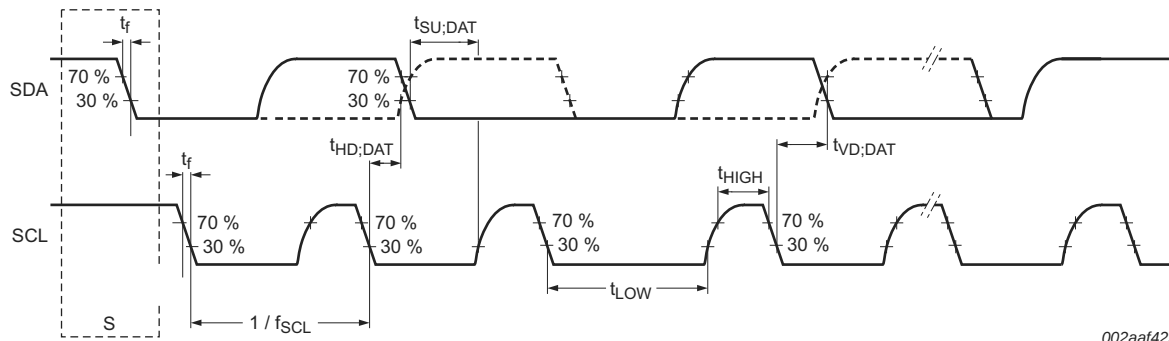
Conditions: $V_{DD} = 3.3$ V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz to 6 MHz: system oscillator enabled; PLL, IRC disabled.

12 MHz: IRC enabled; system oscillator, PLL disabled.

24 MHz to 48 MHz: IRC disabled; system oscillator, PLL enabled.

Fig 30. Sleep mode: Typical supply current I_{DD} versus temperature for different system clock frequencies (for LPC111xXL)



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Fig 46. I²C-bus pins clock timing

11.7 SPI interfaces

Table 29. Dynamic characteristics of SPI pins in SPI mode

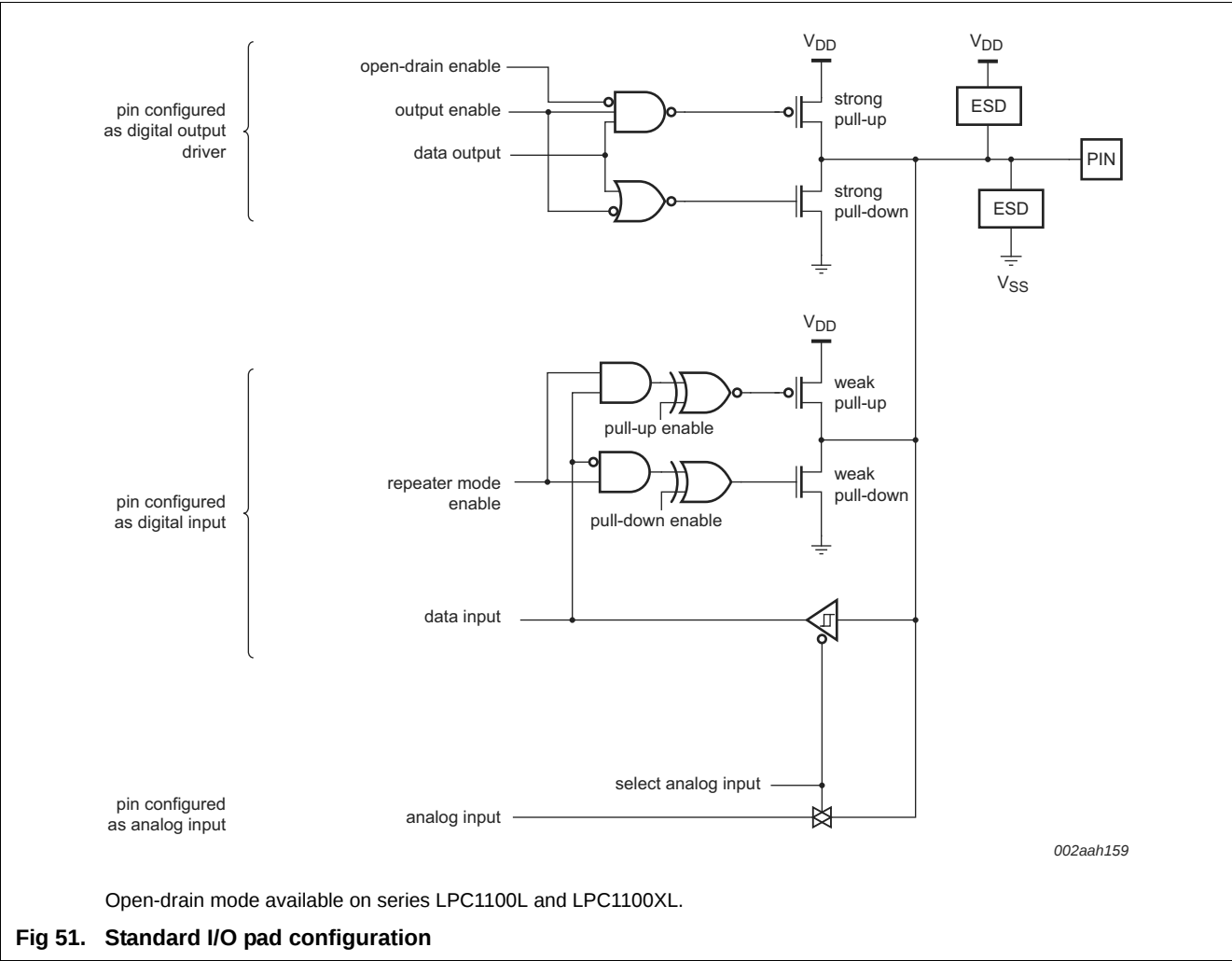
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPI master (in SPI mode)						
$T_{cy(clk)}$	clock cycle time	full-duplex mode ^[1]	50	-	-	ns
		when only transmitting ^[1]	40	-	-	ns
t_{DS}	data set-up time	in SPI mode ^[2]	15	-	-	ns
		$2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$				
		$2.0\text{ V} \leq V_{DD} < 2.4\text{ V}$ ^[2]	20	-	-	ns
		$1.8\text{ V} \leq V_{DD} < 2.0\text{ V}$ ^[2]	24	-	-	ns
t_{DH}	data hold time	in SPI mode ^[2]	0	-	-	ns
$t_{V(Q)}$	data output valid time	in SPI mode ^[2]	-	-	10	ns
$t_{h(Q)}$	data output hold time	in SPI mode ^[2]	0	-	-	ns
SPI slave (in SPI mode)						
$T_{cy(PCLK)}$	PCLK cycle time		20	-	-	ns
t_{DS}	data set-up time	in SPI mode ^{[3][4]}	0	-	-	ns
t_{DH}	data hold time	in SPI mode ^{[3][4]}	$3 \times T_{cy(PCLK)} + 4$	-	-	ns
$t_{V(Q)}$	data output valid time	in SPI mode ^{[3][4]}	-	-	$3 \times T_{cy(PCLK)} + 11$	ns
$t_{h(Q)}$	data output hold time	in SPI mode ^{[3][4]}	-	-	$2 \times T_{cy(PCLK)} + 5$	ns

[1] $T_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPSDVSR) / f_{main}$. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main} , the SPI peripheral clock divider (SSPCLKDIV), the SPI SCR parameter (specified in the SSP0CR0 register), and the SPI CPSDVSR parameter (specified in the SPI clock prescale register).

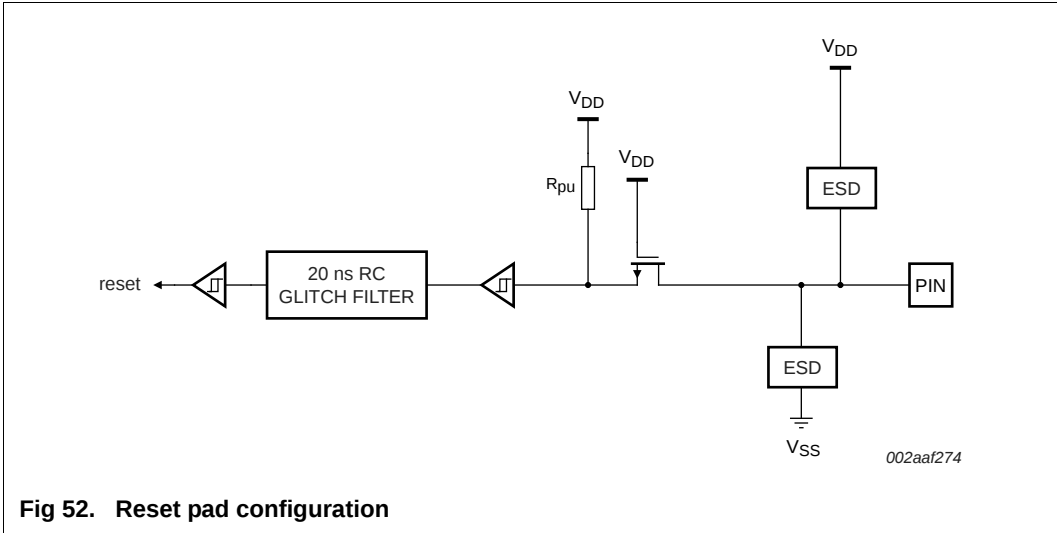
[2] $T_{amb} = -40\text{ °C to }105\text{ °C}$.

[3] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$.

[4] $T_{amb} = 25\text{ °C}$; for normal voltage supply range: $V_{DD} = 3.3\text{ V}$.



12.6 Reset pad configuration



HVQFN33: plastic thermal enhanced very thin quad flat package; no leads;
33 terminals; body 7 x 7 x 0.85 mm

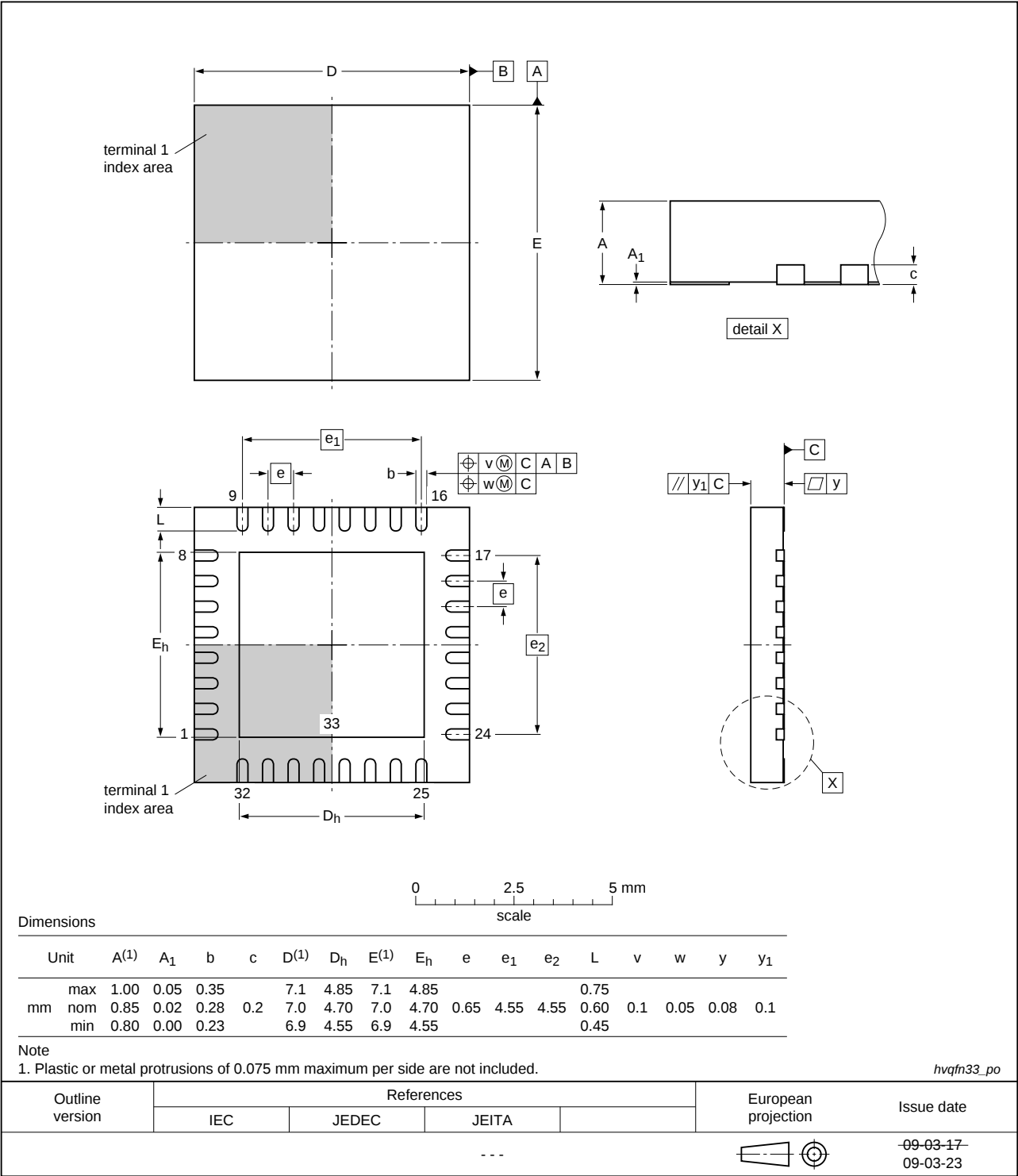


Fig 59. Package outline (HVQFN33 7x7)

TFBGA48: plastic thin fine-pitch ball grid array package; 48 balls; body 4.5 x 4.5 x 0.7 mm

SOT1155-2

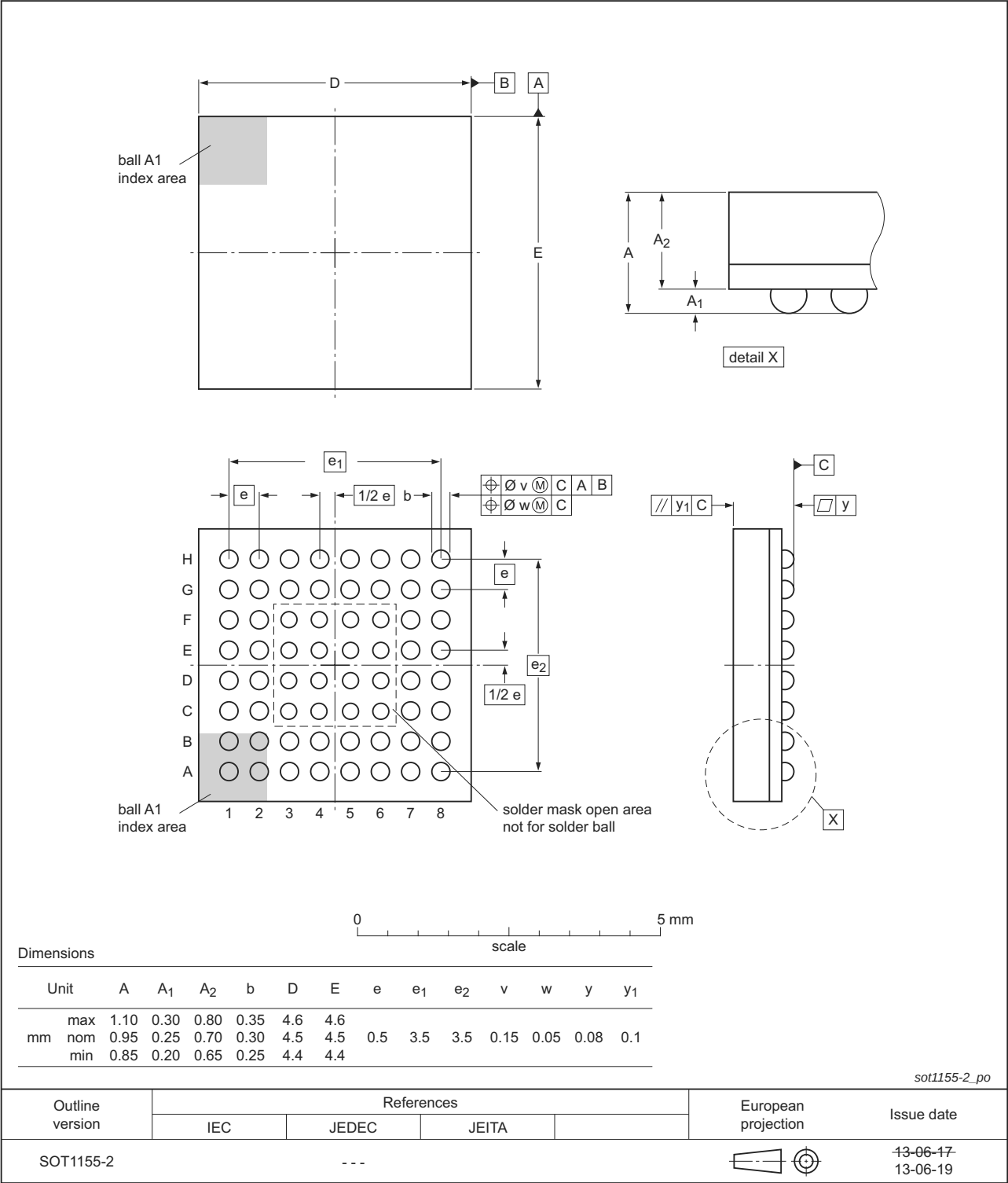


Fig 62. Package outline TFBGA48 (SOT1155-2)

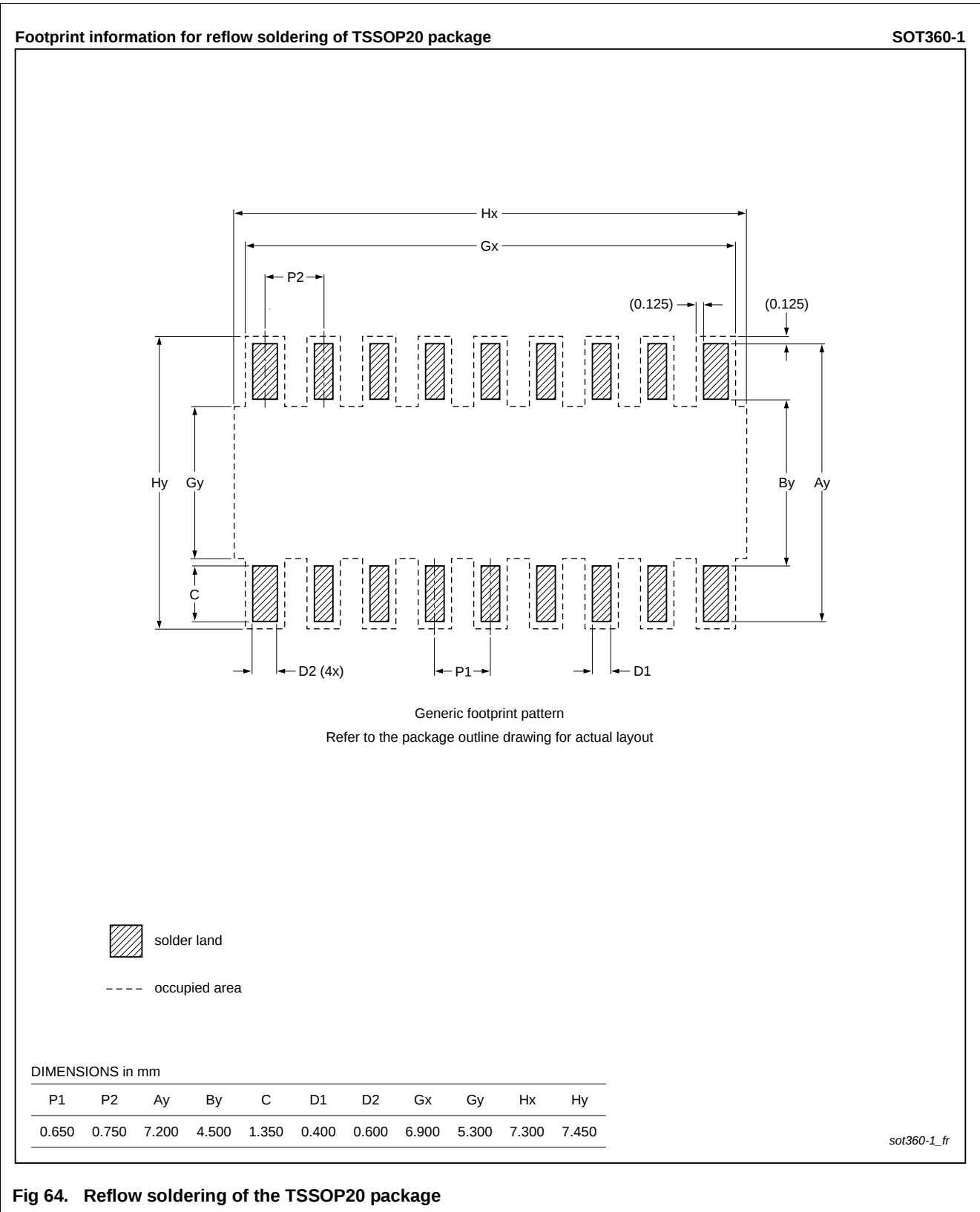


Fig 64. Reflow soldering of the TSSOP20 package

Footprint information for reflow soldering of HVQFN33 package

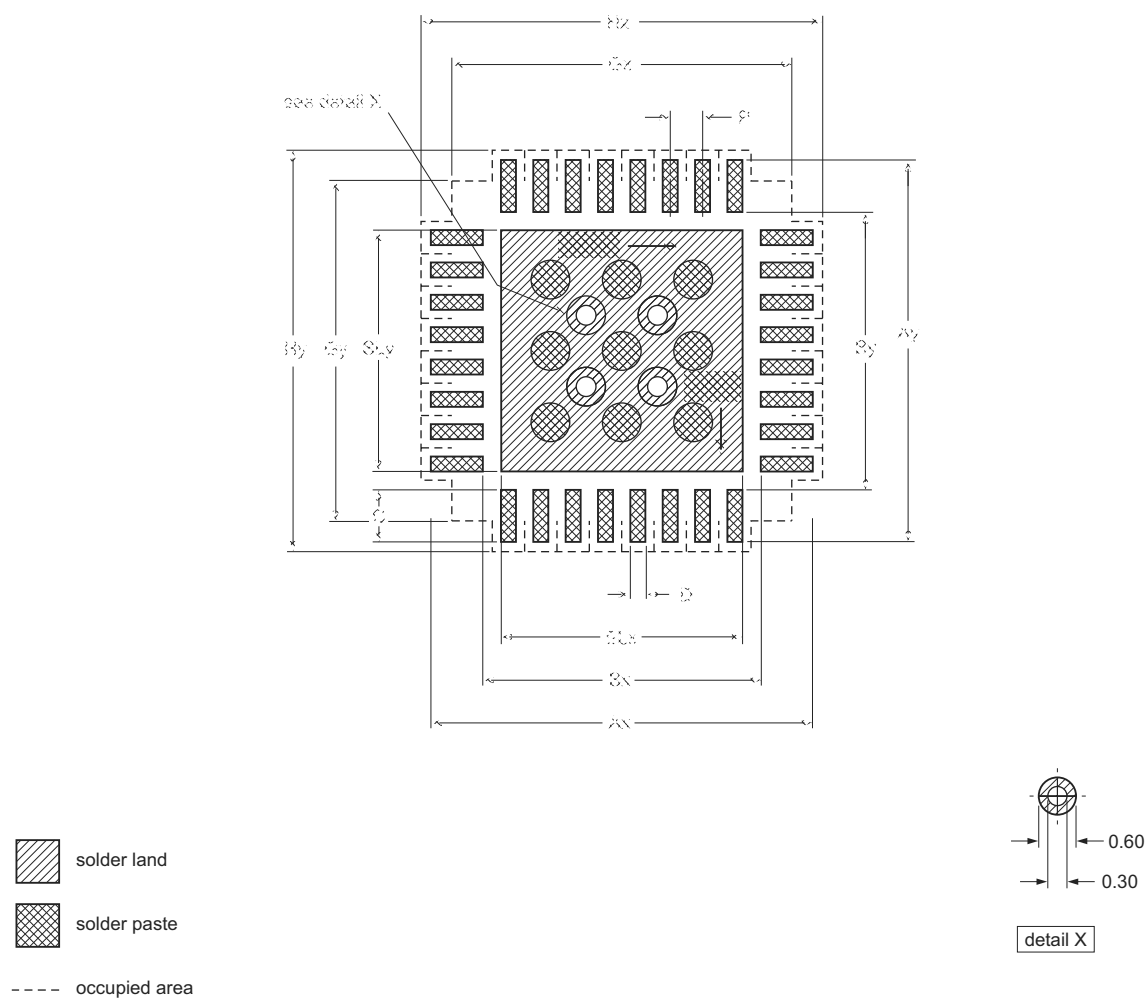


Fig 67. Reflow soldering of the HVQFN33 package (5x5)

15. Abbreviations

Table 33. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
GPIO	General Purpose Input/Output
PLL	Phase-Locked Loop
RC	Resistor-Capacitor
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
TEM	Transverse ElectroMagnetic
UART	Universal Asynchronous Receiver/Transmitter

16. References

- [1] LPC111x/LPC11Cxx User manual UM10398:
http://www.nxp.com/documents/user_manual/UM10398.pdf
- [2] LPC111x Errata sheet:
http://www.nxp.com/documents/errata_sheet/ES_LPC111X.pdf

Table 34. Revision history ...continued

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	BOD level 0 for reset added in Table 15.			
LPC111X v.7.4	20120730	Product data sheet	-	LPC111X v.7.3
Modifications:	- Function SSEL1 added to pin PIO2_0 in Figure 6 "LPC1100XL series pin configuration HVQFN33" and Table 11 "LPC1100XL series: LPC1111/12/13/14 pin description table (HVQFN33 package)". - BOD level 0 for reset and interrupt removed.			
LPC111X v.7.3	20120706	Product data sheet	-	LPC111X v.7.2
Modifications:	Corrected pinout for part LPC1112FHN24/202. Pin XTALOUT replaced by V_{DD}. See Table 6 and Figure 10.			
LPC111X v.7.2	20120604	Product data sheet	-	LPC111X v.7.1
Modifications:	- For parameters I_{OL}, V_{OL}, I_{OH}, V_{OH}, changed conditions to 1.8 V ≤ V_{DD} < 2.5 V and 2.5 V ≤ V_{DD} ≤ 3.6 V in Table 13). - Capture-clear feature added to general-purpose counter/timers (see Section 7.12; LPC1100XL series only). - Figure 47 updated for parts with configurable open-drain mode. - Added Section 9.5 "CoreMark data" - Added LPC1100L series part (LPC1112FHN24/202). - WDOSc frequency range corrected.			
LPC111X v.7.1	20120401	Product data sheet	-	LPC111X v.7
Modifications:	Added HVQFN33 (5x5) reflow soldering information.			
LPC111X v.7	20120301	Product data sheet	-	LPC1110_11_12_13_14 v.6
Modifications:	LPC1100XL series parts added (LPC1111FHN33/103, LPC1111FHN33/203, LPC1112FHN33/103, LPC1112FHN33/203, LPC1112FHI33/203, LPC1113FBD48/303, LPC1113FHN33/203, LPC1113FHN33/303, LPC1114FBD48/303, LPC1114FHN33/203, LPC1114FHN33/303, LPC1114FHI33/303, LPC1114FBD48/323, LPC1114FBD48/333, LPC1114FHN33/333, LPC1115FBD48/303).			
LPC1110_11_12_13_14 v.6	20111102	Product data sheet	-	LPC1111_12_13_14 v.5
Modifications:	- Parts LPC1112FHI33/202 and LPC1114FHI33/302 added. - Parts LPC1112FDH28/102, LPC1114FDH28/102, LPC1114FN28/102, LPC1112FDH20/102, LPC1110FD20, LPC1111FDH20/002, LPC1112FD20/102 added.			
LPC1111_12_13_14 v.5	20110622	Product data sheet	-	LPC1111_12_13_14 v.4
Modifications:	- ADC sampling frequency corrected in Table 7 (Table note 7). - Pull-up level specified in Table 3 to Table 4 and Section 7.7.1. - Parameter T_{cy(clk)} corrected on Table 17. - WWDT for parts LPC111x/102/202/302 added in Section 2 and Section 7.15. - Programmable open-drain mode for parts LPC111x/102/202/302 added in Section 2 and Section 7.12. - Condition for parameter T_{stg} in Table 5 updated. - Table note 4 of Table 5 updated. - Section 13 added. - Removed PLCC44 package information.			
LPC1111_12_13_14 v.4	20110210	Product data sheet	-	LPC1111_12_13_14 v.3

Table 34. Revision history ...continued

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	- Power consumption graphs added for parts LPC111x/102/202/302 (Figure 13 to Figure 17). - Parameter V_{hys} for I²C bus pins: typical value corrected $V_{\text{hys}} = 0.05V_{\text{DD}}$ in Table 7. - Typical value for parameter N_{endu} added in Table 12 "Flash characteristics". - I²C-bus pins configured as standard mode pins, parameter I_{OL} changed to 3.5 mA (minimum) for $2.0\text{ V} \leq V_{\text{DD}} \leq 3.6\text{ V}$. - Section 11.6 "ElectroMagnetic Compatibility (EMC)" added. - Power-up characterization added (Section 10.1 "Power-up ramp conditions").			
LPC1111_12_13_14 v.3	20101110	Product data sheet	-	LPC1111_12_13_14 v.2
Modifications:	- Parts LPC111x/102/202/302 added (LPC1100L series). - Power consumption data for parts LPC111x/102/202/302 added in Table 7. - PLL output frequency limited to 100 MHz in Section 7.15.2. - Description of $\overline{\text{RESET}}$ and WAKEUP functions updated in Section 6. - WDT description updated in Section 7.14. The WDT is a 24-bit timer. - Power profiles added to Section 2 and Section 7 for parts LPC111x/102/202/302.			
LPC1111_12_13_14 v.2	20100818	Product data sheet	-	LPC1111_12_13_14 v.1
Modifications:	V_{ESD} limit changed to -6500 V (min) /+6500 V (max) in Table 6. t_{DS} updated for SPI in master mode (Table 17). - Deep-sleep mode functionality changed to allow BOD and watchdog oscillator as the only analog blocks allowed to remain running in Deep-sleep mode (Section 7.15.5.3). V_{DD} range changed to $3.0\text{ V} \leq V_{\text{DD}} \leq 3.6\text{ V}$ in Table 15. - Reset state of pins and start logic functionality added in Table 3 to Table 5. - Section 7.16.1 added. - Section "Memory mapping control" removed. V_{OH} and I_{OH} specifications updated for high-drive pins in Table 7. - Section 9.4 added.			
LPC1111_12_13_14 v.1	20100416	Product data sheet	-	-