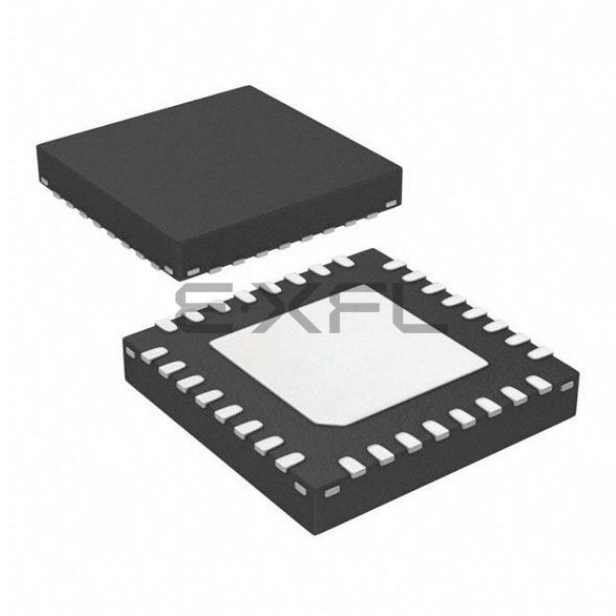

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Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	28
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VQFN Exposed Pad
Supplier Device Package	32-HVQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1112jhn33-203e

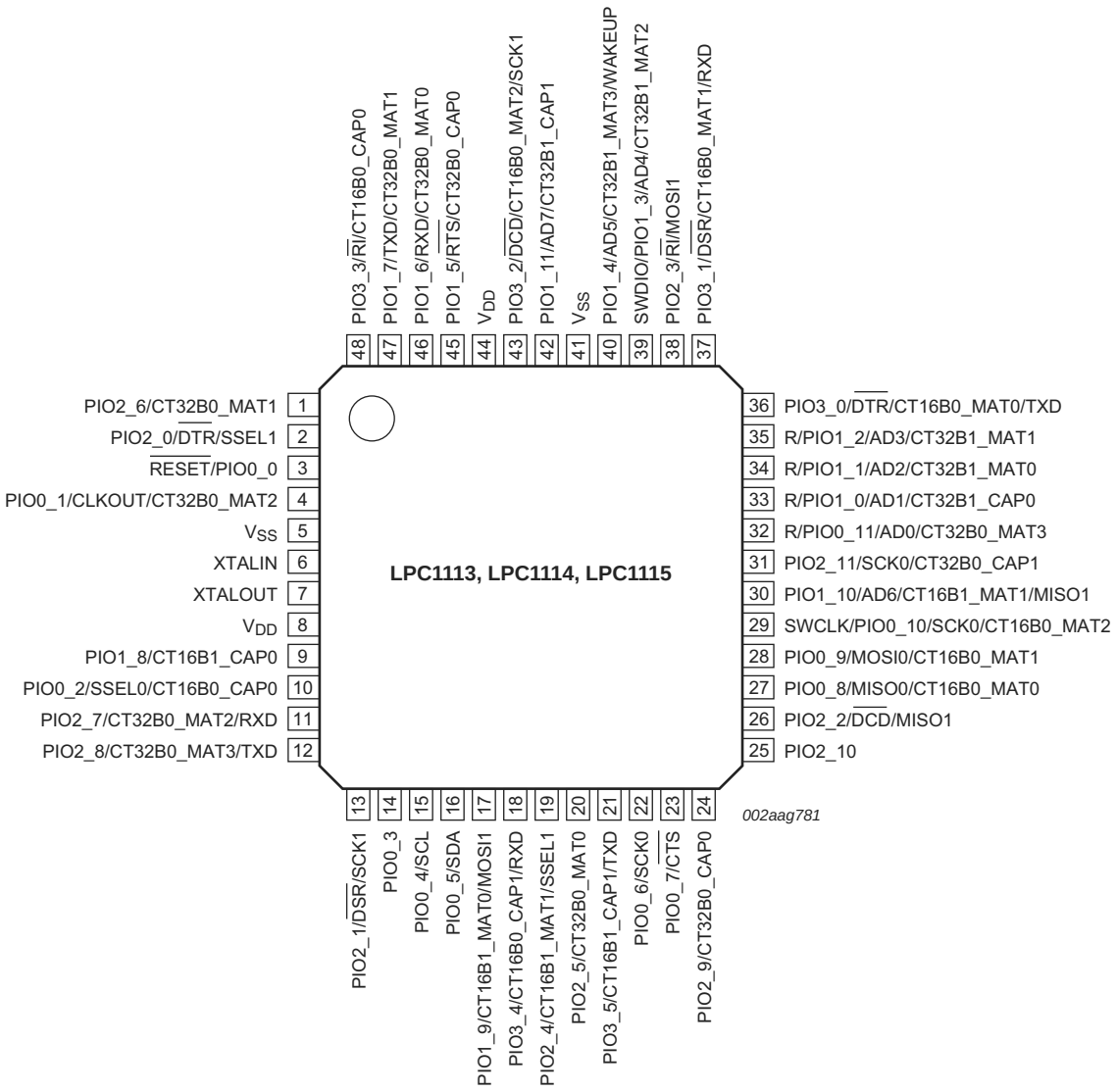


Fig 4. LPC1100XL series pin configuration LQFP48 package

Table 9. LPC1100 and LPC1100L series: LPC1111/12/13/14 pin description table (HVQFN33 package)

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO0_0 to PIO0_11					**Port 0 —** Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.
$\overline{\text{RESET}}$/PIO0_0	2[2]	yes	I	I;PU	**$\overline{\text{RESET}}$ —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO pin if an external $\overline{\text{RESET}}$ function is not needed and Deep power-down mode is not used.
			I/O	-	**PIO0_0 —** General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/ CT32B0_MAT2	3[3]	yes	I/O	I;PU	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
			O	-	**CLKOUT —** Clock out pin.
			O	-	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	8[3]	yes	I/O	I;PU	**PIO0_2 —** General purpose digital input/output pin.
			I/O	-	**SSEL0 —** Slave select for SPI0.
			I	-	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO0_3	9[3]	yes	I/O	I;PU	**PIO0_3 —** General purpose digital input/output pin.
PIO0_4/SCL	10[4]	yes	I/O	I;IA	**PIO0_4 —** General purpose digital input/output pin (open-drain).
			I/O	-	**SCL —** I^2C-bus, open-drain clock input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	11[4]	yes	I/O	I;IA	**PIO0_5 —** General purpose digital input/output pin (open-drain).
			I/O	-	**SDA —** I^2C-bus, open-drain data input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	15[3]	yes	I/O	I;PU	**PIO0_6 —** General purpose digital input/output pin.
			I/O	-	**SCK0 —** Serial clock for SPI0.
PIO0_7/$\overline{\text{CTS}}$	16[3]	yes	I/O	I;PU	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
			I	-	**$\overline{\text{CTS}}$ —** Clear To Send input for UART.
PIO0_8/MISO0/ CT16B0_MAT0	17[3]	yes	I/O	I;PU	**PIO0_8 —** General purpose digital input/output pin.
			I/O	-	**MISO0 —** Master In Slave Out for SPI0.
			O	-	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	18[3]	yes	I/O	I;PU	**PIO0_9 —** General purpose digital input/output pin.
			I/O	-	**MOSI0 —** Master Out Slave In for SPI0.
			O	-	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2	19[3]	yes	I	I;PU	**SWCLK —** Serial wire clock.
			I/O	-	**PIO0_10 —** General purpose digital input/output pin.
			I/O	-	**SCK0 —** Serial clock for SPI0.
			O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.

[6] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

Table 10. LPC1100XL series: LPC1113/14/15 pin description table (LQFP48 and TFBGA48 package)

Symbol	LQFP48	TFBGA48	Start logic input	Type	Reset state [1]	Description
PIO0_0 to PIO0_11				I/O		**Port 0 —** Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.
$\overline{\text{RESET}}$/PIO0_0	3[2]	C1[2]	yes	I	I; PU	**$\overline{\text{RESET}}$ —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO pin if an external $\overline{\text{RESET}}$ function is not needed and Deep power-down mode is not used.
				I/O	-	**PIO0_0 —** General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/ CT32B0_MAT2	4[3]	C2[3]	yes	I/O	I; PU	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
				O	-	**CLKOUT —** Clockout pin.
				O	-	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	10[3]	F1[3]	yes	I/O	I; PU	**PIO0_2 —** General purpose digital input/output pin.
				I/O	-	**SSEL0 —** Slave Select for SPI0.
				I	-	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO0_3	14[3]	H2[3]	yes	I/O	I; PU	**PIO0_3 —** General purpose digital input/output pin.
PIO0_4/SCL	15[4]	G3[4]	yes	I/O	I; IA	**PIO0_4 —** General purpose digital input/output pin (open-drain).
				I/O	-	**SCL —** I^2C-bus, open-drain clock input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	16[4]	H3[4]	yes	I/O	I; IA	**PIO0_5 —** General purpose digital input/output pin (open-drain).
				I/O	-	**SDA —** I^2C-bus, open-drain data input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	22[3]	H6[3]	yes	I/O	I; PU	**PIO0_6 —** General purpose digital input/output pin.
				I/O	-	**SCK0 —** Serial clock for SPI0.
PIO0_7/$\overline{\text{CTS}}$	23[3]	G7[3]	yes	I/O	I; PU	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
				I	-	**$\overline{\text{CTS}}$ —** Clear To Send input for UART.

Table 10. LPC1100XL series: LPC1113/14/15 pin description table (LQFP48 and TFBGA48 package) *…continued*

Symbol	LQFP48	TFBGA48	Start logic input	Type	Reset state [1]	Description
PIO2_2/$\overline{\text{DCD}}$/MISO1	26[3]	G8[3]	no	I/O	I; PU	**PIO2_2 —** General purpose digital input/output pin.
				I	-	**$\overline{\text{DCD}}$ —** Data Carrier Detect input for UART.
				I/O	-	**MISO1 —** Master In Slave Out for SPI1.
PIO2_3/$\overline{\text{RI}}$/MOSI1	38[3]	A7[3]	no	I/O	I; PU	**PIO2_3 —** General purpose digital input/output pin.
				I	-	**$\overline{\text{RI}}$ —** Ring Indicator input for UART.
				I/O	-	**MOSI1 —** Master Out Slave In for SPI1.
PIO2_4/ CT16B1_MAT1/ SSEL1	19[3]	G5[3]	no	I/O	I; PU	**PIO2_4 —** General purpose digital input/output pin.
				O	-	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
				O	-	**SSEL1 —** Slave Select for SPI1.
PIO2_5/ CT32B0_MAT0	20[3]	H5[3]	no	I/O	I; PU	**PIO2_5 —** General purpose digital input/output pin.
				O	-	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO2_6/ CT32B0_MAT1	1[3]	A1[3]	no	I/O	I; PU	**PIO2_6 —** General purpose digital input/output pin.
				O	-	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO2_7/ CT32B0_MAT2/RXD	11[3]	G2[3]	no	I/O	I; PU	**PIO2_7 —** General purpose digital input/output pin.
				O	-	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
				I	-	**RXD —** Receiver input for UART.
PIO2_8/ CT32B0_MAT3/TXD	12[3]	G1[3]	no	I/O	I; PU	**PIO2_8 —** General purpose digital input/output pin.
				O	-	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
				O	-	**TXD —** Transmitter output for UART.
PIO2_9/ CT32B0_CAP0	24[3]	H7[3]	no	I/O	I; PU	**PIO2_9 —** General purpose digital input/output pin.
				I	-	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
PIO2_10	25[3]	H8[3]	no	I/O	I; PU	**PIO2_10 —** General purpose digital input/output pin.
PIO2_11/SCK0/ CT32B0_CAP1	31[3]	D7[3]	no	I/O	I; PU	**PIO2_11 —** General purpose digital input/output pin.
				I/O	-	**SCK0 —** Serial clock for SPI0.
				I	-	**CT32B0_CAP1 —** Capture input for 32-bit timer 0.
PIO3_0 to PIO3_5				I/O		**Port 3 —** Port 3 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 3 pins depends on the function selected through the IOCONFIG register block. Pins PIO3_6 to PIO3_11 are not available.
PIO3_0/$\overline{\text{DTR}}$/ CT16B0_MAT0/TXD	36[3]	B8[3]	no	I/O	I; PU	**PIO3_0 —** General purpose digital input/output pin.
				O	-	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for UART.
				O	-	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
				O	-	**TXD —** Transmitter Output for UART.
PIO3_1/$\overline{\text{DSR}}$/ CT16B0_MAT1/RXD	37[3]	A8[3]	no	I/O	I; PU	**PIO3_1 —** General purpose digital input/output pin.
				I	-	**$\overline{\text{DSR}}$ —** Data Set Ready input for UART.
				O	-	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
				I	-	**RXD —** Receiver input for UART.

Table 11. LPC1100XL series: LPC1111/12/13/14 pin description table (HVQFN33 package) *…continued*

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
R/PIO0_11/AD0/ CT32B0_MAT3	21[5]	yes	-	I;PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO0_11 —** General purpose digital input/output pin.
			I	-	**AD0 —** A/D converter, input 0.
			O	-	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
PIO1_0 to PIO1_11					**Port 1 —** Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block.
R/PIO1_0/AD1/ CT32B1_CAP0	22[5]	yes	-	I;PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO1_0 —** General purpose digital input/output pin.
			I	-	**AD1 —** A/D converter, input 1.
			I	-	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
R/PIO1_1/AD2/ CT32B1_MAT0	23[5]	no	-	I;PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO1_1 —** General purpose digital input/output pin.
			I	-	**AD2 —** A/D converter, input 2.
			O	-	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
R/PIO1_2/AD3/ CT32B1_MAT1	24[5]	no	-	I;PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO1_2 —** General purpose digital input/output pin.
			I	-	**AD3 —** A/D converter, input 3.
			O	-	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ AD4/CT32B1_MAT2	25[5]	no	I/O	I;PU	**SWDIO —** Serial wire debug input/output.
			I/O	-	**PIO1_3 —** General purpose digital input/output pin.
			I	-	**AD4 —** A/D converter, input 4.
			O	-	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
PIO1_4/AD5/ CT32B1_MAT3/ WAKEUP	26[5]	no	I/O	I;PU	**PIO1_4 —** General purpose digital input/output pin with 10 ns glitch filter. In Deep power-down mode, this pin serves as the Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
			I	-	**AD5 —** A/D converter, input 5.
			O	-	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
PIO1_5/$\overline{\text{RTS}}$/ CT32B0_CAP0	30[3]	no	I/O	I;PU	**PIO1_5 —** General purpose digital input/output pin.
			O	-	**$\overline{\text{RTS}}$ —** Request To Send output for UART.
			I	-	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
PIO1_6/RXD/ CT32B0_MAT0	31[3]	no	I/O	I;PU	**PIO1_6 —** General purpose digital input/output pin.
			I	-	**RXD —** Receiver input for UART.
			O	-	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

7.16.1.3 Watchdog oscillator

The watchdog oscillator can be used as a clock source that directly drives the CPU, the watchdog timer, or the CLKOUT pin. The watchdog oscillator nominal frequency is programmable between 9.4 kHz and 2.3 MHz. The frequency spread over processing and temperature is ±40 %.

7.16.2 System PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The PLL output frequency must be lower than 100 MHz. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

7.16.3 Clock output

The LPC1110/11/12/13/14/15 features a clock output function that routes the IRC oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin.

7.16.4 Wake-up process

The LPC1110/11/12/13/14/15 begin operation at power-up and when awakened from Deep power-down mode by using the 12 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the system oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

7.16.5 Power control

The LPC1110/11/12/13/14/15 support a variety of power control features. There are three special modes of processor power reduction: Sleep mode, Deep-sleep mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

7.16.5.1 Power profiles (LPC1100L and LPC1100XL series only)

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC1110/11/12/13/14/15 for one of the following power modes:

Table 15. LPC111x/x02 Thermal resistance value (C/W): ±15 %

HVQFN33		**LQFP48**	
θ**ja**		θ**ja**	
JEDEC (4.5 in × 4 in)		**JEDEC (4.5 in × 4 in)**	
0 m/s	40.8	0 m/s	83.3
1 m/s	33.1	1 m/s	74.9
2.5 m/s	28.7	2.5 m/s	69.4
Single-layer (4.5 in × 3 in)		**8-layer (4.5 in × 3 in)**	
0 m/s	85.2	0 m/s	116.3
1 m/s	62	1 m/s	96
2.5 m/s	53.5	2.5 m/s	87.5
θjc	17.9	θjc	28.3
θjb	1.5	θjb	35.5

Table 16. Static characteristics (LPC1100, LPC1100L series) *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as Fast-mode Plus pins 2.5 V ≤ V_{DD} ≤ 3.6 V	20	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V	16	-	-	
I_{LI}	input leakage current	V_I = V_{DD} [16]	-	2	4	μA
		V_I = 5 V	-	10	22	μA
Oscillator pins						
$V_{i(xtal)}$	crystal input voltage		−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage		−0.5	1.8	1.95	V
Pin capacitance						
C_{io}	input/output capacitance	pins configured for analog function	-	-	7.1	pF
		I^2C-bus pins (PIO0_4 and PIO0_5)	-	-	2.5	pF
		pins configured as GPIO	-	-	2.8	pF

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] T_{amb} = 25 °C.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] IRC enabled; system oscillator disabled; system PLL disabled.

[5] BOD disabled.

[6] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks to UART and SPI0/1 disabled in system configuration block.

[7] IRC disabled; system oscillator enabled; system PLL enabled.

[8] All oscillators and analog blocks turned off in the PDSLEEPCFG register; PDSLEEPCFG = 0x0000 18FF.

[9] WAKEUP pin and RESET pin are pulled HIGH externally.

[10] System oscillator enabled; IRC disabled; system PLL disabled.

[11] Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.

[12] Including voltage on outputs in 3-state mode.

[13] V_{DD} supply voltage must be present.

[14] 3-state outputs go into 3-state mode in Deep power-down mode.

[15] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[16] To V_{SS}.

10.3 ADC static characteristics

Table 18. ADC static characteristics

T_{amb} = −40 °C to +105 °C unless otherwise specified; ADC frequency 4.5 MHz, V_{DD} = 2.5 V to 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		0	-	V_{DD}	V
C_{ia}	analog input capacitance		-	-	1	pF
E_D	differential linearity error	[1][2]	-	-	± 1	LSB
$E_{L(adj)}$	integral non-linearity	[3]	-	-	± 1.5	LSB
E_O	offset error	[4]	-	-	± 3.5	LSB
E_G	gain error	[5]	-	-	0.6	%
E_T	absolute error	[6]	-	-	± 4	LSB
R_{vsi}	voltage source interface resistance		-	-	40	kΩ
R_i	input resistance	[7][8]	-	-	2.5	MΩ

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 17.

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 17.

[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 17.

[5] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 17.

[6] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 17.

[7] T_{amb} = 25 °C; maximum sampling frequency f_s = 400 kSamples/s and analog input capacitance C_{ia} = 1 pF.

[8] Input resistance R_i depends on the sampling frequency f_s: $R_i = 1 / (f_s \times C_{ia})$.

10.4 BOD static characteristics

Table 19. BOD static characteristics[1]

T_{amb} = 25 °C.

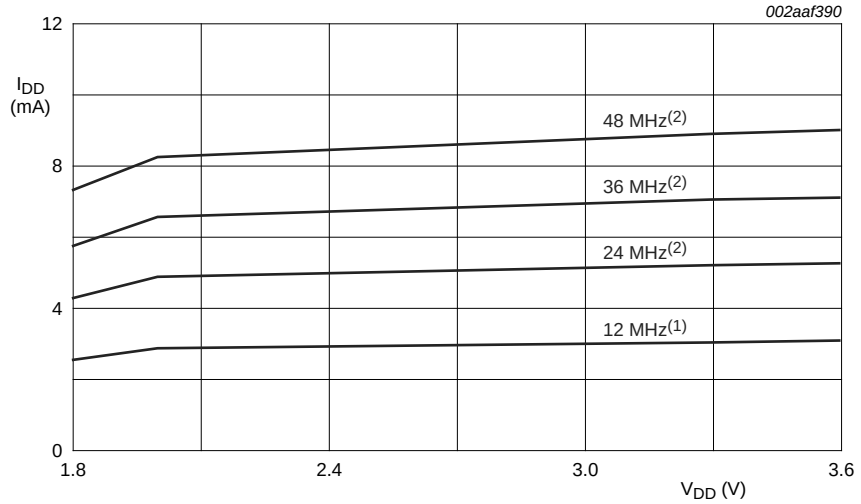
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 1				
		assertion	-	2.22	-	V
		de-assertion	-	2.35	-	V
		interrupt level 2				
		assertion	-	2.52	-	V
		de-assertion	-	2.66	-	V
		interrupt level 3				
		assertion	-	2.80	-	V
		de-assertion	-	2.90	-	V
		reset level 0				
		assertion	-	1.46	-	V
		de-assertion	-	1.63	-	V
		reset level 1				
		assertion	-	2.06	-	V
		de-assertion	-	2.15	-	V
		reset level 2				
		assertion	-	2.35	-	V
		de-assertion	-	2.43	-	V
		reset level 3				
		assertion	-	2.63	-	V
		de-assertion	-	2.71	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *LPC111x user manual*.

10.5 Power consumption LPC1100 series (LPC111x/101/201/301)

Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see *LPC111x user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCONFIG block.
- Configure GPIO pins as outputs using the GPIOnDIR registers.
- Write 0 to all GPIOnDATA registers to drive the outputs LOW.



Conditions: T_{amb} = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

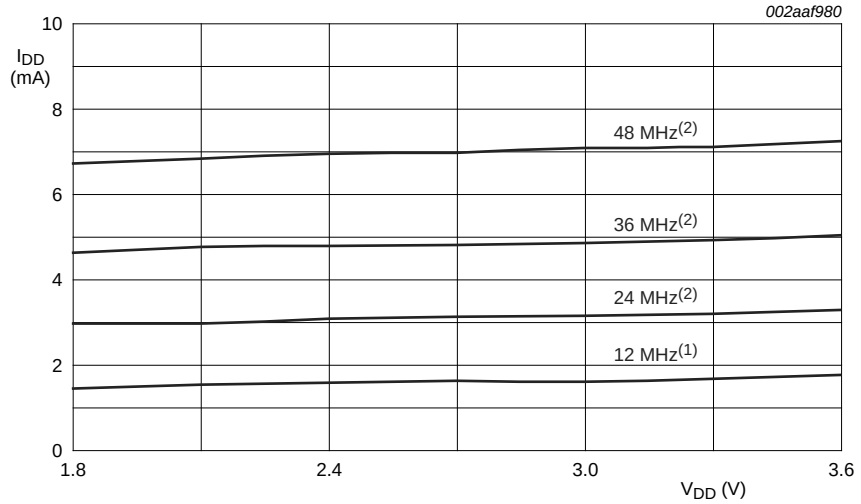
(2) System oscillator and system PLL enabled; IRC disabled.

Fig 18. Active mode: Typical supply current I_{DD} versus supply voltage V_{DD} for different system clock frequencies (for LPC111x/101/201/301)

10.6 Power consumption LPC1100L series (LPC111x/002/102/202/302)

Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see *LPC111x user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCONFIG block.
- Configure GPIO pins as outputs using the GPIOnDIR registers.
- Write 0 to all GPIOnDATA registers to drive the outputs LOW.



Conditions: T_{amb} = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 23. Active mode: Typical supply current I_{DD} versus supply voltage V_{DD} for different system clock frequencies (for LPC111x/002/102/202/302)

10.7 Power consumption LPC1100XL series (LPC111x/103/203/303/323/333)

Table 20. Power consumption at very low frequencies using the watchdog oscillator

Symbol	Parameter	Conditions[1]	Min	Typ[2]	Max	Unit
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash				
		system clock = 8.8 kHz	-	275	-	μA
		system clock = 257 kHz	-	305	-	μA
		system clock = 515 kHz	-	335	-	μA
		system clock = 784 kHz	-	368	-	μA
		system clock = 1028 kHz	-	396	-	μA
		system clock = 2230 kHz	-	538	-	μA
		Sleep mode; system clock = 8.8 kHz	-	274	-	μA
		system clock = 257 kHz	-	285	-	μA
		system clock = 515 kHz	-	295	-	μA
		system clock = 784 kHz	-	309	-	μA
		system clock = 1028 kHz	-	317	-	μA
		system clock = 2230 kHz	-	368	-	μA

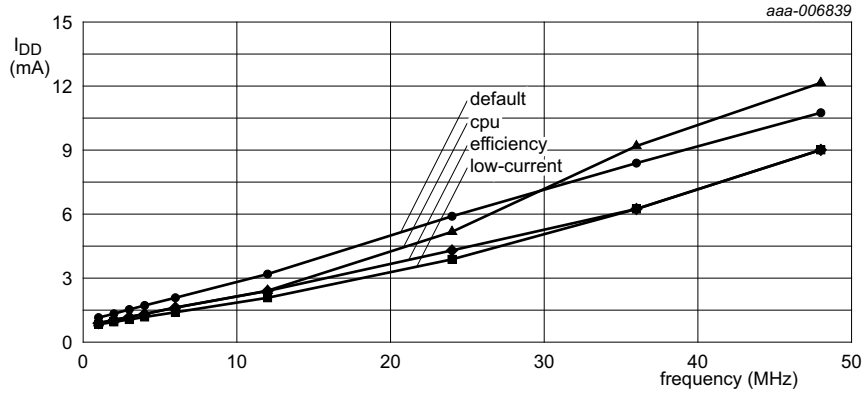
[1] WDT OSC enabled, V_{DD} = 3.3 V, Temp = 25 °C.

Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.

I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled, IRC disabled, System Oscillator disabled, System PLL disabled, BOD disabled.

All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks to UART and SPI0/1 disabled in system configuration block.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.



V_{DD} = 3.3 V; T = 25 °C; active mode; typical samples. IRC enabled; main clock derived from IRC; PLL and SYSAHBCLKDIV enabled as needed.

Fig 35. CoreMark current consumption for different power modes using IRC

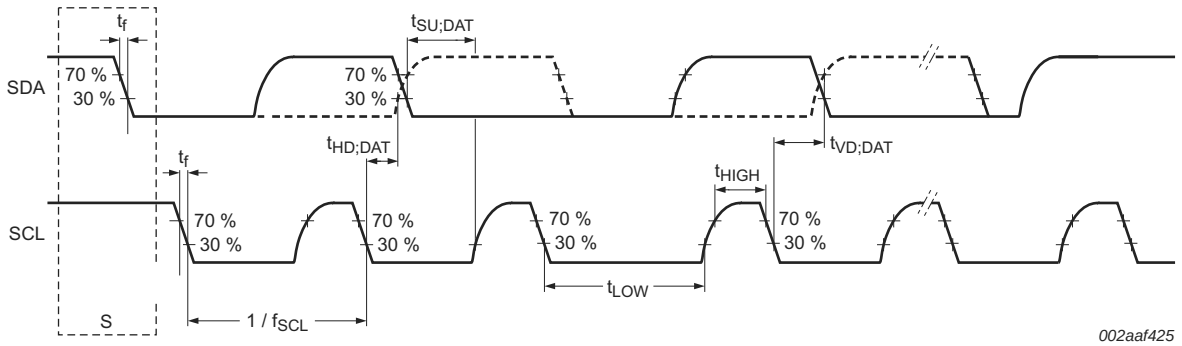


Fig 46. I^2C-bus pins clock timing

11.7 SPI interfaces

Table 29. Dynamic characteristics of SPI pins in SPI mode

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SPI master (in SPI mode)							
$T_{cy(clk)}$	clock cycle time	full-duplex mode	[1]	50	-	-	ns
		when only transmitting	[1]	40			ns
t_{DS}	data set-up time	in SPI mode	[2]	15	-	-	ns
		2.4 V ≤ V_{DD} ≤ 3.6 V					
		2.0 V ≤ V_{DD} < 2.4 V	[2]	20			ns
		1.8 V ≤ V_{DD} < 2.0 V	[2]	24	-	-	ns
t_{DH}	data hold time	in SPI mode	[2]	0	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[2]	-	-	10	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[2]	0	-	-	ns
SPI slave (in SPI mode)							
$T_{cy(PCLK)}$	PCLK cycle time			20	-	-	ns
t_{DS}	data set-up time	in SPI mode	[3][4]	0	-	-	ns
t_{DH}	data hold time	in SPI mode	[3][4]	3 × $T_{cy(PCLK)}$ + 4	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[3][4]	-	-	3 × $T_{cy(PCLK)}$ + 11	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[3][4]	-	-	2 × $T_{cy(PCLK)}$ + 5	ns

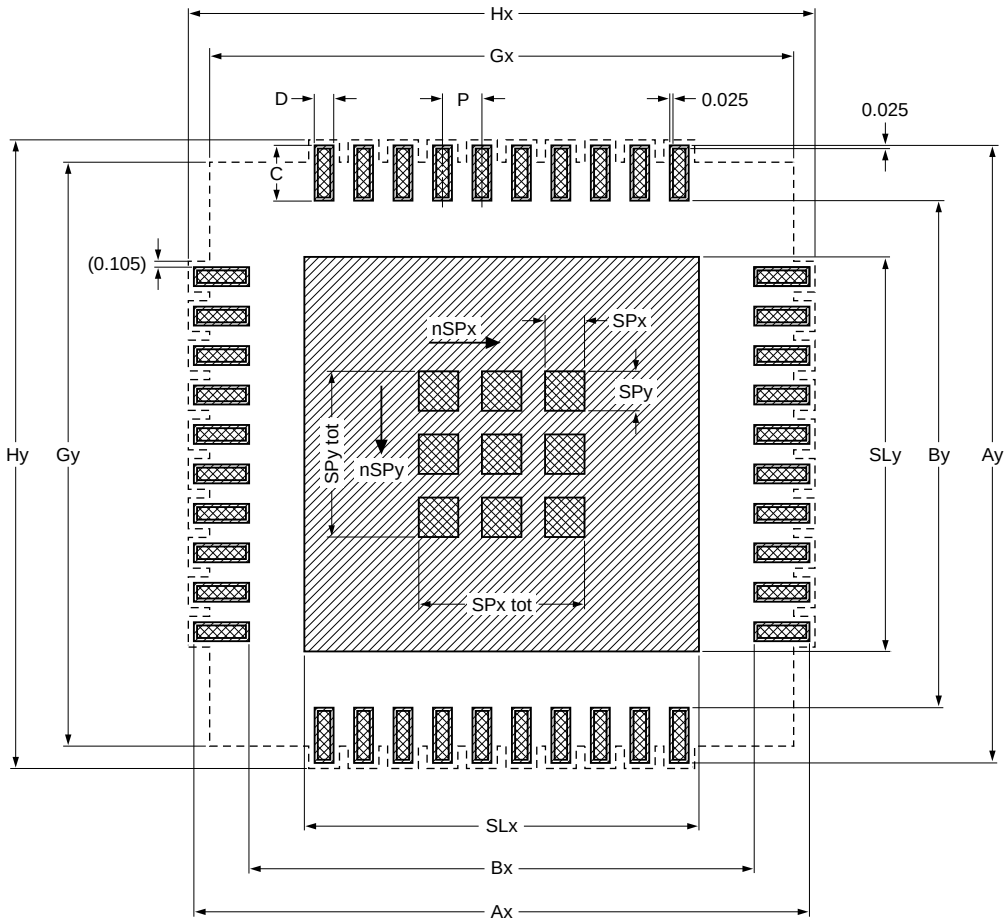
[1] $T_{cy(clk)}$ = (SSPCLKDIV × (1 + SCR) × CPSDVSR) / f_{main}. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SPI peripheral clock divider (SSPCLKDIV), the SPI SCR parameter (specified in the SSP0CR0 register), and the SPI CPSDVSR parameter (specified in the SPI clock prescale register).

[2] T_{amb} = −40 °C to 105 °C.

[3] $T_{cy(clk)}$ = 12 × $T_{cy(PCLK)}$.

[4] T_{amb} = 25 °C; for normal voltage supply range: V_{DD} = 3.3 V.

Footprint information for reflow soldering of HVQFN24 package **SOT616-3**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

solder paste deposit

solder land plus solder paste

occupied area

nSPx	nSPy
2	2

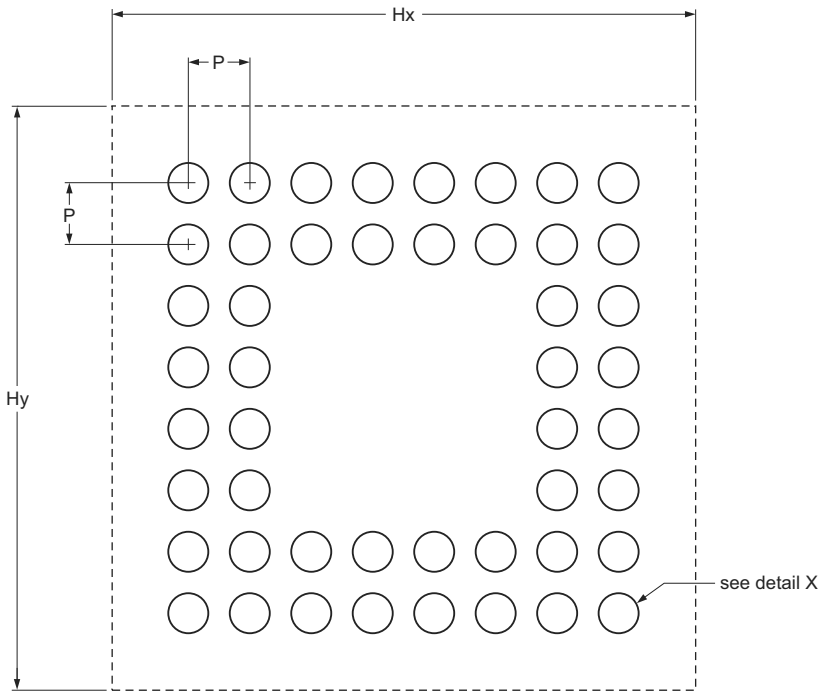
Dimensions in mm

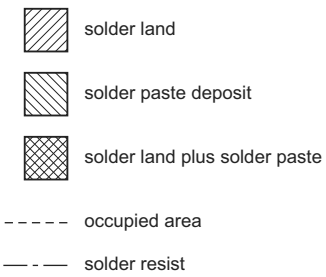
P	Ax	Ay	Bx	By	C	D	SLx	SLy	SPx tot	SPy tot	SPx	SPy	Gx	Gy	Hx	Hy
0.500	5.000	5.000	3.200	3.200	0.900	0.240	2.500	2.500	1.500	1.500	0.550	0.550	4.300	4.300	5.250	5.250

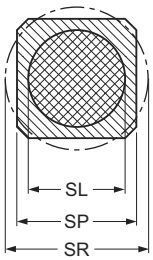
Issue date ~~07-05-07~~ 09-06-15 *sot616-3_fr*

Fig 66. Reflow soldering of the HVQFN24 package

Footprint information for reflow soldering of TFBGA48 package **SOT1155-2**







detail X

DIMENSIONS in mm

P	SL	SP	SR	Hx	Hy
0.50	0.225	0.275	0.325	4.75	4.75

sot1155-2_fr

Fig 70. Reflow soldering for the TFBGA48 package

Table 34. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	BOD level 0 for reset added in Table 15.			
LPC111X v.7.4	20120730	Product data sheet	-	LPC111X v.7.3
Modifications:	• Function SSEL1 added to pin PIO2_0 in Figure 6 “LPC1100XL series pin configuration HVQFN33” and Table 11 “LPC1100XL series: LPC1111/12/13/14 pin description table (HVQFN33 package)”. • BOD level 0 for reset and interrupt removed.			
LPC111X v.7.3	20120706	Product data sheet	-	LPC111X v.7.2
Modifications:	• Corrected pinout for part LPC1112FHN24/202. Pin XTALOUT replaced by V_{DD}. See Table 6 and Figure 10.			
LPC111X v.7.2	20120604	Product data sheet	-	LPC111X v.7.1
Modifications:	• For parameters I_{OL}, V_{OL}, I_{OH}, V_{OH}, changed conditions to 1.8 V ≤ V_{DD} < 2.5 V and 2.5 V ≤ V_{DD} ≤ 3.6 V in Table 13). • Capture-clear feature added to general-purpose counter/timers (see Section 7.12; LPC1100XL series only). • Figure 47 updated for parts with configurable open-drain mode. • Added Section 9.5 “CoreMark data” • Added LPC1100L series part (LPC1112FHN24/202). • WDOSc frequency range corrected.			
LPC111X v.7.1	20120401	Product data sheet	-	LPC111X v.7
Modifications:	• Added HVQFN33 (5x5) reflow soldering information.			
LPC111X v.7	20120301	Product data sheet	-	LPC1110_11_12_13_14 v.6
Modifications:	• LPC1100XL series parts added (LPC1111FHN33/103, LPC1111FHN33/203, LPC1112FHN33/103, LPC1112FHN33/203, LPC1112FHI33/203, LPC1113FBD48/303, LPC1113FHN33/203, LPC1113FHN33/303, LPC1114FBD48/303, LPC1114FHN33/203, LPC1114FHN33/303, LPC1114FHI33/303, LPC1114FBD48/323, LPC1114FBD48/333, LPC1114FHN33/333, LPC1115FBD48/303).			
LPC1110_11_12_13_14 v.6	20111102	Product data sheet	-	LPC1111_12_13_14 v.5
Modifications:	• Parts LPC1112FHI33/202 and LPC1114FHI33/302 added. • Parts LPC1112FDH28/102, LPC1114FDH28/102, LPC1114FN28/102, LPC1112FDH20/102, LPC1110FD20, LPC1111FDH20/002, LPC1112FD20/102 added.			
LPC1111_12_13_14 v.5	20110622	Product data sheet	-	LPC1111_12_13_14 v.4
Modifications:	• ADC sampling frequency corrected in Table 7 (Table note 7). • Pull-up level specified in Table 3 to Table 4 and Section 7.7.1. • Parameter $T_{cy(clk)}$ corrected on Table 17. • WWDT for parts LPC111x/102/202/302 added in Section 2 and Section 7.15. • Programmable open-drain mode for parts LPC111x/102/202/302 added in Section 2 and Section 7.12. • Condition for parameter T_{stg} in Table 5 updated. • Table note 4 of Table 5 updated. • Section 13 added. • Removed PLCC44 package information.			
LPC1111_12_13_14 v.4	20110210	Product data sheet	-	LPC1111_12_13_14 v.3

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18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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