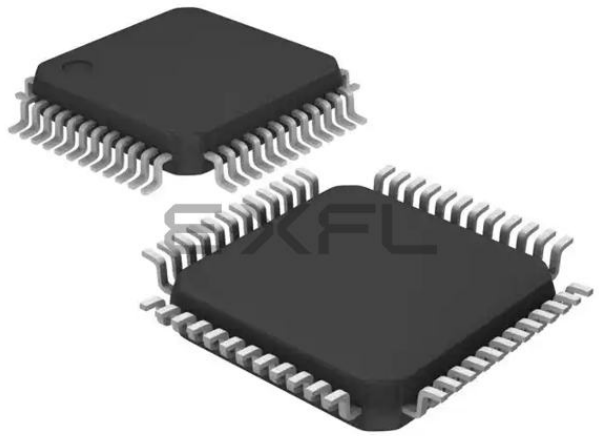


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, WDT |
| Number of I/O | 42 |
| Program Memory Size | 24KB (24K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1113fbd48-301-1 |

- LPC1100L series available as TSSOP28 package, DIP28 package, TSSOP20 package, and SO20 package.
- Extended temperature (−40 °C to +105 °C) for selected parts (see Table 2).

## 3. Applications

- eMetering
- Alarm systems
- Lighting
- White goods

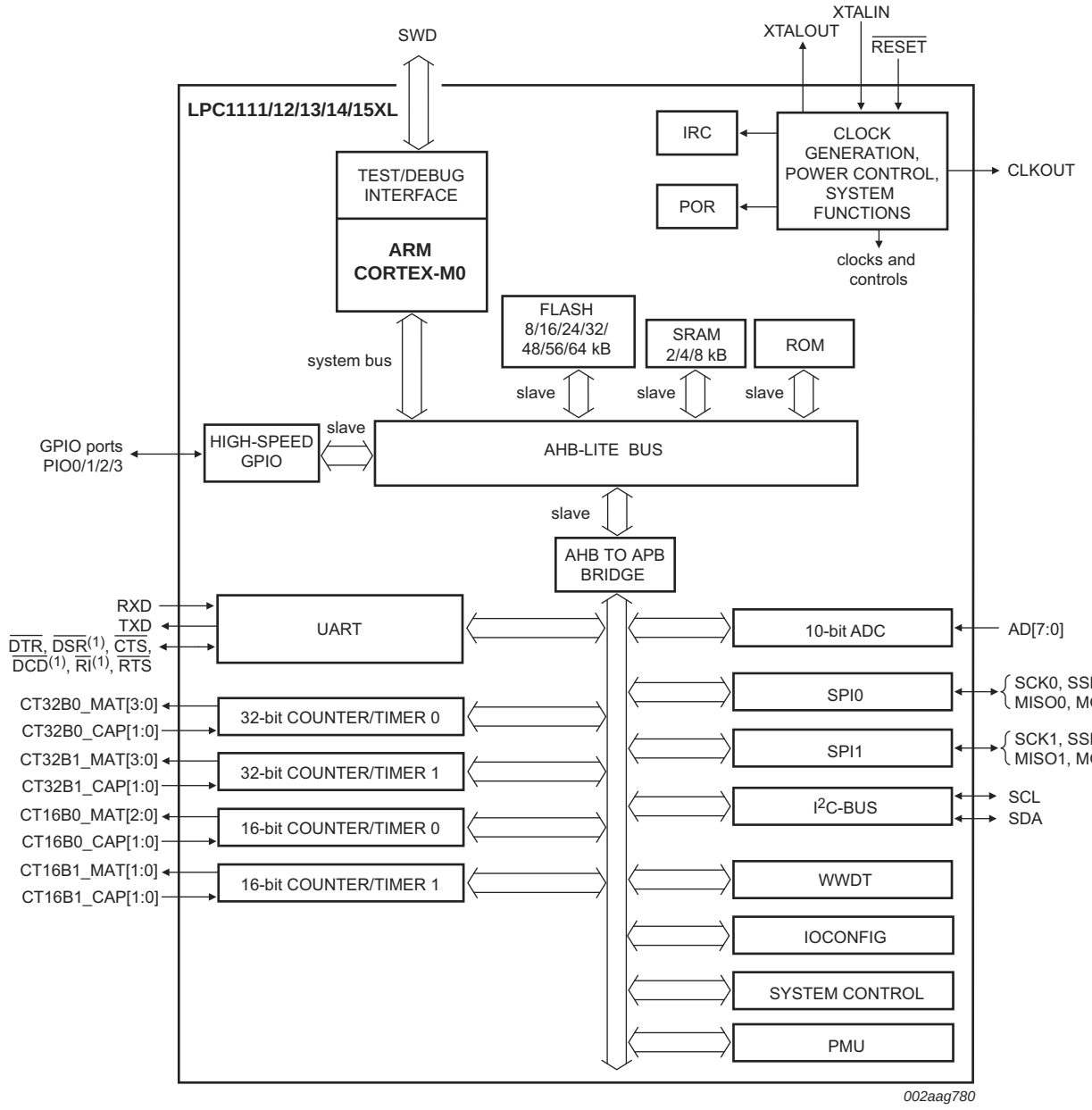
## 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| **SO20, TSSOP20, TSSOP28, and DIP28 packages** | | | |
| LPC1110FD20 | SO20 | SO20: plastic small outline package; 20 leads; body width 7.5 mm | SOT163-1 |
| LPC1111FDH20/002 | TSSOP20 | TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm | SOT360-1 |
| LPC1112FD20/102 | SO20 | SO20: plastic small outline package; 20 leads; body width 7.5 mm | SOT163-1 |
| LPC1112FDH20/102 | TSSOP20 | TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm | SOT360-1 |
| LPC1112FDH28/102 | TSSOP28 | TSSOP28: plastic thin shrink small outline package; 28 leads; body width 4.4 mm | SOT361-1 |
| LPC1114FDH28/102 | TSSOP28 | TSSOP28: plastic thin shrink small outline package; 28 leads; body width 4.4 mm | SOT361-1 |
| LPC1114FN28/102 | DIP28 | DIP28: plastic dual in-line package; 28 leads (600 mil) | SOT117-1 |
| **HVQFN24/33, LQFP48, and TFBGA48 packages** | | | |
| LPC1111FHN33/101 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1111FHN33/102 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1111FHN33/201 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1111FHN33/202 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1111FHN33/103 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1111JHN33/103 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1111FHN33/203 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1111JHN33/203 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1112FHN33/101 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1112FHN33/102 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |

**Table 1. Ordering information** *…continued*

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| LPC1112FHN33/201 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1112FHN33/202 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1112FHN24/202 | HVQFN24 | HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm | SOT616-3 |
| LPC1112FHI33/102 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm | n/a |
| LPC1112FHI33/202 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm | n/a |
| LPC1112FHI33/203 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm | n/a |
| LPC1112JHI33/203 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm | n/a |
| LPC1112FHN33/103 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1112JHN33/103 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1112JHN33/203 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1112FHN33/203 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1113FHN33/201 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1113FHN33/202 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1113FHN33/203 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1113JHN33/203 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1113FHN33/301 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1113FHN33/302 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1113FHN33/303 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1113JHN33/303 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1114FHN33/201 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1114FHN33/202 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1114FHN33/301 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |
| LPC1114FHN33/302 | HVQFN33 | HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm | n/a |




(1) LQFP48 and TFBGA48 only.

**Fig 2. LPC1100XL series block diagram**

**Table 5. LPC1100L series: LPC1112 pin description table (TSSOP20 with $V_{DDA}$ and $V_{SSA}$ pins)** *…continued*

| Symbol | Pin TSSOP20 | Start logic input | Type | Reset state [1] | Description |
|---|---|---|---|---|---|
| SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2 | 3 [3] | yes | I | I; PU | **SWCLK —** Serial wire clock. |
| | | | I/O | - | **PIO0_10 —** General purpose digital input/output pin. |
| | | | I/O | - | **SCK0 —** Serial clock for SPI0. |
| | | | O | - | **CT16B0_MAT2 —** Match output 2 for 16-bit timer 0. |
| R/PIO0_11/ AD0/CT32B0_MAT3 | 4 [4] | yes | I | I; PU | **R —** Reserved. Configure for an alternate function in the IOCONFIG block. |
| | | | I/O | - | **PIO0_11 —** General purpose digital input/output pin. |
| | | | I | - | **AD0 —** A/D converter, input 0. |
| | | | O | - | **CT32B0_MAT3 —** Match output 3 for 32-bit timer 0. |
| PIO1_0 to PIO1_7 | | | I/O | | **Port 1 —** Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block. |
| R/PIO1_0/ AD1/CT32B1_CAP0 | 7 [4] | yes | I | I; PU | **R —** Reserved. Configure for an alternate function in the IOCONFIG block. |
| | | | I/O | - | **PIO1_0 —** General purpose digital input/output pin. |
| | | | I | - | **AD1 —** A/D converter, input 1. |
| | | | I | - | **CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1. |
| R/PIO1_1/ AD2/CT32B1_MAT0 | 8 [4] | no | O | I; PU | **R —** Reserved. Configure for an alternate function in the IOCONFIG block. |
| | | | I/O | - | **PIO1_1 —** General purpose digital input/output pin. |
| | | | I | - | **AD2 —** A/D converter, input 2. |
| | | | O | - | **CT32B1_MAT0 —** Match output 0 for 32-bit timer 1. |
| R/PIO1_2/ AD3/CT32B1_MAT1 | 9 [4] | no | I | I; PU | **R —** Reserved. Configure for an alternate function in the IOCONFIG block. |
| | | | I/O | - | **PIO1_2 —** General purpose digital input/output pin. |
| | | | I | - | **AD3 —** A/D converter, input 3. |
| | | | O | - | **CT32B1_MAT1 —** Match output 1 for 32-bit timer 1. |
| SWDIO/PIO1_3/ AD4/CT32B1_MAT2 | 10 [4] | no | I/O | I; PU | **SWDIO —** Serial wire debug input/output. |
| | | | I/O | - | **PIO1_3 —** General purpose digital input/output pin. |
| | | | I | - | **AD4 —** A/D converter, input 4. |
| | | | O | - | **CT32B1_MAT2 —** Match output 2 for 32-bit timer 1. |
| PIO1_6/RXD/ CT32B0_MAT0 | 11 [3] | no | I/O | I; PU | **PIO1_6 —** General purpose digital input/output pin. |
| | | | I | - | **RXD —** Receiver input for UART. |
| | | | O | - | **CT32B0_MAT0 —** Match output 0 for 32-bit timer 0. |
| PIO1_7/TXD/ CT32B0_MAT1 | 12 [3] | no | I/O | I; PU | **PIO1_7 —** General purpose digital input/output pin. |
| | | | O | - | **TXD —** Transmitter output for UART. |
| | | | O | - | **CT32B0_MAT1 —** Match output 1 for 32-bit timer 0. |
| $V_{DD}$ | 15 | - | I | - | 3.3 V supply voltage to the internal regulator and the external rail. |

**Table 7. LPC1100L series: LPC1112/14 pin description table (TSSOP28 and DIP28 packages)** *…continued*

| Symbol | Pin TSSOP28/ DIP28 | Start logic input | Type | Reset state [1] | Description |
|---|---|---|---|---|---|
| SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2 | 3 [3] | yes | I | I; PU | **SWCLK —** Serial wire clock. |
| | | | I/O | - | **PIO0_10 —** General purpose digital input/output pin. |
| | | | I/O | - | **SCK0 —** Serial clock for SPI0. |
| | | | O | - | **CT16B0_MAT2 —** Match output 2 for 16-bit timer 0. |
| R/PIO0_11/ AD0/CT32B0_MAT3 | 4 [5] | yes | I | I; PU | **R —** Reserved. Configure for an alternate function in the IOCONFIG block. |
| | | | I/O | - | **PIO0_11 —** General purpose digital input/output pin. |
| | | | I | - | **AD0 —** A/D converter, input 0. |
| | | | O | - | **CT32B0_MAT3 —** Match output 3 for 32-bit timer 0. |
| PIO1_0 to PIO1_9 | | | I/O | | **Port 1 —** Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block. |
| R/PIO1_0/ AD1/CT32B1_CAP0 | 9 [5] | yes | I | I; PU | **R —** Reserved. Configure for an alternate function in the IOCONFIG block. |
| | | | I/O | - | **PIO1_0 —** General purpose digital input/output pin. |
| | | | I | - | **AD1 —** A/D converter, input 1. |
| | | | I | - | **CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1. |
| R/PIO1_1/ AD2/CT32B1_MAT0 | 10 [5] | no | O | I; PU | **R —** Reserved. Configure for an alternate function in the IOCONFIG block. |
| | | | I/O | - | **PIO1_1 —** General purpose digital input/output pin. |
| | | | I | - | **AD2 —** A/D converter, input 2. |
| | | | O | - | **CT32B1_MAT0 —** Match output 0 for 32-bit timer 1. |
| R/PIO1_2/ AD3/CT32B1_MAT1 | 11 [5] | no | I | I; PU | **R —** Reserved. Configure for an alternate function in the IOCONFIG block. |
| | | | I/O | - | **PIO1_2 —** General purpose digital input/output pin. |
| | | | I | - | **AD3 —** A/D converter, input 3. |
| | | | O | - | **CT32B1_MAT1 —** Match output 1 for 32-bit timer 1. |
| SWDIO/PIO1_3/ AD4/CT32B1_MAT2 | 12 [5] | no | I/O | I; PU | **SWDIO —** Serial wire debug input/output. |
| | | | I/O | - | **PIO1_3 —** General purpose digital input/output pin. |
| | | | I | - | **AD4 —** A/D converter, input 4. |
| | | | O | - | **CT32B1_MAT2 —** Match output 2 for 32-bit timer 1. |
| PIO1_4/AD5/ CT32B1_MAT3/ WAKEUP | 13 [5] | no | I/O | I; PU | **PIO1_4 —** General purpose digital input/output pin with 10 ns glitch filter. In Deep power-down mode, this pin serves as the Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part. |
| | | | I | - | **AD5 —** A/D converter, input 5. |
| | | | O | - | **CT32B1_MAT3 —** Match output 3 for 32-bit timer 1. |

**Table 7. LPC1100L series: LPC1112/14 pin description table (TSSOP28 and DIP28 packages)** *…continued*

| Symbol | Pin TSSOP28/ DIP28 | Start logic input | Type | Reset state [1] | Description |
|---|---|---|---|---|---|
| PIO1_5/$\overline{\text{RTS}}$/ CT32B0_CAP0 | 14 [3] | no | I/O | I; PU | **PIO1_5 —** General purpose digital input/output pin. |
| | | | O | - | **$\overline{\text{RTS}}$ —** Request To Send output for UART. |
| | | | I | - | **CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0. |
| PIO1_6/RXD/ CT32B0_MAT0 | 15 [3] | no | I/O | I; PU | **PIO1_6 —** General purpose digital input/output pin. |
| | | | I | - | **RXD —** Receiver input for UART. |
| | | | O | - | **CT32B0_MAT0 —** Match output 0 for 32-bit timer 0. |
| PIO1_7/TXD/ CT32B0_MAT1 | 16 [3] | no | I/O | I; PU | **PIO1_7 —** General purpose digital input/output pin. |
| | | | O | - | **TXD —** Transmitter output for UART. |
| | | | O | - | **CT32B0_MAT1 —** Match output 1 for 32-bit timer 0. |
| PIO1_8/ CT16B1_CAP0 | 17 [3] | no | I/O | I; PU | **PIO1_8 —** General purpose digital input/output pin. |
| | | | I | - | **CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1. |
| PIO1_9/ CT16B1_MAT0 | 18 [3] | no | I/O | I; PU | **PIO1_9 —** General purpose digital input/output pin. |
| | | | O | - | **CT16B1_MAT0 —** Match output 0 for 16-bit timer 1. |
| $V_{DD}$ | 21 | - | | - | 3.3 V supply voltage to the internal regulator and the external rail. |
| $V_{DDA}$ | 7 | - | - | - | 3.3 V supply voltage to the ADC. Also used as the ADC reference voltage. |
| XTALIN | 20 [6] | - | I | - | Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V. |
| XTALOUT | 19 [6] | - | O | - | Output from the oscillator amplifier. |
| $V_{SS}$ | 22 | - | | - | Ground. |
| $V_{SSA}$ | 8 | - | - | - | Analog ground. |

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to full $V_{DD}$ level ); IA = inactive, no pull-up/down enabled.

[2] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See Figure 52 for the reset pad configuration.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 51).

[4] $I^2C$-bus pads compliant with the $I^2C$-bus specification for $I^2C$ standard mode and $I^2C$ Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 51).

[6] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

**Table 9. LPC1100 and LPC1100L series: LPC1111/12/13/14 pin description table (HVQFN33 package)** *…continued*

| Symbol | Pin | Start logic input | Type | Reset state [1] | Description |
|---|---|---|---|---|---|
| PIO1_7/TXD/ CT32B0_MAT1 | 32[3] | no | I/O | I;PU | **PIO1_7 —** General purpose digital input/output pin. |
| | | | O | - | **TXD —** Transmitter output for UART. |
| | | | O | - | **CT32B0_MAT1 —** Match output 1 for 32-bit timer 0. |
| PIO1_8/ CT16B1_CAP0 | 7[3] | no | I/O | I;PU | **PIO1_8 —** General purpose digital input/output pin. |
| | | | I | - | **CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1. |
| PIO1_9/ CT16B1_MAT0 | 12[3] | no | I/O | I;PU | **PIO1_9 —** General purpose digital input/output pin. |
| | | | O | - | **CT16B1_MAT0 —** Match output 0 for 16-bit timer 1. |
| PIO1_10/AD6/ CT16B1_MAT1 | 20[5] | no | I/O | I;PU | **PIO1_10 —** General purpose digital input/output pin. |
| | | | I | - | **AD6 —** A/D converter, input 6. |
| | | | O | - | **CT16B1_MAT1 —** Match output 1 for 16-bit timer 1. |
| PIO1_11/AD7 | 27[5] | no | I/O | I;PU | **PIO1_11 —** General purpose digital input/output pin. |
| | | | I | - | **AD7 —** A/D converter, input 7. |
| PIO2_0 | | | | | **Port 2 —** Port 2 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 2 pins depends on the function selected through the IOCONFIG register block. Pins PIO2_1 to PIO2_11 are not available. |
| PIO2_0/$\overline{\text{DTR}}$ | 1[3] | no | I/O | I;PU | **PIO2_0 —** General purpose digital input/output pin. |
| | | | O | - | **$\overline{\text{DTR}}$ —** Data Terminal Ready output for UART. |
| PIO3_0 to PIO3_5 | | | | | **Port 3 —** Port 3 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 3 pins depends on the function selected through the IOCONFIG register block. Pins PIO3_0, PIO3_1, PIO3_3 and PIO3_6 to PIO3_11 are not available. |
| PIO3_2 | 28[3] | no | I/O | I;PU | **PIO3_2 —** General purpose digital input/output pin. |
| PIO3_4 | 13[3] | no | I/O | I;PU | **PIO3_4 —** General purpose digital input/output pin. |
| PIO3_5 | 14[3] | no | I/O | I;PU | **PIO3_5 —** General purpose digital input/output pin. |
| $V_{DD}$ | 6; 29 | - | I | - | 3.3 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage. |
| XTALIN | 4[6] | - | I | - | Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V. |
| XTALOUT | 5[6] | - | O | - | Output from the oscillator amplifier. |
| $V_{SS}$ | 33 | - | - | - | Thermal pad. Connect to ground. |

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to 2.6 V for LPC111x/101/201/301, pins pulled up to full $V_{DD}$ level on LPC111x/002/102/202/302 ($V_{DD}$ = 3.3 V)); IA = inactive, no pull-up/down enabled.

[2] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See Figure 52 for the reset pad configuration.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 51).

[4] $I^2C$-bus pads compliant with the $I^2C$-bus specification for $I^2C$ standard mode and $I^2C$ Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled, and the pin is not 5 V tolerant (see Figure 51).

**Table 11. LPC1100XL series: LPC1111/12/13/14 pin description table (HVQFN33 package)** *…continued*

| Symbol | Pin | Start logic input | Type | Reset state [1] | Description |
|---|---|---|---|---|---|
| $V_{DD}$ | 6; 29 | - | I | - | 3.3 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage. |
| XTALIN | 4[6] | - | I | - | Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V. |
| XTALOUT | 5[6] | - | O | - | Output from the oscillator amplifier. |
| $V_{SS}$ | 33 | - | - | - | Thermal pad. Connect to ground. |

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to full $V_{DD}$ level ($V_{DD}$ = 3.3 V)); IA = inactive, no pull-up/down enabled.

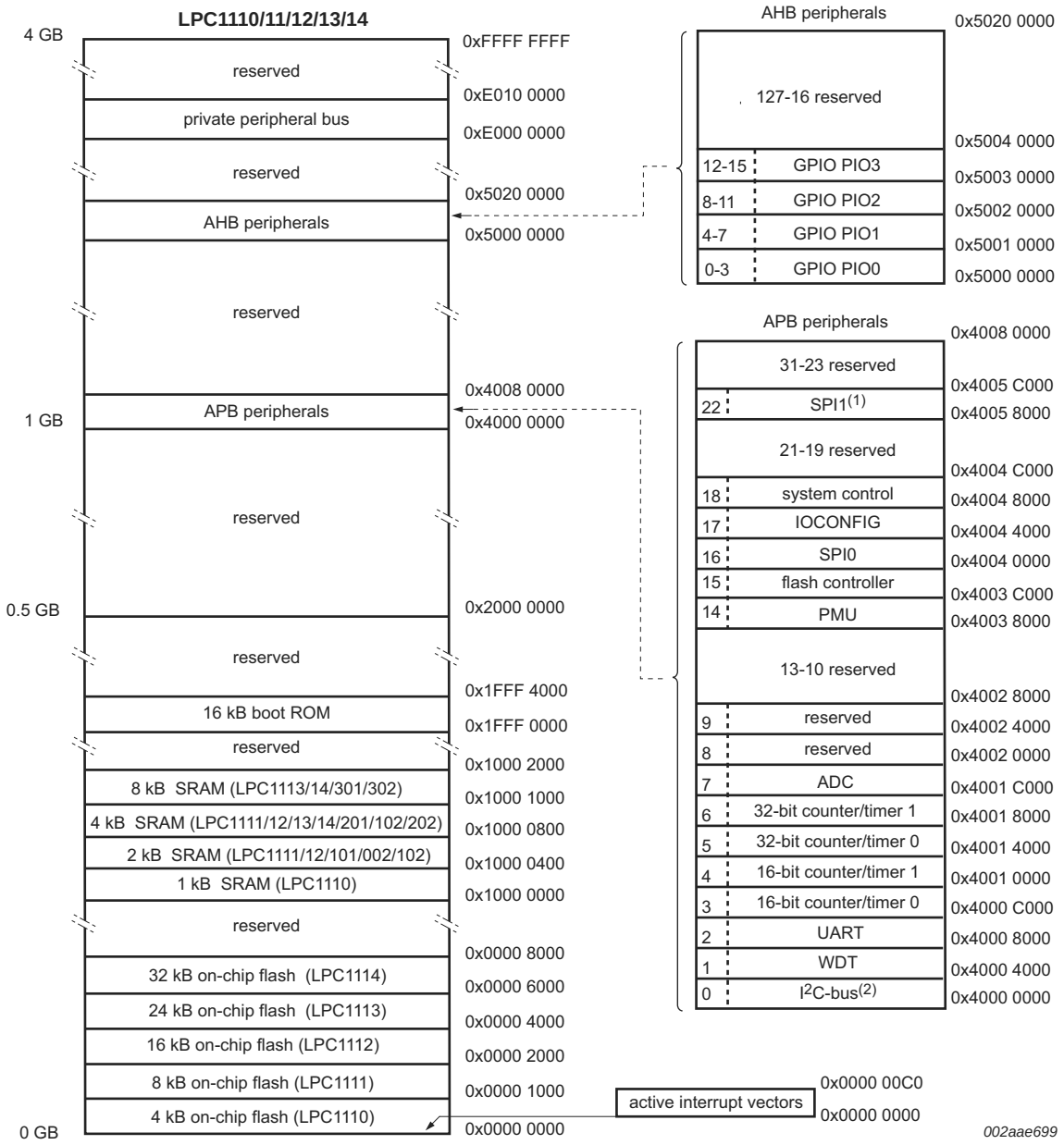
[2] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See Figure 52 for the reset pad configuration.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 51).

[4] $I^2C$-bus pads compliant with the $I^2C$-bus specification for $I^2C$ standard mode and $I^2C$ Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled, and the pin is not 5 V tolerant (see Figure 51).

[6] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.




(1) LQFP48 package only.

(1) Not on part LPC1112FDH20/102.

**Fig 14. LPC1100 and LPC1100L series memory map**

- On the LPC1100L and LPC1100XL series, all GPIO pins (except PIO0_4 and PIO0_5) are pulled up to 3.3 V ($V_{DD}$ = 3.3 V) if their pull-up resistor is enabled in the IOCONFIG block.
- Programmable open-drain mode for series LPC1100L and LPC1100XL.

## 7.8 UART

The LPC1110/11/12/13/14/15 contain one UART.

Support for RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The UART includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

### 7.8.1 Features

- Maximum UART data bit rate of 3.125 MBit/s.
- 16 Byte Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Support for modem control.

## 7.9 SPI serial I/O controller

The LPC1100 and LPC1100L series contain two SPI controllers on the LQFP48 package and one SPI controller on the HVQFN33/TSSOP28/DIP28/TSSOP20/SO20 packages (SPI0).

The LPC1100XL series contain two SPI controllers.

Both SPI controllers support SSP features.

The SPI controller is capable of operation on a SSP, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SPI supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

### 7.9.1 Features

- Maximum SPI speed of 25 Mbit/s (master) or 4.17 Mbit/s (slave) (in SSP mode)
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

#### 7.16.5.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

#### 7.16.5.3 Deep-sleep mode

In Deep-sleep mode, the chip is in Sleep mode, and in addition all analog blocks are shut down. As an exception, the user has the option to keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection. Deep-sleep mode allows for additional power savings.

Up to 13 pins total serve as external wake-up pins to the start logic to wake up the chip from Deep-sleep mode.

Unless the watchdog oscillator is selected to run in Deep-sleep mode, the clock source should be switched to IRC before entering Deep-sleep mode, because the IRC can be switched on and off glitch-free.

#### 7.16.5.4 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip with the exception of the WAKEUP pin. The LPC1110/11/12/13/14/15 can wake up from Deep power-down mode via the WAKEUP pin.

A LOW-going pulse as short as 50 ns wakes up the part from Deep power-down mode.

When entering Deep power-down mode, an external pull-up resistor is required on the WAKEUP pin to hold it HIGH. The $\overline{\text{RESET}}$ pin must also be held HIGH to prevent it from floating while in Deep power-down mode.

## 7.17 System control

### 7.17.1 Start logic

The start logic connects external pins to corresponding interrupts in the NVIC. Each pin shown in Table 8 to Table 9 as input to the start logic has an individual interrupt in the NVIC interrupt vector table. The start logic pins can serve as external interrupt pins when the chip is running. In addition, an input signal on the start logic pins can wake up the chip from Deep-sleep mode when all clocks are shut down.

**Table 17. Static characteristics (LPC1100XL series)** *…continued*
*$T_{amb}$ = −40 °C to +105 °C, unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | LOW-level input voltage | | - | - | $0.3V_{DD}$ | V |
| $V_{hys}$ | hysteresis voltage | | - | 0.4 | - | V |
| $V_{OH}$ | HIGH-level output voltage | 2.5 V ≤ $V_{DD}$ ≤ 3.6 V; $I_{OH}$ = −4 mA | $V_{DD}$ − 0.4 | - | - | V |
| | | 1.8 V ≤ $V_{DD}$ < 2.5 V; $I_{OH}$ = −3 mA | $V_{DD}$ − 0.4 | - | - | V |
| $V_{OL}$ | LOW-level output voltage | 2.5 V ≤ $V_{DD}$ ≤ 3.6 V; $I_{OL}$ = 4 mA | - | - | 0.4 | V |
| | | 1.8 V ≤ $V_{DD}$ < 2.5 V; $I_{OL}$ = 3 mA | - | - | 0.4 | V |
| $I_{OH}$ | HIGH-level output current | $V_{OH}$ = $V_{DD}$ − 0.4 V; 2.5 V ≤ $V_{DD}$ ≤ 3.6 V | −4 | - | - | mA |
| | | 1.8 V ≤ $V_{DD}$ < 2.5 V | −3 | - | - | mA |
| $I_{OL}$ | LOW-level output current | $V_{OL}$ = 0.4 V 2.5 V ≤ $V_{DD}$ ≤ 3.6 V | 4 | - | - | mA |
| | | 1.8 V ≤ $V_{DD}$ < 2.5 V | 3 | - | - | mA |
| $I_{OHS}$ | HIGH-level short-circuit output current | $V_{OH}$ = 0 V [16] | - | - | −45 | mA |
| $I_{OLS}$ | LOW-level short-circuit output current | $V_{OL}$ = $V_{DD}$ [16] | - | - | 50 | mA |
| $I_{pd}$ | pull-down current | $V_I$ = 5 V | 10 | 50 | 150 | µA |
| $I_{pu}$ | pull-up current | $V_I$ = 0 V; 2.0 V ≤ $V_{DD}$ ≤ 3.6 V | −15 | −50 | −85 | µA |
| | | 1.8 V ≤ $V_{DD}$ < 2.0 V | −10 | −50 | −85 | µA |
| | | $V_{DD}$ < $V_I$ < 5 V | 0 | 0 | 0 | µA |
| **High-drive output pin (PIO0_7)** | | | | | | |
| $I_{IL}$ | LOW-level input current | $V_I$ = 0 V; on-chip pull-up resistor disabled | - | 0.5 | 10 | nA |
| $I_{IH}$ | HIGH-level input current | $V_I$ = $V_{DD}$; on-chip pull-down resistor disabled | - | 0.5 | 10 | nA |
| $I_{OZ}$ | OFF-state output current | $V_O$ = 0 V; $V_O$ = $V_{DD}$; on-chip pull-up/down resistors disabled | - | 0.5 | 10 | nA |
| $V_I$ | input voltage | pin configured to provide a digital function [13][14][15] | 0 | - | 5.0 | V |
| $V_O$ | output voltage | output active | 0 | - | $V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | $0.7V_{DD}$ | - | - | V |
| $V_{IL}$ | LOW-level input voltage | | - | - | $0.3V_{DD}$ | V |
| $V_{hys}$ | hysteresis voltage | | 0.4 | - | - | V |

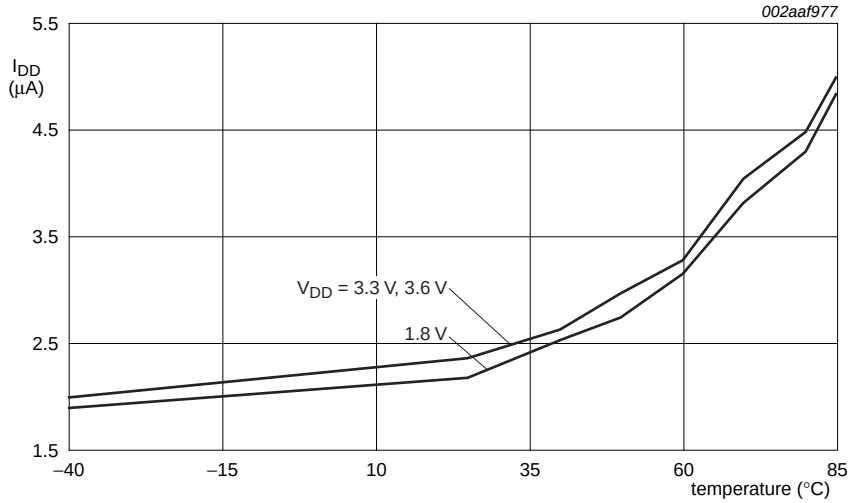
## 10.4 BOD static characteristics

**Table 19. BOD static characteristics[1]**

$T_{amb}$ = 25 °C.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{th}$ | threshold voltage | interrupt level 1 | | | | |
| | | assertion | - | 2.22 | - | V |
| | | de-assertion | - | 2.35 | - | V |
| | | interrupt level 2 | | | | |
| | | assertion | - | 2.52 | - | V |
| | | de-assertion | - | 2.66 | - | V |
| | | interrupt level 3 | | | | |
| | | assertion | - | 2.80 | - | V |
| | | de-assertion | - | 2.90 | - | V |
| | | reset level 0 | | | | |
| | | assertion | - | 1.46 | - | V |
| | | de-assertion | - | 1.63 | - | V |
| | | reset level 1 | | | | |
| | | assertion | - | 2.06 | - | V |
| | | de-assertion | - | 2.15 | - | V |
| | | reset level 2 | | | | |
| | | assertion | - | 2.35 | - | V |
| | | de-assertion | - | 2.43 | - | V |
| | | reset level 3 | | | | |
| | | assertion | - | 2.63 | - | V |
| | | de-assertion | - | 2.71 | - | V |

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *LPC111x user manual*.




Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

**Fig 26. Deep-sleep mode: Typical supply current $I_{DD}$ versus temperature for different supply voltages $V_{DD}$ (for LPC111x/002/102/202/302)**

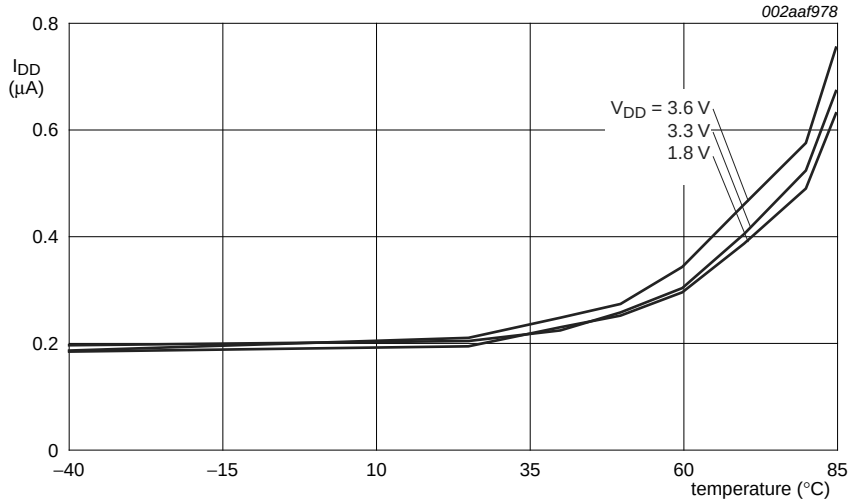
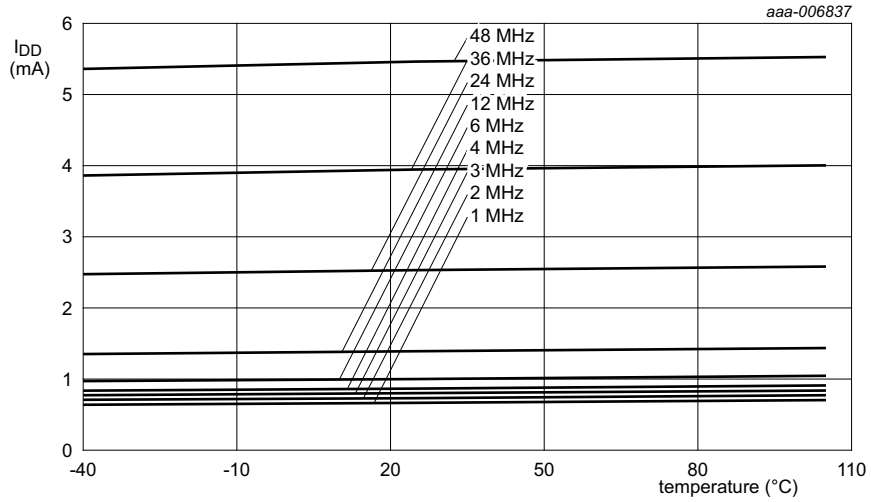



**Fig 27. Deep power-down mode: Typical supply current $I_{DD}$ versus temperature for different supply voltages $V_{DD}$ (for LPC111x/002/102/202/302)**



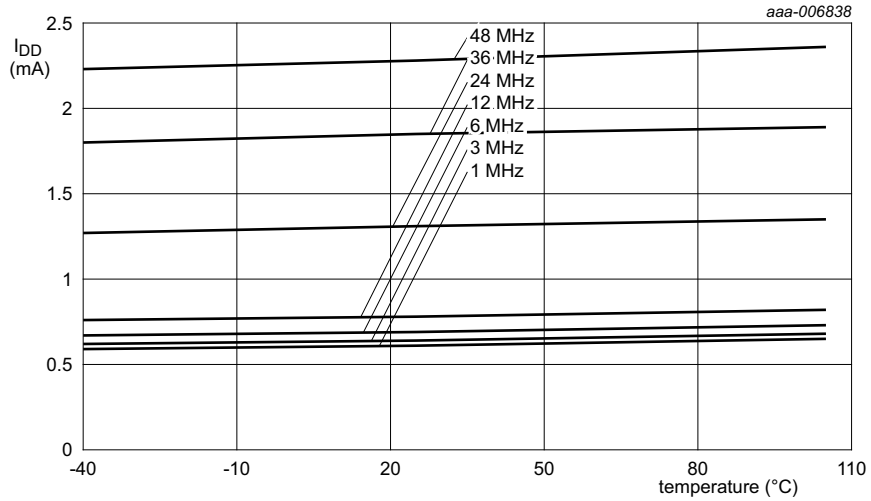

Conditions: $V_{DD}$ = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz to 6 MHz: system oscillator enabled; PLL, IRC disabled.

12 MHz: IRC enabled; system oscillator, PLL disabled.

24 MHz to 48 MHz: IRC disabled; system oscillator, PLL enabled.

**Fig 29. Active mode: Typical supply current $I_{DD}$ versus temperature for different system clock frequencies (for LPC111xXL)**




Conditions: $V_{DD}$ = 3.3 V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz to 6 MHz: system oscillator enabled; PLL, IRC disabled.

12 MHz: IRC enabled; system oscillator, PLL disabled.

24 MHz to 48 MHz: IRC disabled; system oscillator, PLL enabled.

**Fig 30. Sleep mode: Typical supply current $I_{DD}$ versus temperature for different system clock frequencies (for LPC111xXL)**

## 10.9 Peripheral power consumption

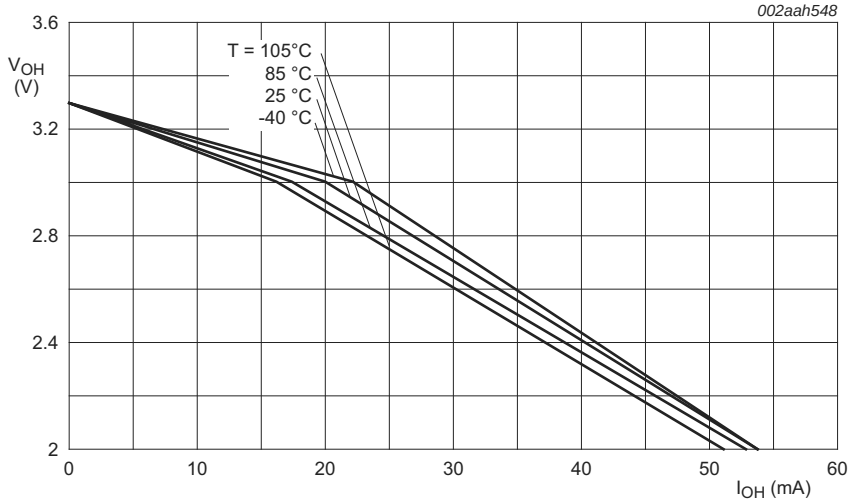
The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at $T_{amb}$ = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 48 MHz.

**Table 21. Power consumption for individual analog and digital blocks**

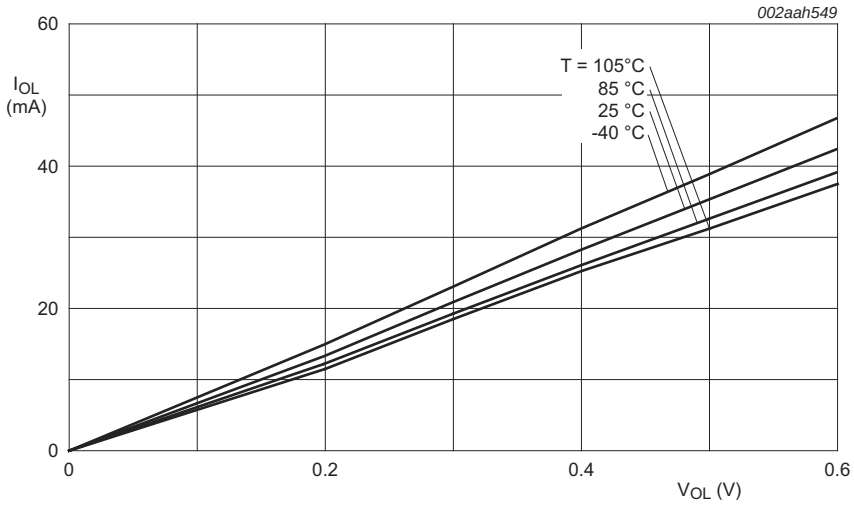
| Peripheral | Typical supply current in mA | | | Notes |
|---|---|---|---|---|
| | n/a | 12 MHz | 48 MHz | |
| IRC | 0.27 | - | - | System oscillator running; PLL off; independent of main clock frequency. |
| System oscillator at 12 MHz | 0.22 | - | - | IRC running; PLL off; independent of main clock frequency. |
| Watchdog oscillator at 500 kHz/2 | 0.004 | - | - | System oscillator running; PLL off; independent of main clock frequency. |
| BOD | 0.051 | - | - | Independent of main clock frequency. |
| Main PLL | - | 0.21 | - | |
| ADC | - | 0.08 | 0.29 | |
| CLKOUT | - | 0.12 | 0.47 | Main clock divided by 4 in the CLKOUTDIV register. |
| CT16B0 | - | 0.02 | 0.06 | |
| CT16B1 | - | 0.02 | 0.06 | |
| CT32B0 | - | 0.02 | 0.07 | |
| CT32B1 | - | 0.02 | 0.06 | |
| GPIO | - | 0.23 | 0.88 | GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register. |
| IOCONFIG | - | 0.03 | 0.10 | |
| I2C | - | 0.04 | 0.13 | |
| ROM | - | 0.04 | 0.15 | |
| SPI0 | - | 0.12 | 0.45 | |
| SPI1 | - | 0.12 | 0.45 | |
| UART | - | 0.22 | 0.82 | |
| WDT/WWDT | - | 0.02 | 0.06 | Main clock selected as clock source for the WDT. |

## 10.10 Electrical pin characteristics



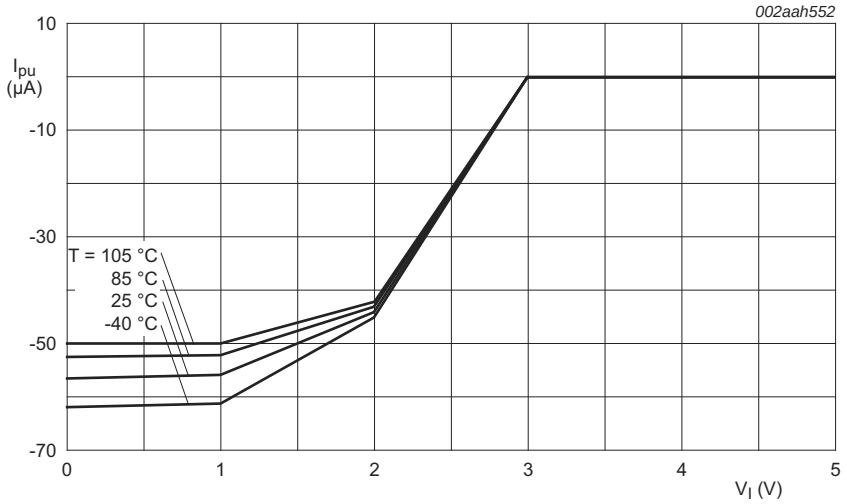

Conditions: $V_{DD}$ = 3.3 V; on pin PIO0_7.

**Fig 36. High-drive output: Typical HIGH-level output voltage $V_{OH}$ versus HIGH-level output current $I_{OH}$.**



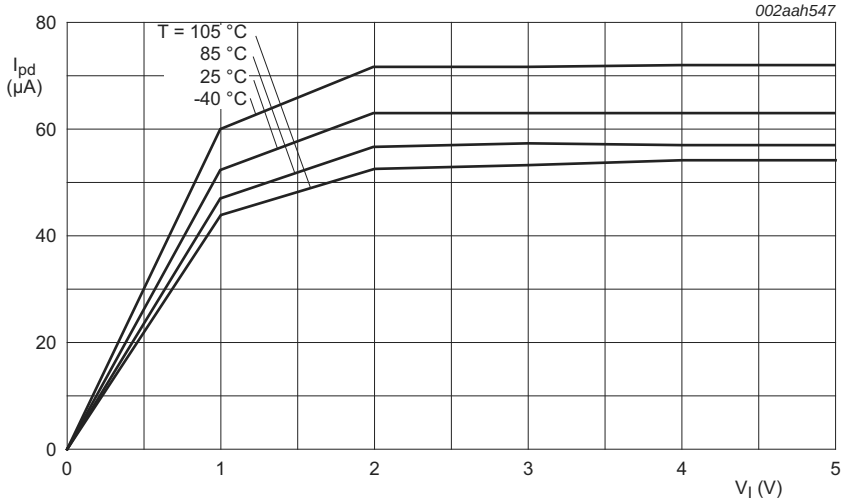

Conditions: $V_{DD}$ = 3.3 V; on pins PIO0_4 and PIO0_5.

**Fig 37. $I^2C$-bus pins (high current sink): Typical LOW-level output current $I_{OL}$ versus LOW-level output voltage $V_{OL}$**




Conditions: $V_{DD}$ = 3.3 V; standard port pins.

**Fig 40. Typical pull-up current $I_{pu}$ versus input voltage $V_I$**




Conditions: $V_{DD}$ = 3.3 V; standard port pins.

**Fig 41. Typical pull-down current $I_{pd}$ versus input voltage $V_I$**

## 12.4 XTAL Printed Circuit Board (PCB) layout guidelines

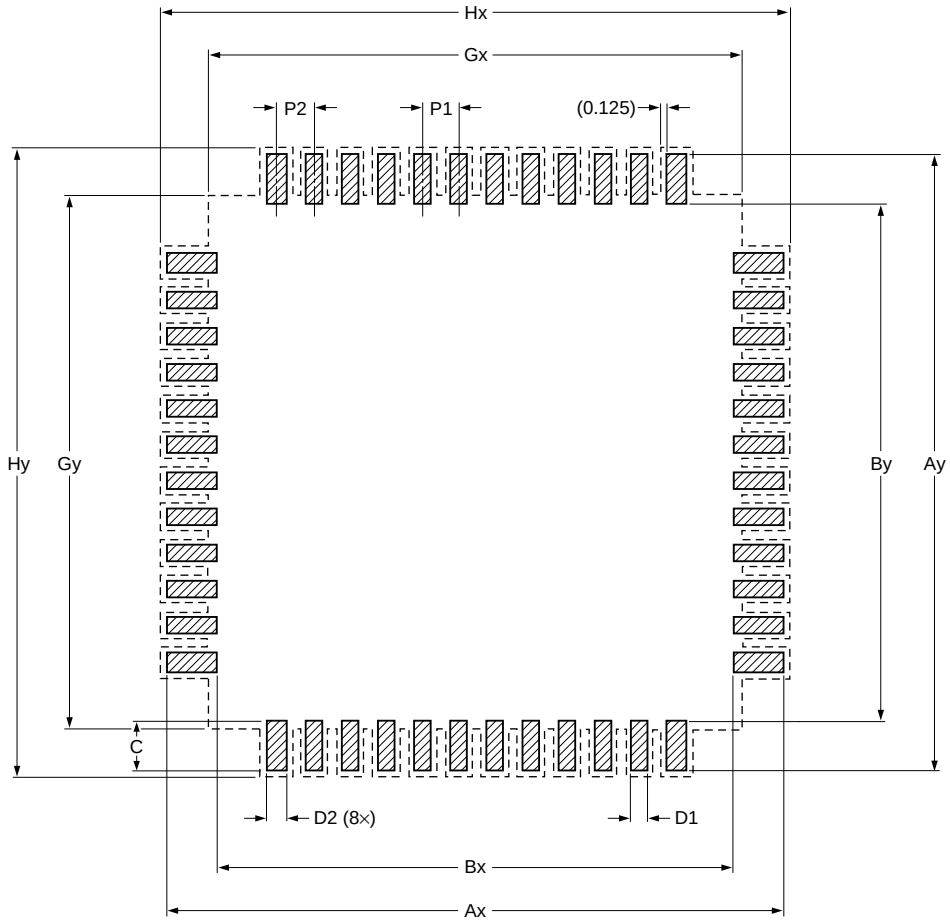
The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors $C_{X1}$, $C_{X2}$, and $C_{X3}$ in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of $C_{X1}$ and $C_{X2}$ should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

## 12.5 Standard I/O pad configuration

Figure 51 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital output: Pseudo open-drain mode enable/disabled
- Analog input

**Footprint information for reflow soldering of LQFP48 package** **SOT313-2**




Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

| P1 | P2 | Ax | Ay | Bx | By | C | D1 | D2 | Gx | Gy | Hx | Hy |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.500 | 0.560 | 10.350 | 10.350 | 7.350 | 7.350 | 1.500 | 0.280 | 0.500 | 7.500 | 7.500 | 10.650 | 10.650 |

*sot313-2_fr*

**Fig 69. Reflow soldering of the LQFP48 package**