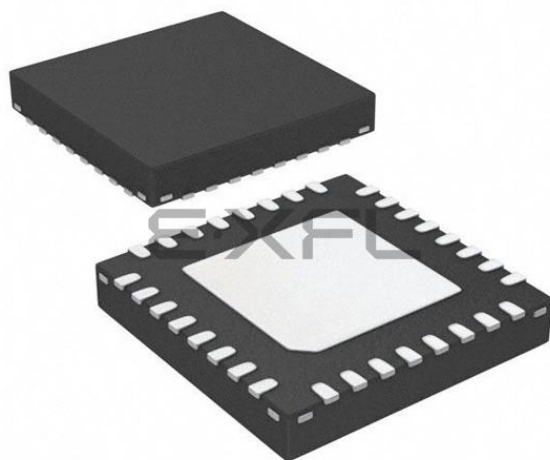




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Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	28
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VQFN Exposed Pad
Supplier Device Package	32-HVQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1113fhn33-201-5

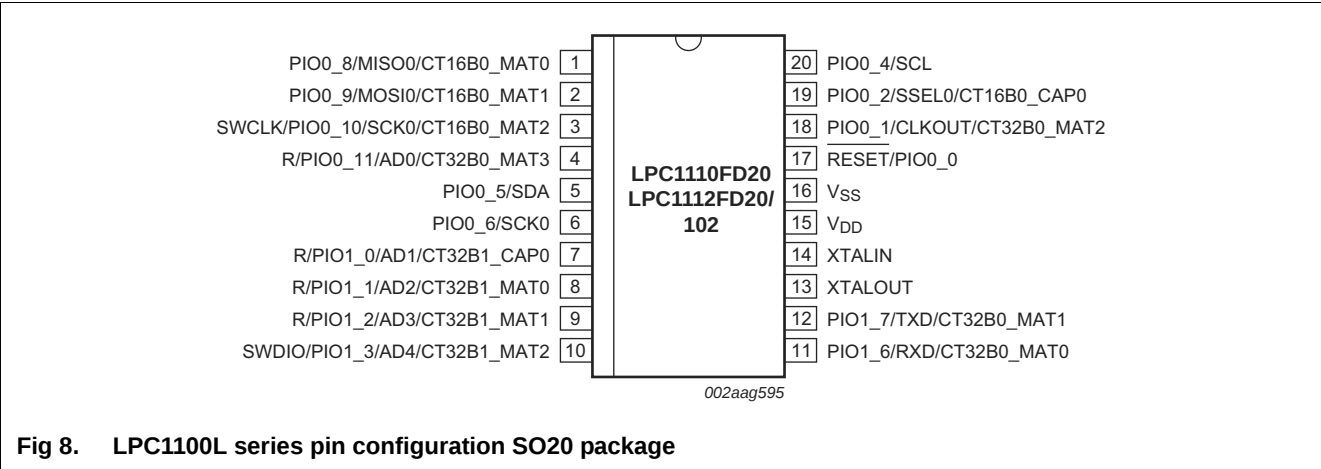
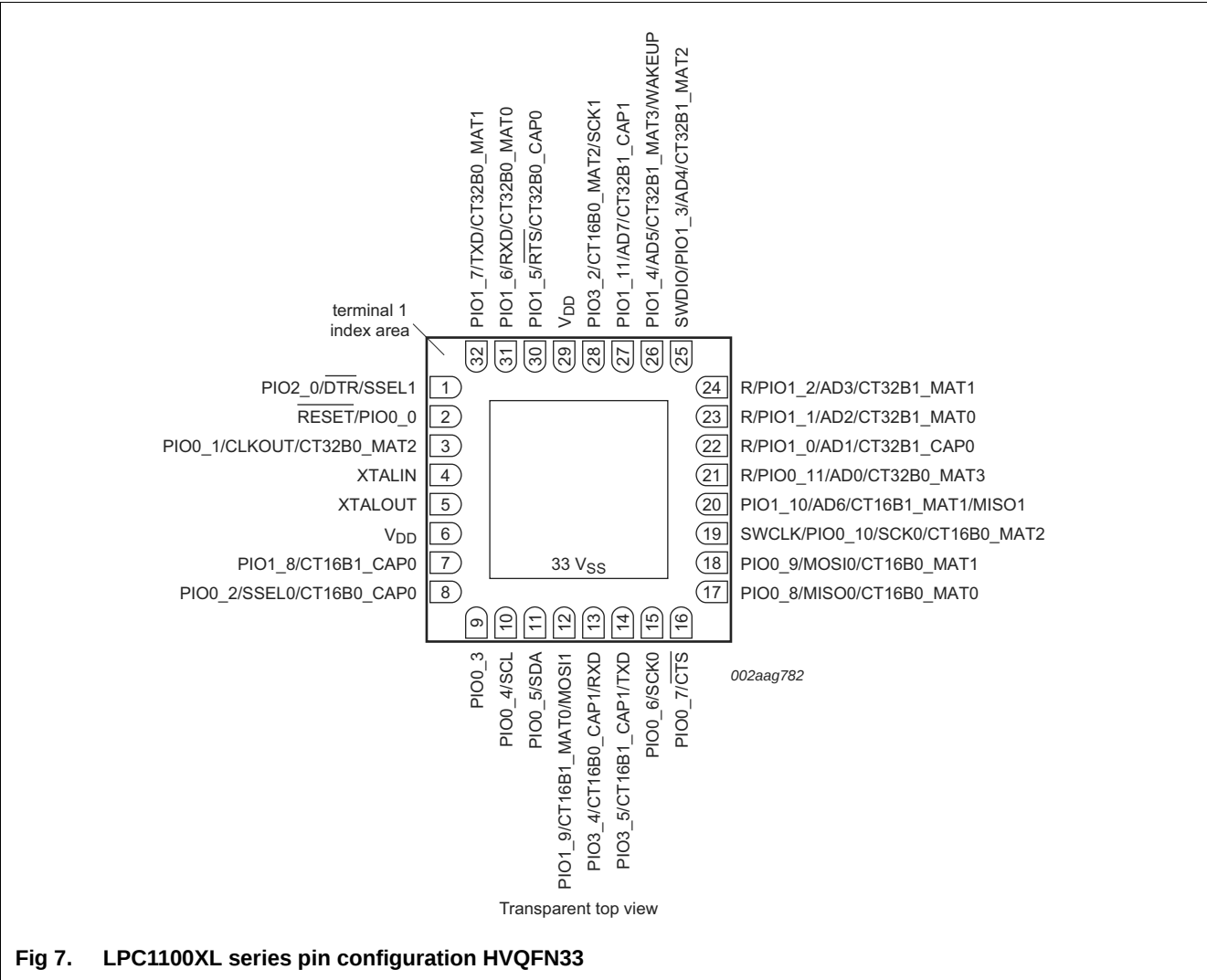
Table 1. Ordering information ...continued

Type number	Package		
	Name	Description	Version
LPC1115JBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1115FET48/303	TFBGA48	plastic thin fine-pitch ball grid array package; 48 balls; body 4.5 × 4.5 × 0.7 mm	SOT1155-2
LPC1115JET48/303	TFBGA48	plastic thin fine-pitch ball grid array package; 48 balls; body 4.5 × 4.5 × 0.7 mm	SOT1155-2

4.1 Ordering options

Table 2. Ordering options

Type number	Series	Flash	Total SRAM	Power profiles	UART	I ² C/ Fast+	SPI	ADC channel	GPIO	Package	Temp ^[1]
LPC1110											
LPC1110FD20	LPC1100L	4 kB	1 kB	yes	1	1	1	5	16	SO20	F
LPC1111											
LPC1111FDH20/002	LPC1100L	8 kB	2 kB	yes	1	1	1	5	16	TSSOP20	F
LPC1111FHN33/101	LPC1100	8 kB	2 kB	no	1	1	1	8	28	HVQFN33	F
LPC1111FHN33/102	LPC1100L	8 kB	2 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1111FHN33/103	LPC1100XL	8 kB	2 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1111JHN33/103	LPC1100XL	8 kB	2 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1111FHN33/201	LPC1100	8 kB	4 kB	no	1	1	1	8	28	HVQFN33	F
LPC1111FHN33/202	LPC1100L	8 kB	4 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1111FHN33/203	LPC1100XL	8 kB	4 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1111JHN33/203	LPC1100XL	8 kB	4 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1112											
LPC1112FD20/102	LPC1100L	16 kB	4 kB	yes	1	1	1	5	16	SO20	F
LPC1112FDH20/102	LPC1100L	16 kB	4 kB	yes	1	-	1	5	14	TSSOP20	F
LPC1112FDH28/102	LPC1100L	16 kB	4 kB	yes	1	1	1	6	22	TSSOP28	F
LPC1112FHN24/202	LPC1100L	16 kB	4 kB	yes	1	1	1	6	19	HVQFN24	F
LPC1112FHN33/101	LPC1100	16 kB	2 kB	no	1	1	1	8	28	HVQFN33	F
LPC1112FHN33/102	LPC1100L	16 kB	2 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1112FHN33/103	LPC1100XL	16 kB	2 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1112JHN33/103	LPC1100XL	16 kB	2 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1112FHN33/201	LPC1100	16 kB	4 kB	no	1	1	1	8	28	HVQFN33	F
LPC1112FHN33/202	LPC1100L	16 kB	4 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1112FHN33/203	LPC1100XL	16 kB	4 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1112JHN33/203	LPC1100XL	16 kB	4 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1112FHI33/102	LPC1100L	16 kB	2 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1112FHI33/202	LPC1100L	16 kB	4 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1112FHI33/203	LPC1100XL	16 kB	4 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1112JHI33/203	LPC1100XL	16 kB	4 kB	yes	1	1	2	8	28	HVQFN33	J



6.2 Pin description

Table 4. LPC1100L series: LPC1110/11/12 pin description table (SO20 and TSSOP20 package with I²C-bus pins)

Symbol	Pin SO20/ TSSOP20	Start logic input	Type	Reset state [1]	Description
PIO0_0 to PIO0_11			I/O		Port 0 — Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.
RESET/PIO0_0	17 [2]	yes	I	I; PU	RESET — External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The RESET pin can be left unconnected or be used as a GPIO pin if an external RESET function is not needed and Deep power-down mode is not used.
			I/O	-	PIO0_0 — General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/ CT32B0_MAT2	18 [3]	yes	I/O	I; PU	PIO0_1 — General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
			O	-	CLKOUT — Clockout pin.
			O	-	CT32B0_MAT2 — Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	19 [3]	yes	I/O	I; PU	PIO0_2 — General purpose digital input/output pin.
			I/O	-	SSEL0 — Slave Select for SPI0.
			I	-	CT16B0_CAP0 — Capture input 0 for 16-bit timer 0.
PIO0_4/SCL	20 [4]	yes	I/O	I; IA	PIO0_4 — General purpose digital input/output pin (open-drain).
			I/O	-	SCL — I ² C-bus, open-drain clock input/output. High-current sink only if I ² C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	5 [4]	yes	I/O	I; IA	PIO0_5 — General purpose digital input/output pin (open-drain).
			I/O	-	SDA — I ² C-bus, open-drain data input/output. High-current sink only if I ² C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	6 [3]	yes	I/O	I; PU	PIO0_6 — General purpose digital input/output pin.
			I/O	-	SCK0 — Serial clock for SPI0.
PIO0_8/MISO0/ CT16B0_MAT0	1 [3]	yes	I/O	I; PU	PIO0_8 — General purpose digital input/output pin.
			I/O	-	MISO0 — Master In Slave Out for SPI0.
			O	-	CT16B0_MAT0 — Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	2 [3]	yes	I/O	I; PU	PIO0_9 — General purpose digital input/output pin.
			I/O	-	MOSI0 — Master Out Slave In for SPI0.
			O	-	CT16B0_MAT1 — Match output 1 for 16-bit timer 0.
SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2	3 [3]	yes	I	I; PU	SWCLK — Serial wire clock.
			I/O	-	PIO0_10 — General purpose digital input/output pin.
			I/O	-	SCK0 — Serial clock for SPI0.
			O	-	CT16B0_MAT2 — Match output 2 for 16-bit timer 0.

Table 10. LPC1100XL series: LPC1113/14/15 pin description table (LQFP48 and TFBGA48 package) ...continued

Symbol	LQFP48	TFBGA48	Start logic input	Type	Reset state [1]	Description
PIO0_8/MISO0/ CT16B0_MAT0	27 ^[3]	F8 ^[3]	yes	I/O	I; PU	PIO0_8 — General purpose digital input/output pin.
				I/O	-	MISO0 — Master In Slave Out for SPI0.
				O	-	CT16B0_MAT0 — Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	28 ^[3]	F7 ^[3]	yes	I/O	I; PU	PIO0_9 — General purpose digital input/output pin.
				I/O	-	MOSI0 — Master Out Slave In for SPI0.
				O	-	CT16B0_MAT1 — Match output 1 for 16-bit timer 0.
SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2	29 ^[3]	E7 ^[3]	yes	I	I; PU	SWCLK — Serial wire clock.
				I/O	-	PIO0_10 — General purpose digital input/output pin.
				I/O	-	SCK0 — Serial clock for SPI0.
				O	-	CT16B0_MAT2 — Match output 2 for 16-bit timer 0.
R/PIO0_11/ AD0/CT32B0_MAT3	32 ^[5]	D8 ^[5]	yes	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
				I/O	-	PIO0_11 — General purpose digital input/output pin.
				I	-	AD0 — A/D converter, input 0.
				O	-	CT32B0_MAT3 — Match output 3 for 32-bit timer 0.
PIO1_0 to PIO1_11				I/O		Port 1 — Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block.
R/PIO1_0/ AD1/CT32B1_CAP0	33 ^[5]	C7 ^[5]	yes	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
				I/O	-	PIO1_0 — General purpose digital input/output pin.
				I	-	AD1 — A/D converter, input 1.
				I	-	CT32B1_CAP0 — Capture input 0 for 32-bit timer 1.
R/PIO1_1/ AD2/CT32B1_MAT0	34 ^[5]	C8 ^[5]	no	O	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
				I/O	-	PIO1_1 — General purpose digital input/output pin.
				I	-	AD2 — A/D converter, input 2.
				O	-	CT32B1_MAT0 — Match output 0 for 32-bit timer 1.
R/PIO1_2/ AD3/CT32B1_MAT1	35 ^[5]	B7 ^[5]	no	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
				I/O	-	PIO1_2 — General purpose digital input/output pin.
				I	-	AD3 — A/D converter, input 3.
				O	-	CT32B1_MAT1 — Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ AD4/CT32B1_MAT2	39 ^[5]	B6 ^[5]	no	I/O	I; PU	SWDIO — Serial wire debug input/output.
				I/O	-	PIO1_3 — General purpose digital input/output pin.
				I	-	AD4 — A/D converter, input 4.
				O	-	CT32B1_MAT2 — Match output 2 for 32-bit timer 1.

Table 11. LPC1100XL series: LPC1111/12/13/14 pin description table (HVQFN33 package)

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO0_0 to PIO0_11					Port 0 — Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.
RESET/PIO0_0	2[2]	yes	I	I;PU	RESET — External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The RESET pin can be left unconnected or be used as a GPIO pin if an external RESET function is not needed and Deep power-down mode is not used.
			I/O	-	PIO0_0 — General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/CT32B0_MAT2	3[3]	yes	I/O	I;PU	PIO0_1 — General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
			O	-	CLKOUT — Clock out pin.
			O	-	CT32B0_MAT2 — Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/CT16B0_CAP0	8[3]	yes	I/O	I;PU	PIO0_2 — General purpose digital input/output pin.
			I/O	-	SSEL0 — Slave select for SPI0.
			I	-	CT16B0_CAP0 — Capture input 0 for 16-bit timer 0.
PIO0_3	9[3]	yes	I/O	I;PU	PIO0_3 — General purpose digital input/output pin.
PIO0_4/SCL	10[4]	yes	I/O	I;IA	PIO0_4 — General purpose digital input/output pin (open-drain).
			I/O	-	SCL — I ² C-bus, open-drain clock input/output. High-current sink only if I ² C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	11[4]	yes	I/O	I;IA	PIO0_5 — General purpose digital input/output pin (open-drain).
			I/O	-	SDA — I ² C-bus, open-drain data input/output. High-current sink only if I ² C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	15[3]	yes	I/O	I;PU	PIO0_6 — General purpose digital input/output pin.
			I/O	-	SCK0 — Serial clock for SPI0.
PIO0_7/CTS	16[3]	yes	I/O	I;PU	PIO0_7 — General purpose digital input/output pin (high-current output driver).
			I	-	CTS — Clear To Send input for UART.
PIO0_8/MISO0/CT16B0_MAT0	17[3]	yes	I/O	I;PU	PIO0_8 — General purpose digital input/output pin.
			I/O	-	MISO0 — Master In Slave Out for SPI0.
			O	-	CT16B0_MAT0 — Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/CT16B0_MAT1	18[3]	yes	I/O	I;PU	PIO0_9 — General purpose digital input/output pin.
			I/O	-	MOSI0 — Master Out Slave In for SPI0.
			O	-	CT16B0_MAT1 — Match output 1 for 16-bit timer 0.
SWCLK/PIO0_10/SCK0/CT16B0_MAT2	19[3]	yes	I	I;PU	SWCLK — Serial wire clock.
			I/O	-	PIO0_10 — General purpose digital input/output pin.
			I/O	-	SCK0 — Serial clock for SPI0.
			O	-	CT16B0_MAT2 — Match output 2 for 16-bit timer 0.

The start logic must be configured in the system configuration block and in the NVIC before being used.

7.17.2 Reset

Reset has four sources on the LPC1110/11/12/13/14/15: the $\overline{\text{RESET}}$ pin, the Watchdog reset, Power-On Reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

A LOW-going pulse as short as 50 ns resets the part.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

An external pull-up resistor is required on the $\overline{\text{RESET}}$ pin if Deep power-down mode is used.

7.17.3 Brownout detection

The LPC1110/11/12/13/14/15 includes up to four levels for monitoring the voltage on the V_{DD} pin. If this voltage falls below one of the selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC in order to cause a CPU interrupt; if not, software can monitor the signal by reading a dedicated status register. Four threshold levels can be selected to cause a forced reset of the chip.

7.17.4 Code security (Code Read Protection - CRP)

This feature of the LPC1110/11/12/13/14/15 allows user to enable different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

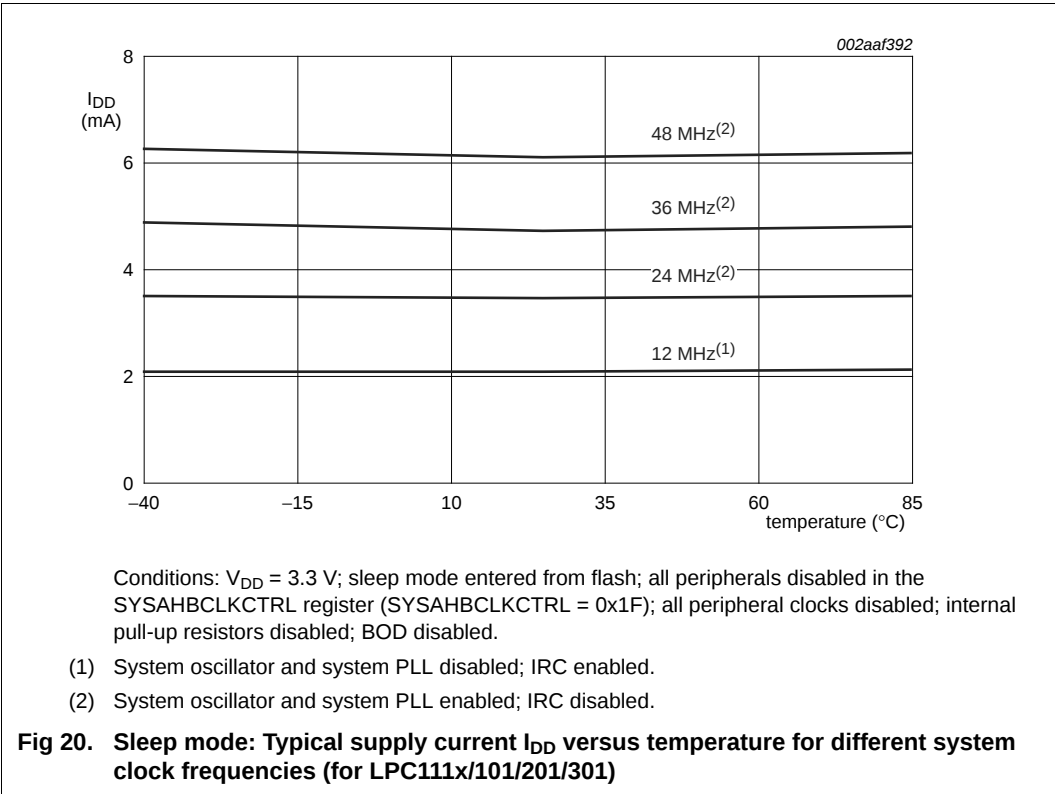
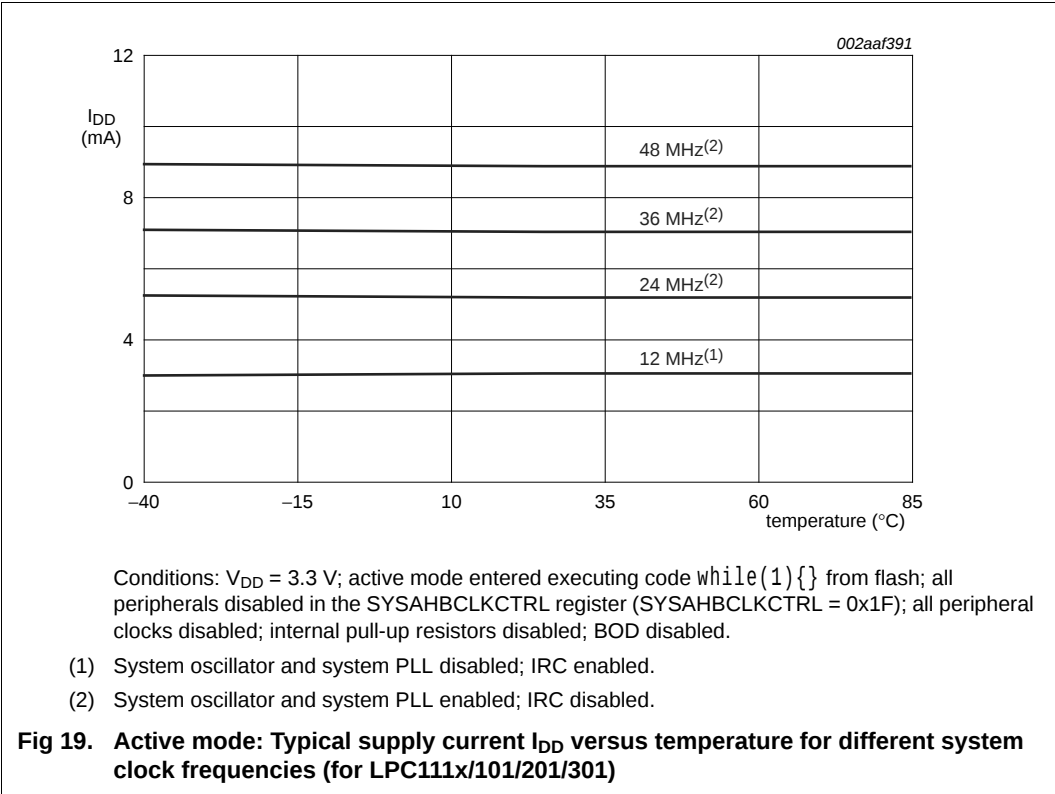
In addition, ISP entry via the PIO0_1 pin can be disabled without enabling CRP. For details see the *LPC111x user manual*.

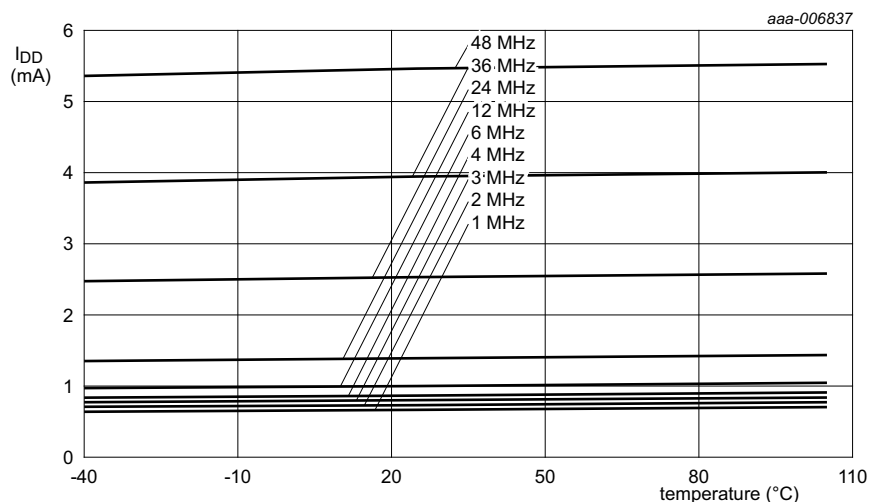
There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_1 pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via the UART.

Table 17. Static characteristics (LPC1100XL series) ...continued $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
V _{IL}	LOW-level input voltage		-	-	0.3V _{DD}	V
V _{hys}	hysteresis voltage		-	0.4	-	V
V _{OH}	HIGH-level output voltage	2.5 V ≤ V _{DD} ≤ 3.6 V; I _{OH} = −4 mA	V _{DD} − 0.4	-	-	V
		1.8 V ≤ V _{DD} < 2.5 V; I _{OH} = −3 mA	V _{DD} − 0.4	-	-	V
V _{OL}	LOW-level output voltage	2.5 V ≤ V _{DD} ≤ 3.6 V; I _{OL} = 4 mA	-	-	0.4	V
		1.8 V ≤ V _{DD} < 2.5 V; I _{OL} = 3 mA	-	-	0.4	V
I _{OH}	HIGH-level output current	V _{OH} = V _{DD} − 0.4 V; 2.5 V ≤ V _{DD} ≤ 3.6 V	−4	-	-	mA
		1.8 V ≤ V _{DD} < 2.5 V	−3	-	-	mA
I _{OL}	LOW-level output current	V _{OL} = 0.4 V 2.5 V ≤ V _{DD} ≤ 3.6 V	4	-	-	mA
		1.8 V ≤ V _{DD} < 2.5 V	3	-	-	mA
I _{OHS}	HIGH-level short-circuit output current	V _{OH} = 0 V ^[16]	-	-	−45	mA
I _{OLS}	LOW-level short-circuit output current	V _{OL} = V _{DD} ^[16]	-	-	50	mA
I _{pd}	pull-down current	V _I = 5 V	10	50	150	μA
I _{pu}	pull-up current	V _I = 0 V; 2.0 V ≤ V _{DD} ≤ 3.6 V	−15	−50	−85	μA
		1.8 V ≤ V _{DD} < 2.0 V	−10	−50	−85	μA
		V _{DD} < V _I < 5 V	0	0	0	μA
High-drive output pin (PIO0_7)						
I _{IL}	LOW-level input current	V _I = 0 V; on-chip pull-up resistor disabled	-	0.5	10	nA
I _{IH}	HIGH-level input current	V _I = V _{DD} ; on-chip pull-down resistor disabled	-	0.5	10	nA
I _{OZ}	OFF-state output current	V _O = 0 V; V _O = V _{DD} ; on-chip pull-up/down resistors disabled	-	0.5	10	nA
V _I	input voltage	pin configured to provide a digital function ^{[13][14][15]}	0	-	5.0	V
V _O	output voltage	output active	0	-	V _{DD}	V
V _{IH}	HIGH-level input voltage		0.7V _{DD}	-	-	V
V _{IL}	LOW-level input voltage		-	-	0.3V _{DD}	V
V _{hys}	hysteresis voltage		0.4	-	-	V





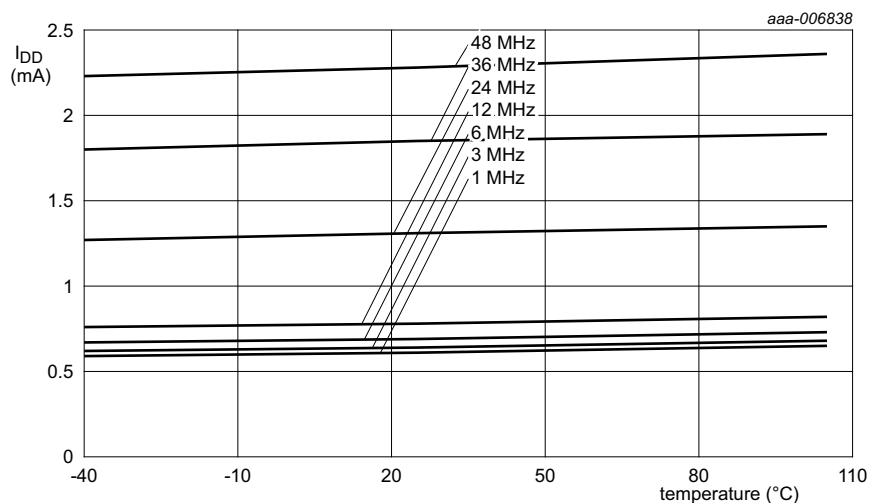
Conditions: $V_{DD} = 3.3$ V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz to 6 MHz: system oscillator enabled; PLL, IRC disabled.

12 MHz: IRC enabled; system oscillator, PLL disabled.

24 MHz to 48 MHz: IRC disabled; system oscillator, PLL enabled.

Fig 29. Active mode: Typical supply current I_{DD} versus temperature for different system clock frequencies (for LPC111xXL)



Conditions: $V_{DD} = 3.3$ V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz to 6 MHz: system oscillator enabled; PLL, IRC disabled.

12 MHz: IRC enabled; system oscillator, PLL disabled.

24 MHz to 48 MHz: IRC disabled; system oscillator, PLL enabled.

Fig 30. Sleep mode: Typical supply current I_{DD} versus temperature for different system clock frequencies (for LPC111xXL)

10.9 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at $T_{amb} = 25\text{ }^{\circ}\text{C}$. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 48 MHz.

Table 21. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	48 MHz	
IRC	0.27	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	0.22	-	-	IRC running; PLL off; independent of main clock frequency.
Watchdog oscillator at 500 kHz/2	0.004	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	0.051	-	-	Independent of main clock frequency.
Main PLL	-	0.21	-	
ADC	-	0.08	0.29	
CLKOUT	-	0.12	0.47	Main clock divided by 4 in the CLKOUTDIV register.
CT16B0	-	0.02	0.06	
CT16B1	-	0.02	0.06	
CT32B0	-	0.02	0.07	
CT32B1	-	0.02	0.06	
GPIO	-	0.23	0.88	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
IOCONFIG	-	0.03	0.10	
I2C	-	0.04	0.13	
ROM	-	0.04	0.15	
SPI0	-	0.12	0.45	
SPI1	-	0.12	0.45	
UART	-	0.22	0.82	
WDT/WWDT	-	0.02	0.06	Main clock selected as clock source for the WDT.

11.3 External clock

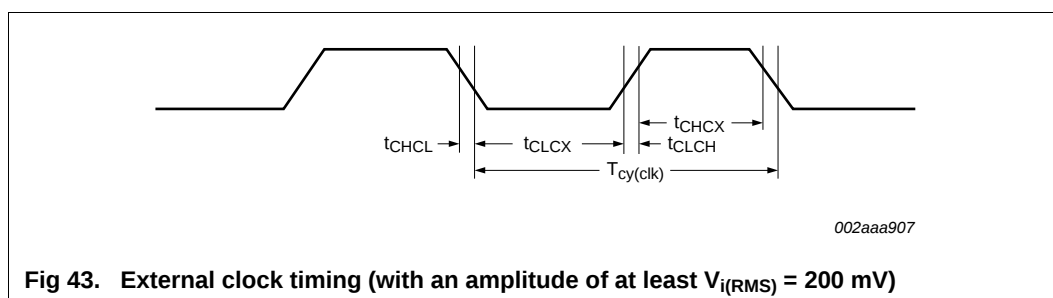
Table 24. Dynamic characteristic: external clock

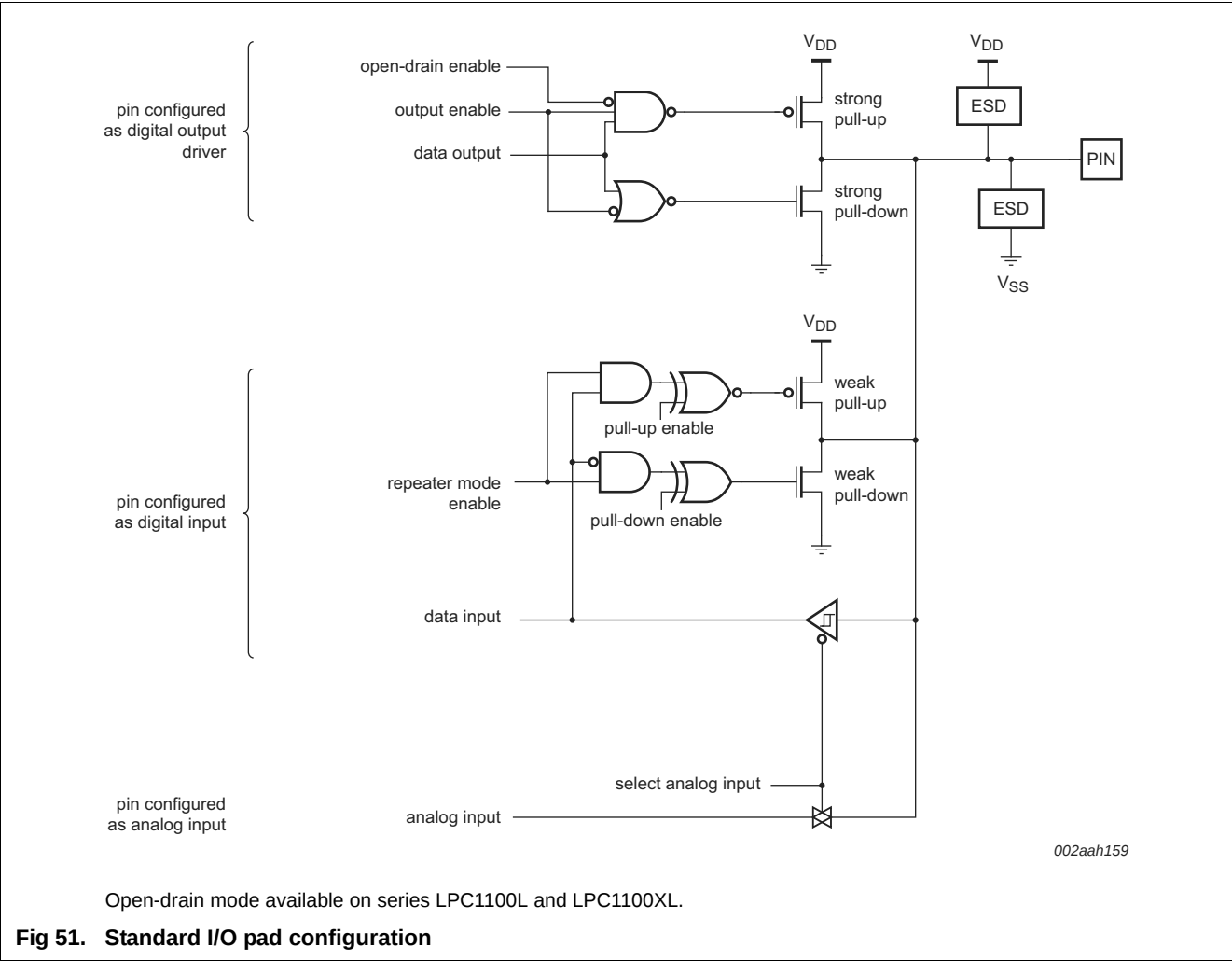
$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$; V_{DD} over specified ranges.^[1]

Symbol	Parameter	Conditions	Min	Typ ^[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

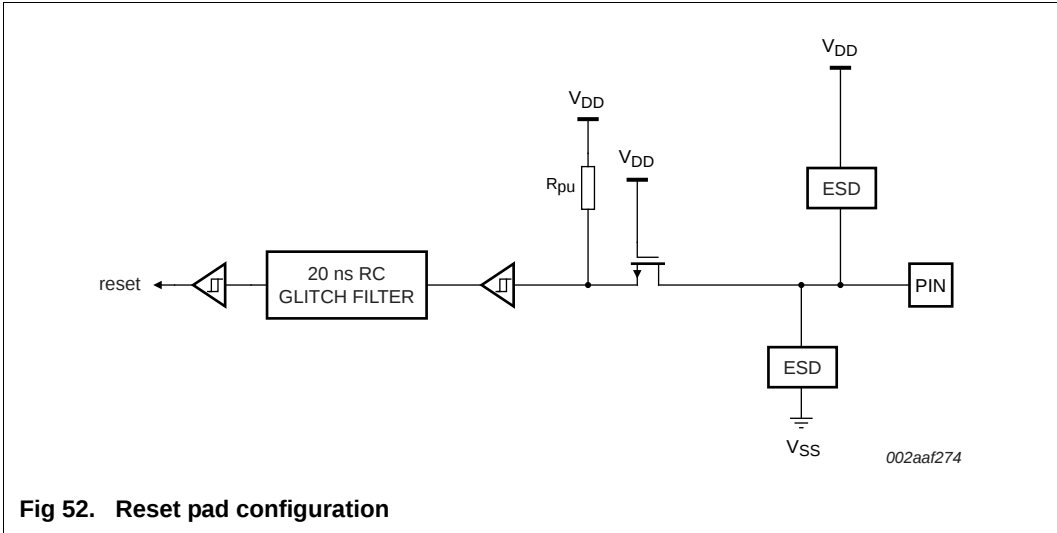
[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.



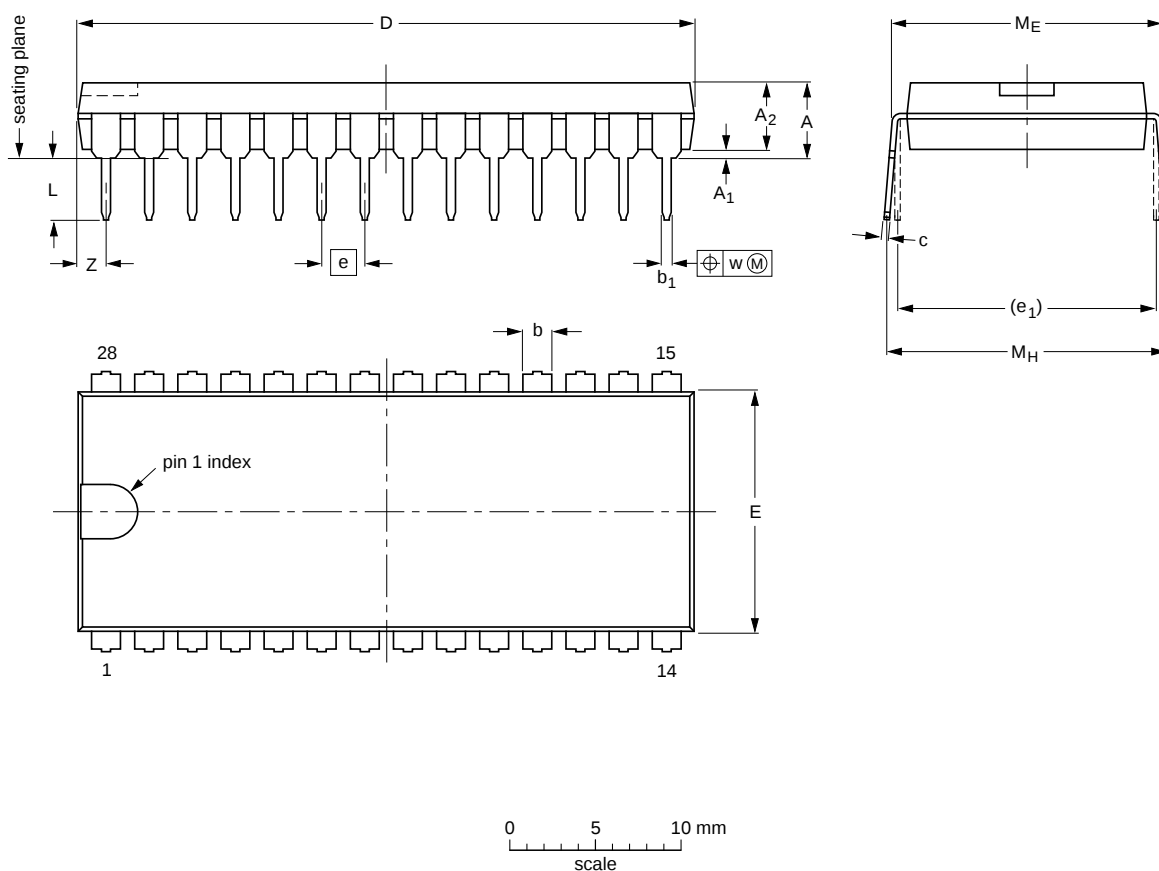


12.6 Reset pad configuration



DIP28: plastic dual in-line package; 28 leads (600 mil)

SOT117-1



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	5.1	0.51	4	1.7 1.3	0.53 0.38	0.32 0.23	36 35	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.2	0.02	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.1	0.6	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT117-1	051G05	MO-015	SC-510-28			99-12-27 03-02-13

Fig 57. Package outline SOT117-1 (DIP28)

HVQFN33: plastic thermal enhanced very thin quad flat package; no leads;
33 terminals; body 7 x 7 x 0.85 mm

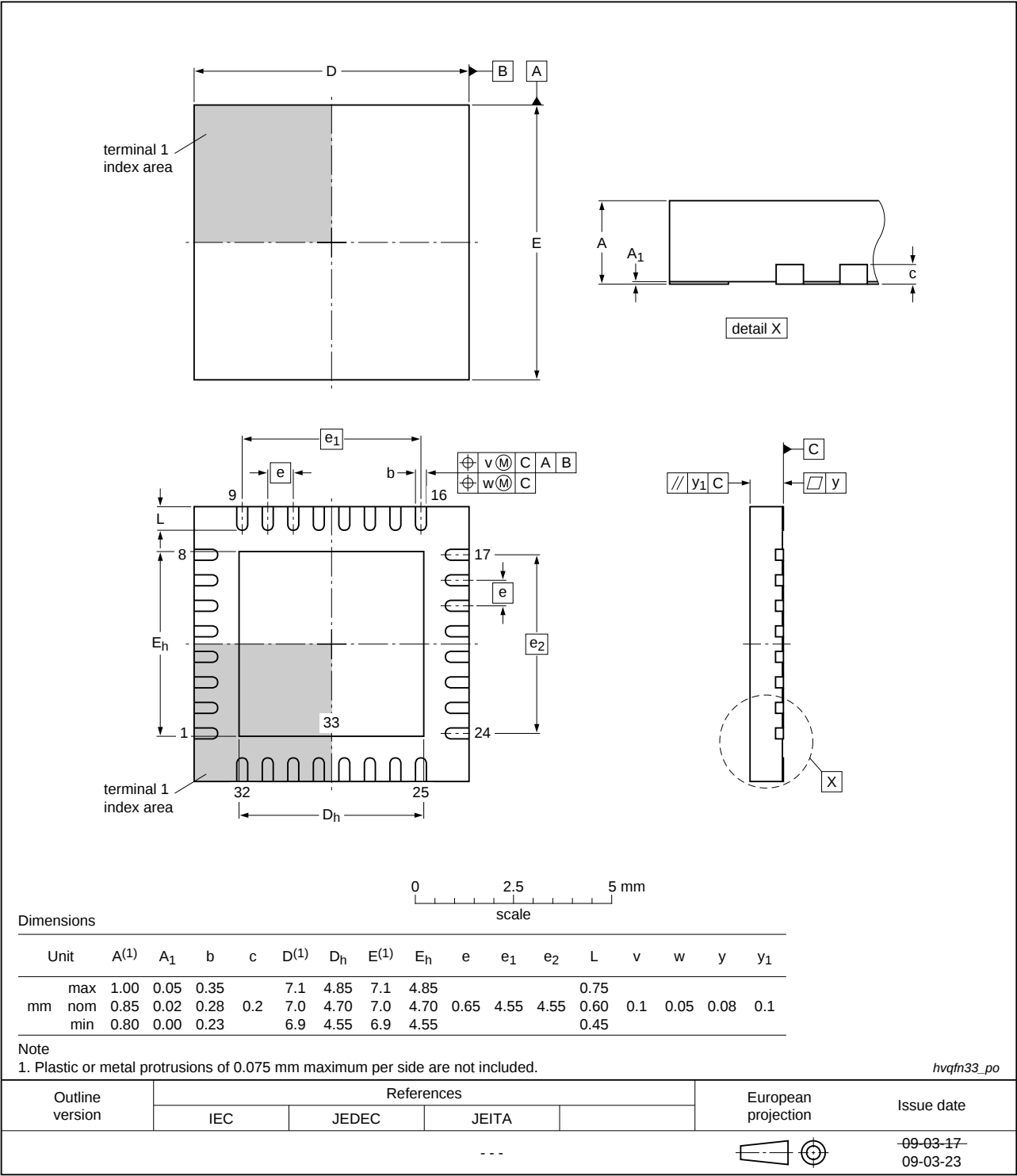


Fig 59. Package outline (HVQFN33 7x7)

14. Soldering

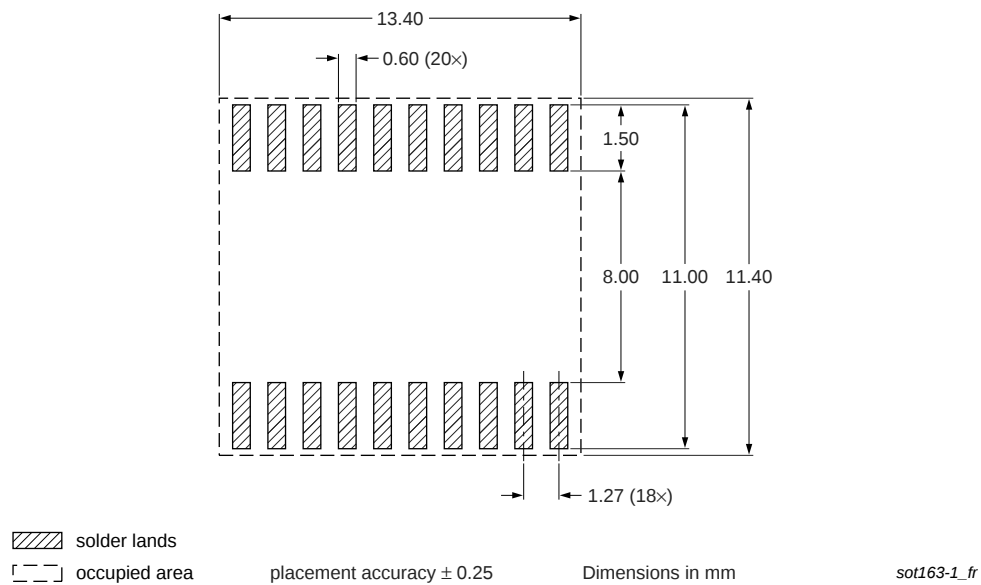


Fig 63. Reflow soldering of the SO20 package

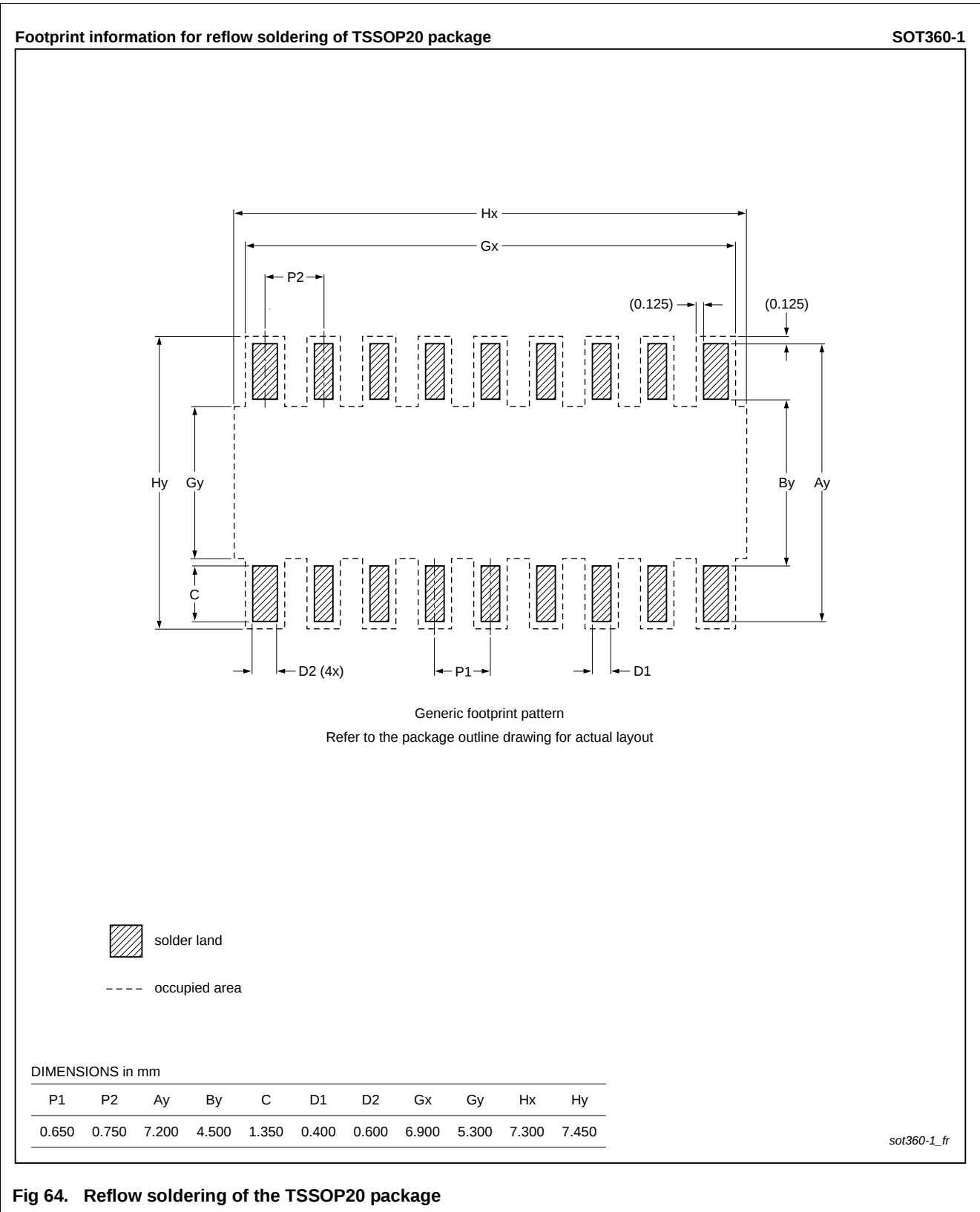


Fig 64. Reflow soldering of the TSSOP20 package

17. Revision history

Table 34. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC111X v.9.2	20140326	Product data sheet	-	LPC111X v.9.1
Modifications:	- Pin description tables for RESET/PIO0_0 updated: In deep power-down mode, this pin must be pulled HIGH externally. The RESET pin can be left unconnected or be used as a GPIO pin if an external RESET function is not needed. See Section 6.2. - Pin description notes relating to open-drain I2C-bus pins updated for clarity in Section 6.2. - Pin description of the WAKEUP pin updated for clarity. See Section 6.2. - Parts added: LPC1114JHI33/303, LPC1111JHN33/103, LPC1112JHN33/203, LPC1113JHN33/203, LPC1114JHN33/303, LPC1114JBD48/333, LPC1112FHI33/102, LPC1114JBD48/303, LPC1114JBD48/323, LPC1113JBD48/303, LPC1113JHN33/303, LPC1112JHN33/103, LPC1111JHN33/203, LPC1114JHN33/203.			
LPC111X v.9.1	20131213	Product data sheet	-	LPC111X v.9
Modifications:	- Table 17 "Static characteristics (LPC1100XL series)": - Added I_{DD} max spec for Deep-sleep and Deep power-down modes @ 25 °C and 105 °C. - Added Table note 11 "105 °C spec applies only to the LPC1112JHI33, LPC1114JHN33, LPC1115JBD48, and LPC1115JET48 parts." - Updated Table note 12 "WAKEUP pin and RESET pin are pulled HIGH externally." - Table 16 "Static characteristics (LPC1100, LPC1100L series)": - Updated Table note 9 "WAKEUP pin and RESET pin are pulled HIGH externally."			
LPC111X v.9	20131029	Product data sheet	-	LPC111X v.8.2
Modifications:	- Added LPC1112JHI33/203, LPC1114JHN33/333, LPC1115JBD48/303, and LPC1115JET48/303 parts. - Removed t_{clk(H)} and t_{clk(L)} from Figure 47 "SPI master timing in SPI mode" and Figure 48 "SPI slave timing in SPI mode"; spec not characterized. - Table 22 "Power-up characteristics[1]": Added table note "Does not apply to LPC1100XL series".			
LPC111X v.8.2	20130805	Product data sheet	-	LPC111X v.8.1
Modifications:	Added LPC1115FET48/303.			
LPC111X v.8.1	20130524	Product data sheet	-	LPC111X v.8
Modifications:	- Table 4 thru Table 11: Added "5 V tolerant pad" to RESET/PIO0_0 table note. - Added Section 9 "Thermal characteristics". - SRAM size corrected for part LPC1112FHN24/202 (4 kB). See Table 2.			
LPC111X v.8	20130220	Product data sheet	-	LPC111X v.7.5
Modifications:	- Table 16 "Static characteristics" added Pin capacitance section. - Default pin state corrected for pins PIO0_4 and PIO0_5 (I; IA) in Table 11 "LPC1100XL series: LPC1111/12/13/14 pin description table (HVQFN33 package)". - Table 12 "Limiting values" expanded for clarity. - Table 19 "Power consumption at very low frequencies using the watchdog oscillator" added. - Added Section 12.2 "Use of ADC input trigger signals". - Added Section 12.8 "ADC effective input impedance".			
LPC111X v.7.5	20121002	Product data sheet	-	LPC111X v.7.4

Table 34. Revision history ...continued

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	- Power consumption graphs added for parts LPC111x/102/202/302 (Figure 13 to Figure 17). - Parameter V_{hys} for I²C bus pins: typical value corrected $V_{hys} = 0.05V_{DD}$ in Table 7. - Typical value for parameter N_{endu} added in Table 12 "Flash characteristics". - I²C-bus pins configured as standard mode pins, parameter I_{OL} changed to 3.5 mA (minimum) for $2.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$. - Section 11.6 "ElectroMagnetic Compatibility (EMC)" added. - Power-up characterization added (Section 10.1 "Power-up ramp conditions").			
LPC1111_12_13_14 v.3	20101110	Product data sheet	-	LPC1111_12_13_14 v.2
Modifications:	- Parts LPC111x/102/202/302 added (LPC1100L series). - Power consumption data for parts LPC111x/102/202/302 added in Table 7. - PLL output frequency limited to 100 MHz in Section 7.15.2. - Description of $\overline{\text{RESET}}$ and WAKEUP functions updated in Section 6. - WDT description updated in Section 7.14. The WDT is a 24-bit timer. - Power profiles added to Section 2 and Section 7 for parts LPC111x/102/202/302.			
LPC1111_12_13_14 v.2	20100818	Product data sheet	-	LPC1111_12_13_14 v.1
Modifications:	V_{ESD} limit changed to $-6500\text{ V (min) }/+6500\text{ V (max)}$ in Table 6. t_{DS} updated for SPI in master mode (Table 17). - Deep-sleep mode functionality changed to allow BOD and watchdog oscillator as the only analog blocks allowed to remain running in Deep-sleep mode (Section 7.15.5.3). V_{DD} range changed to $3.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ in Table 15. - Reset state of pins and start logic functionality added in Table 3 to Table 5. - Section 7.16.1 added. - Section "Memory mapping control" removed. V_{OH} and I_{OH} specifications updated for high-drive pins in Table 7. - Section 9.4 added.			
LPC1111_12_13_14 v.1	20100416	Product data sheet	-	-

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For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

20. Contents

1	General description	1	7.16.5.1	Power profiles (LPC1100L and LPC1100XL series only)	54
2	Features and benefits	1	7.16.5.2	Sleep mode	55
3	Applications	3	7.16.5.3	Deep-sleep mode	55
4	Ordering information	3	7.16.5.4	Deep power-down mode	55
4.1	Ordering options	6	7.17	System control	55
5	Block diagram	9	7.17.1	Start logic	55
6	Pinning information	11	7.17.2	Reset	56
6.1	Pinning	11	7.17.3	Brownout detection	56
6.2	Pin description	19	7.17.4	Code security (Code Read Protection - CRP)	56
7	Functional description	45	7.17.5	APB interface	57
7.1	ARM Cortex-M0 processor	45	7.17.6	AHBLite	57
7.2	On-chip flash program memory	45	7.17.7	External interrupt inputs	57
7.3	On-chip SRAM	45	7.18	Emulation and debugging	57
7.4	Memory map	45	8	Limiting values	58
7.5	Nested Vectored Interrupt Controller (NVIC)	47	9	Thermal characteristics	59
7.5.1	Features	47	10	Static characteristics	61
7.5.2	Interrupt sources	48	10.1	LPC1100, LPC1100L series	61
7.6	IOCONFIG block	48	10.2	LPC1100XL series	65
7.7	Fast general purpose parallel I/O	48	10.3	ADC static characteristics	69
7.7.1	Features	48	10.4	BOD static characteristics	71
7.8	UART	49	10.5	Power consumption LPC1100 series (LPC111x/101/201/301)	72
7.8.1	Features	49	10.6	Power consumption LPC1100L series (LPC111x/002/102/202/302)	75
7.9	SPI serial I/O controller	49	10.7	Power consumption LPC1100XL series (LPC111x/103/203/303/323/333)	78
7.9.1	Features	49	10.8	CoreMark data	82
7.10	I ² C-bus serial I/O controller	50	10.9	Peripheral power consumption	84
7.10.1	Features	50	10.10	Electrical pin characteristics	85
7.11	10-bit ADC	50	11	Dynamic characteristics	88
7.11.1	Features	50	11.1	Power-up ramp conditions	88
7.12	General purpose external event counter/timers	51	11.2	Flash memory	88
7.12.1	Features	51	11.3	External clock	89
7.13	System tick timer	51	11.4	Internal oscillators	90
7.14	Watchdog timer (LPC1100 series, LPC111x/101/201/301)	51	11.5	I/O pins	92
7.14.1	Features	51	11.6	I ² C-bus	93
7.15	Windowed WatchDog Timer (LPC1100L and LPC1100XL series)	52	11.7	SPI interfaces	94
7.15.1	Features	52	12	Application information	97
7.16	Clocking and power control	52	12.1	ADC usage notes	97
7.16.1	Crystal oscillators	52	12.2	Use of ADC input trigger signals	97
7.16.1.1	Internal RC oscillator	53	12.3	XTAL input	97
7.16.1.2	System oscillator	53	12.4	XTAL Printed Circuit Board (PCB) layout guidelines	99
7.16.1.3	Watchdog oscillator	54	12.5	Standard I/O pad configuration	99
7.16.2	System PLL	54	12.6	Reset pad configuration	100
7.16.3	Clock output	54	12.7	ElectroMagnetic Compatibility (EMC)	101
7.16.4	Wake-up process	54			
7.16.5	Power control	54			

continued >>