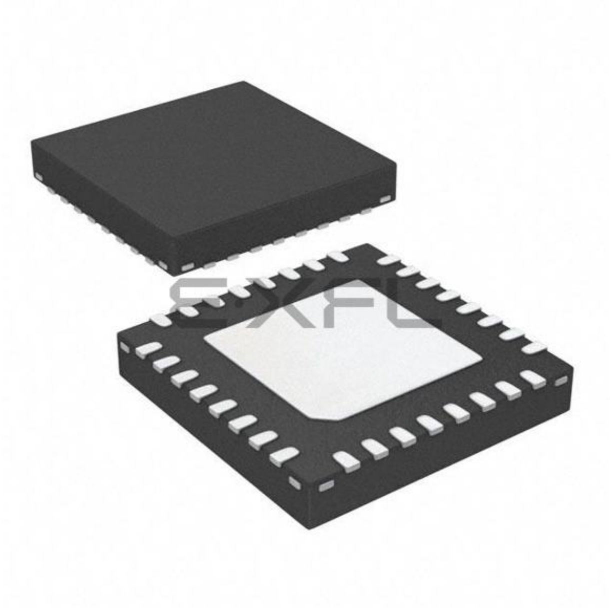
NXP USA Inc. - LPC1113FHN33/203,5 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	28
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VQFN Exposed Pad
Supplier Device Package	32-HVQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1113fhn33-203-5

Table 1. Ordering information *…continued*

Type number	Package		
	Name	Description	Version
LPC1114FHI33/302	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC1114FHI33/303	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC1114JHI33/303	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC1114FHN33/203	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1114JHN33/203	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1114FHN33/303	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1114JHN33/303	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1114FHN33/333	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1114JHN33/333	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1113FBD48/301	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1113FBD48/302	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1113FBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1113JBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114FBD48/301	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114FBD48/302	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114FBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114JBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114FBD48/323	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114JBD48/323	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114FBD48/333	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114JBD48/333	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1115FBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

Table 2. Ordering options *…continued*

Type number	Series	Flash	Total SRAM	Power profiles	UART	I^2C/ Fast+	SPI	ADC channel	GPIO	Package	Temp[1]
LPC1115JBD48/303	LPC1100XL	64 kB	8 kB	yes	1	1	2	8	42	LQFP48	J
LPC1115FET48/303	LPC1100XL	64 kB	8 kB	yes	1	1	2	8	42	TFBGA48	F
LPC1115JET48/303	LPC1100XL	64 kB	8 kB	yes	1	1	2	8	42	TFBGA48	J

[1] F = −40 °C to +85 °C, J = −40 °C to +105 °C.

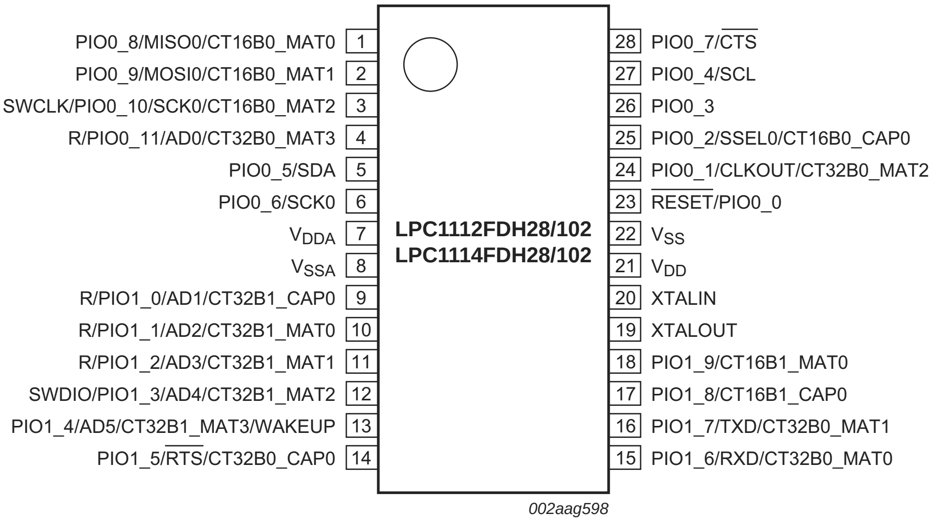


Fig 12. LPC1100L pin configuration TSSOP28 package

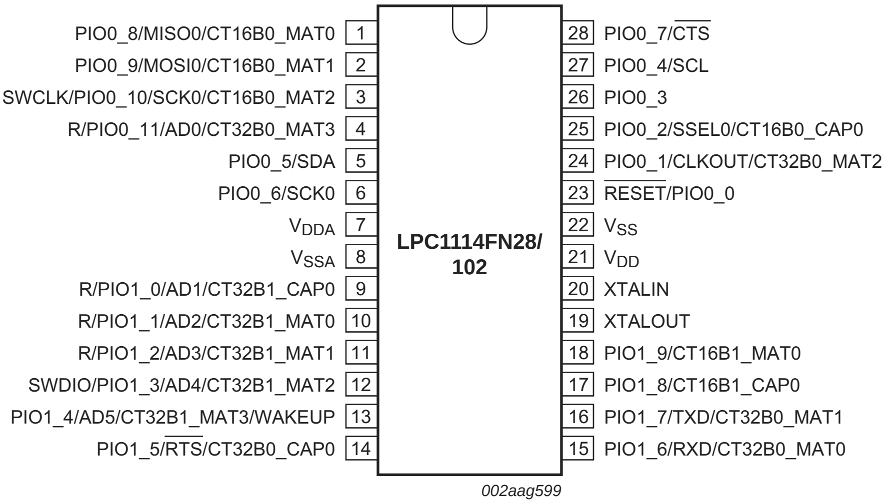


Fig 13. LPC1100L series pin configuration DIP28 package

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level); IA = inactive, no pull-up/down enabled.

[2] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 51).

[4] I^2C-bus pin compliant with the I^2C-bus specification for I^2C standard mode and I^2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 51).

[6] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

Table 5. LPC1100L series: LPC1112 pin description table (TSSOP20 with V_{DDA} and V_{SSA} pins)

Symbol	Pin TSSOP20		Start logic input	Type	Reset state [1]	Description
PIO0_0 to PIO0_11				I/O		**Port 0 —** Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.
$\overline{\text{RESET}}$/PIO0_0	17	[2]	yes	I	I; PU	**$\overline{\text{RESET}}$ —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO pin if an external $\overline{\text{RESET}}$ function is not needed and Deep power-down mode is not used.
				I/O	-	**PIO0_0 —** General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/ CT32B0_MAT2	18	[3]	yes	I/O	I; PU	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
				O	-	**CLKOUT —** Clockout pin.
				O	-	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	19	[3]	yes	I/O	I; PU	**PIO0_2 —** General purpose digital input/output pin.
				I/O	-	**SSEL0 —** Slave Select for SPI0.
				I	-	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO0_3	20	[3]	yes	I/O	I; PU	**PIO0_3 —** General purpose digital input/output pin.
PIO0_8/MISO0/ CT16B0_MAT0	1	[3]	yes	I/O	I; PU	**PIO0_8 —** General purpose digital input/output pin.
				I/O	-	**MISO0 —** Master In Slave Out for SPI0.
				O	-	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	2	[3]	yes	I/O	I; PU	**PIO0_9 —** General purpose digital input/output pin.
				I/O	-	**MOSI0 —** Master Out Slave In for SPI0.
				O	-	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.

Table 10. LPC1100XL series: LPC1113/14/15 pin description table (LQFP48 and TFBGA48 package) *…continued*

Symbol	LQFP48	TFBGA48	Start logic input	Type	Reset state [1]	Description
PIO3_2/$\overline{\text{DCD}}$/ CT16B0_MAT2/ SCK1	43[3]	A4[3]	no	I/O	I; PU	**PIO3_2 —** General purpose digital input/output pin.
				I	-	**$\overline{\text{DCD}}$ —** Data Carrier Detect input for UART.
				O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
				I/O	-	**SCK1 —** Serial clock for SPI1.
PIO3_3/$\overline{\text{RI}}$/ CT16B0_CAP0	48[3]	A2[3]	no	I/O	I; PU	**PIO3_3 —** General purpose digital input/output pin.
				I	-	**$\overline{\text{RI}}$ —** Ring Indicator input for UART.
				I	-	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO3_4/ CT16B0_CAP1/RXD	18[3]	H4[3]	no	I/O	I; PU	**PIO3_4 —** General purpose digital input/output pin.
				I	-	**CT16B0_CAP1 —** Capture input 1 for 16-bit timer 0.
				I	-	**RXD —** Receiver input for UART
PIO3_5/ CT16B1_CAP1/TXD	21[3]	G6[3]	no	I/O	I; PU	**PIO3_5 —** General purpose digital input/output pin.
				I	-	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
				O	-	**TXD —** Transmitter output for UART
V_{DD}	8; 44	E2; B4	-	I	-	3.3 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	6[6]	D1[6]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	7[6]	E1[6]	-	O	-	Output from the oscillator amplifier.
V_{SS}	5; 41	D2; B5	-	I	-	Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level (V_{DD} = 3.3 V)); IA = inactive, no pull-up/down enabled.

[2] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See Figure 52 for the reset pad configuration.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 51).

[4] I^2C-bus pads compliant with the I^2C-bus specification for I^2C standard mode and I^2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 51).

[6] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

Table 11. LPC1100XL series: LPC1111/12/13/14 pin description table (HVQFN33 package) *…continued*

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO1_7/TXD/ CT32B0_MAT1	32[3]	no	I/O	I;PU	**PIO1_7 —** General purpose digital input/output pin.
			O	-	**TXD —** Transmitter output for UART.
			O	-	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO1_8/ CT16B1_CAP0	7[3]	no	I/O	I;PU	**PIO1_8 —** General purpose digital input/output pin.
			I	-	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
PIO1_9/ CT16B1_MAT0/ MOSI1	12[3]	no	I/O	I;PU	**PIO1_9 —** General purpose digital input/output pin.
			O	-	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
			I/O	-	**MOSI1 —** Master Out Slave In for SPI1
PIO1_10/AD6/ CT16B1_MAT1/ MISO1	20[5]	no	I/O	I;PU	**PIO1_10 —** General purpose digital input/output pin.
			I	-	**AD6 —** A/D converter, input 6.
			O	-	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
			I/O	-	**MISO1 —** Master In Slave Out for SPI1
PIO1_11/AD7/ CT32B1_CAP1	27[5]	no	I/O	I;PU	**PIO1_11 —** General purpose digital input/output pin.
			I	-	**AD7 —** A/D converter, input 7.
			I	-	**CT32B1_CAP1 —** Capture input 1 for 32-bit timer 1.
PIO2_0					**Port 2 —** Port 2 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 2 pins depends on the function selected through the IOCONFIG register block. Pins PIO2_1 to PIO2_11 are not available.
PIO2_0/$\overline{\text{DTR}}$/SSEL1	1[3]	no	I/O	I;PU	**PIO2_0 —** General purpose digital input/output pin.
			O	-	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for UART.
			I/O	-	**SSEL1 —** Slave Select for SPI1.
PIO3_0 to PIO3_5					**Port 3 —** Port 3 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 3 pins depends on the function selected through the IOCONFIG register block. Pins PIO3_0, PIO3_1, PIO3_3 and PIO3_6 to PIO3_11 are not available.
PIO3_2/ CT16B0_MAT2/ SCK1	28[3]	no	I/O	I;PU	**PIO3_2 —** General purpose digital input/output pin.
			O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
			I/O	-	**SCK1 —** Serial clock for SPI1.
PIO3_4/ CT16B0_CAP1/RXD	13[3]	no	I/O	I;PU	**PIO3_4 —** General purpose digital input/output pin.
			I	-	**CT16B0_CAP1 —** Capture input 1 for 16-bit timer 0.
			I	-	**RXD —** Receiver input for UART.
PIO3_5/ CT16B1_CAP1/TXD	14[3]	no	I/O	I;PU	**PIO3_5 —** General purpose digital input/output pin.
			I	-	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
			O	-	**TXD —** Transmitter output for UART.

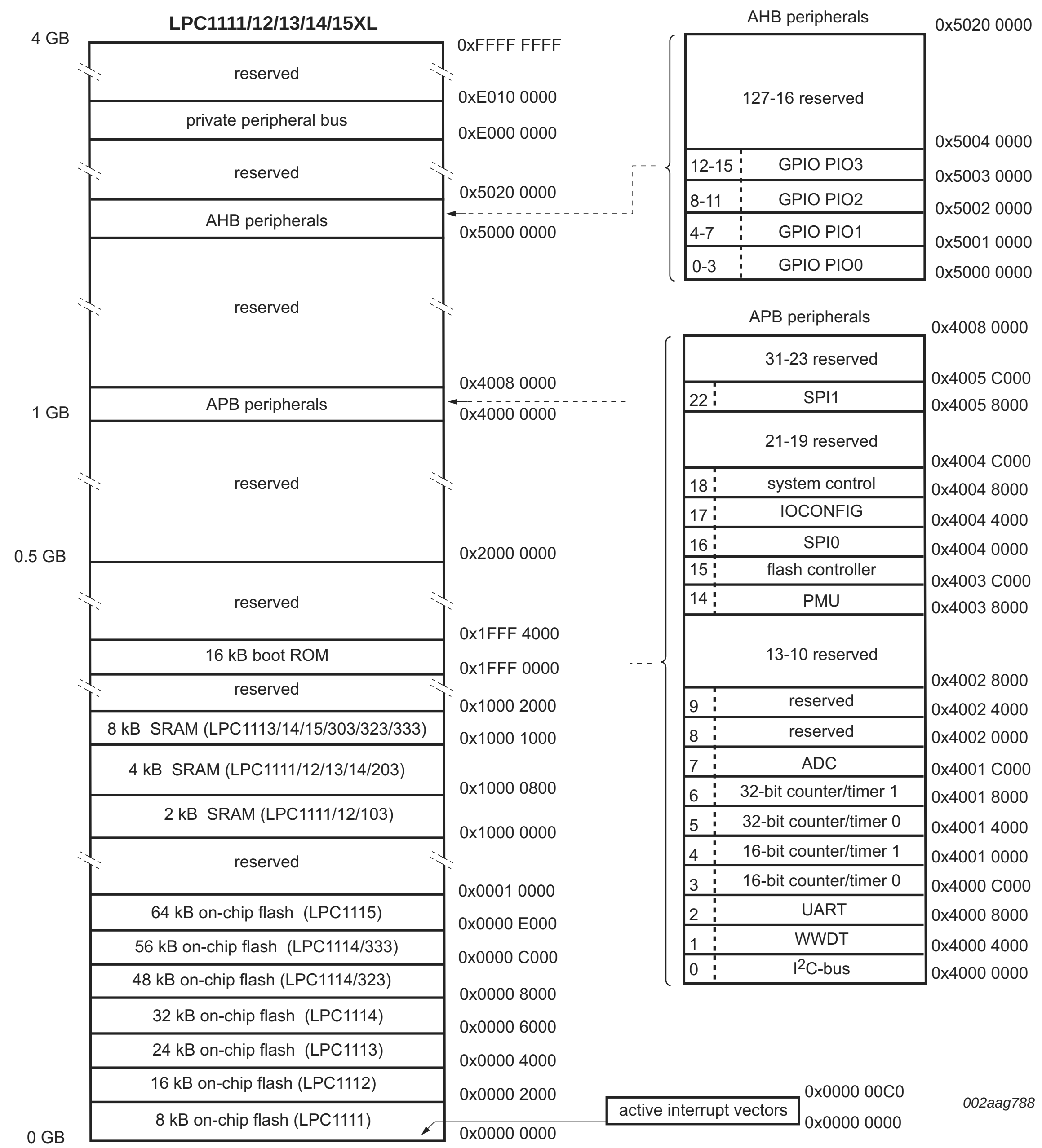


Fig 15. LPC1100XL series memory map

7.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.

- Optional conversion on transition of input pin or timer match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.

7.12 General purpose external event counter/timers

The LPC1110/11/12/13/14/15 include two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes up to two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.12.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- Up to two capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

7.13 System tick timer

The ARM Cortex-M0 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

7.14 Watchdog timer (LPC1100 series, LPC111x/101/201/301)

Remark: The watchdog timer without windowed features is available on parts LPC111x/101/201/301.

The purpose of the watchdog is to reset the microcontroller within a selectable time period.

7.14.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.

Table 17. Static characteristics (LPC1100XL series) *…continued*
T_{amb} = –40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage		-	0.4	-	V
V_{OH}	HIGH-level output voltage	$2.5 V \leq V_{DD} \leq 3.6 V$; $I_{OH} = -4 mA$	$V_{DD} - 0.4$	-	-	V
		$1.8 V \leq V_{DD} < 2.5 V$; $I_{OH} = -3 mA$	$V_{DD} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	$2.5 V \leq V_{DD} \leq 3.6 V$; $I_{OL} = 4 mA$	-	-	0.4	V
		$1.8 V \leq V_{DD} < 2.5 V$; $I_{OL} = 3 mA$	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD} - 0.4 V$; $2.5 V \leq V_{DD} \leq 3.6 V$	–4	-	-	mA
		$1.8 V \leq V_{DD} < 2.5 V$	–3	-	-	mA
I_{OL}	LOW-level output current	$V_{OL} = 0.4 V$ $2.5 V \leq V_{DD} \leq 3.6 V$	4	-	-	mA
		$1.8 V \leq V_{DD} < 2.5 V$	3	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	$V_{OH} = 0 V$ [16]	-	-	–45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$ [16]	-	-	50	mA
I_{pd}	pull-down current	$V_I = 5 V$	10	50	150	μA
I_{pu}	pull-up current	$V_I = 0 V$; $2.0 V \leq V_{DD} \leq 3.6 V$	–15	–50	–85	μA
		$1.8 V \leq V_{DD} < 2.0 V$	–10	–50	–85	μA
		$V_{DD} < V_I < 5 V$	0	0	0	μA
High-drive output pin (PIO0_7)						
I_{IL}	LOW-level input current	$V_I = 0 V$; on-chip pull-up resistor disabled	-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled	-	0.5	10	nA
I_{OZ}	OFF-state output current	$V_O = 0 V$; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled	-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function [13][14] [15]	0	-	5.0	V
V_O	output voltage	output active	0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage		0.4	-	-	V

10.4 BOD static characteristics

Table 19. BOD static characteristics[1]

T_{amb} = 25 °C.

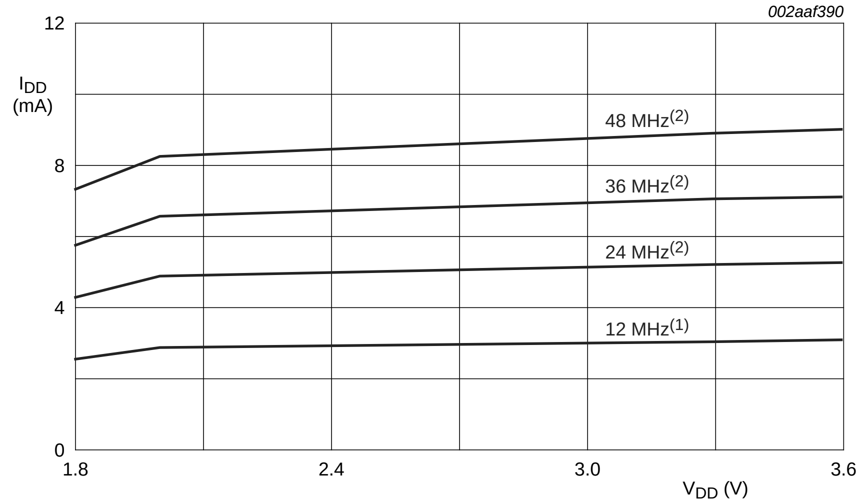
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 1				
		assertion	-	2.22	-	V
		de-assertion	-	2.35	-	V
		interrupt level 2				
		assertion	-	2.52	-	V
		de-assertion	-	2.66	-	V
		interrupt level 3				
		assertion	-	2.80	-	V
		de-assertion	-	2.90	-	V
		reset level 0				
		assertion	-	1.46	-	V
		de-assertion	-	1.63	-	V
		reset level 1				
		assertion	-	2.06	-	V
		de-assertion	-	2.15	-	V
		reset level 2				
		assertion	-	2.35	-	V
		de-assertion	-	2.43	-	V
		reset level 3				
		assertion	-	2.63	-	V
		de-assertion	-	2.71	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *LPC111x user manual*.

10.5 Power consumption LPC1100 series (LPC111x/101/201/301)

Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see *LPC111x user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCONFIG block.
- Configure GPIO pins as outputs using the GPIOnDIR registers.
- Write 0 to all GPIOnDATA registers to drive the outputs LOW.

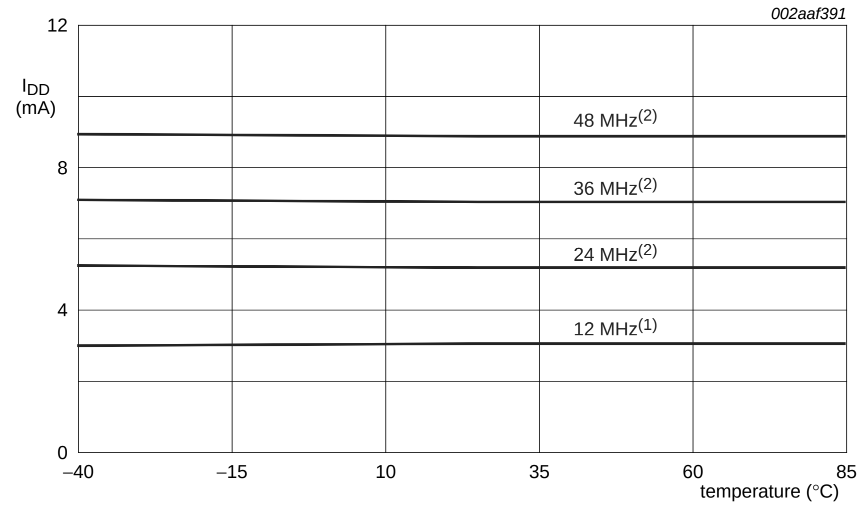


Conditions: T_{amb} = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 18. Active mode: Typical supply current I_{DD} versus supply voltage V_{DD} for different system clock frequencies (for LPC111x/101/201/301)

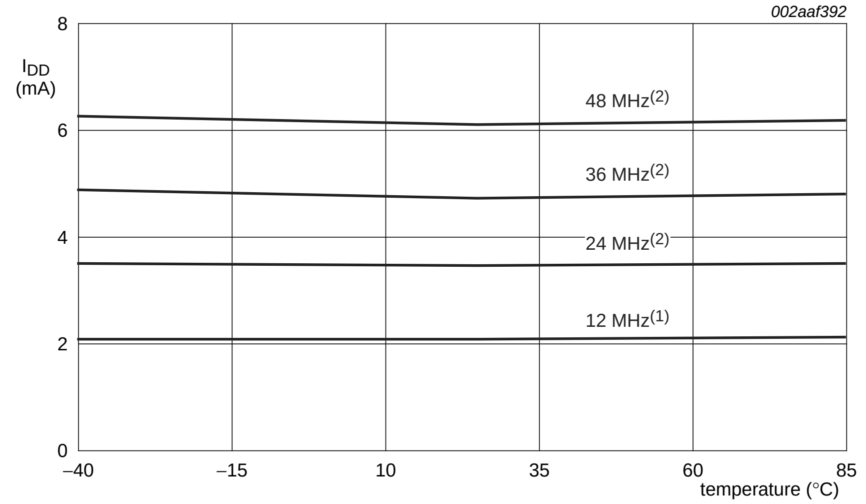


Conditions: V_{DD} = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 19. Active mode: Typical supply current I_{DD} versus temperature for different system clock frequencies (for LPC111x/101/201/301)



Conditions: V_{DD} = 3.3 V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled.

(1) System oscillator and system PLL disabled; IRC enabled.

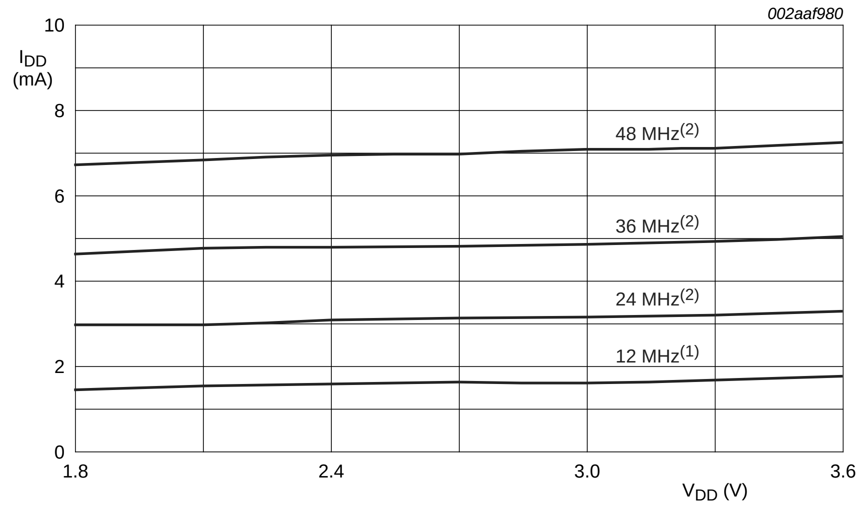
(2) System oscillator and system PLL enabled; IRC disabled.

Fig 20. Sleep mode: Typical supply current I_{DD} versus temperature for different system clock frequencies (for LPC111x/101/201/301)

10.6 Power consumption LPC1100L series (LPC111x/002/102/202/302)

Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see *LPC111x user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCONFIG block.
- Configure GPIO pins as outputs using the GPIOnDIR registers.
- Write 0 to all GPIOnDATA registers to drive the outputs LOW.

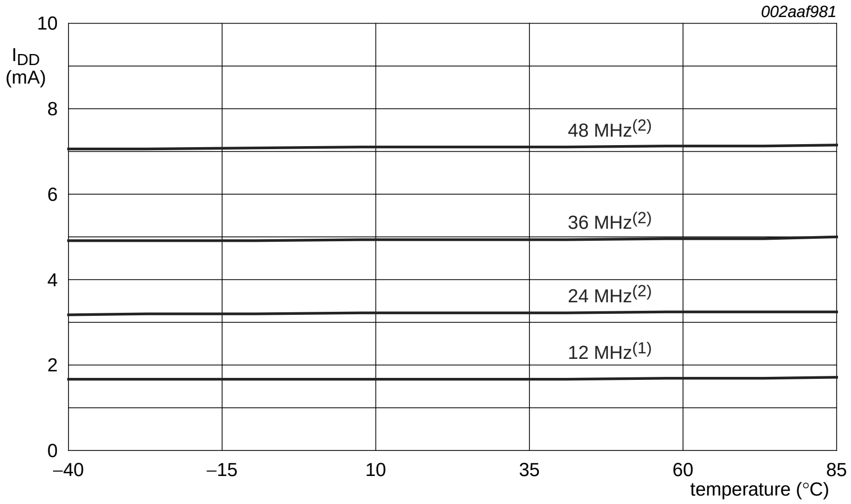


Conditions: T_{amb} = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 23. Active mode: Typical supply current I_{DD} versus supply voltage V_{DD} for different system clock frequencies (for LPC111x/002/102/202/302)

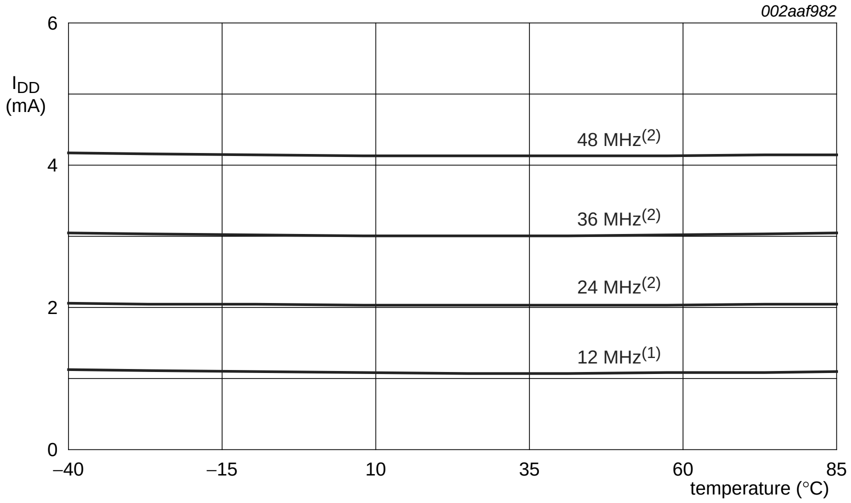


Conditions: V_{DD} = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 24. Active mode: Typical supply current I_{DD} versus temperature for different system clock frequencies (for LPC111x/002/102/202/302)



Conditions: V_{DD} = 3.3 V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

(1) System oscillator and system PLL disabled; IRC enabled.

(2) System oscillator and system PLL enabled; IRC disabled.

Fig 25. Sleep mode: Typical supply current I_{DD} versus temperature for different system clock frequencies (for LPC111x/002/102/202/302)

11. Dynamic characteristics

11.1 Power-up ramp conditions

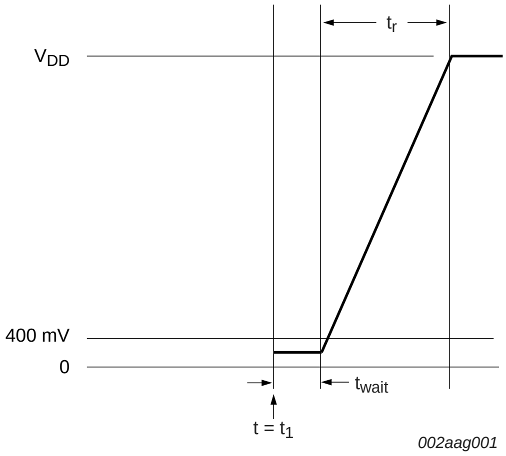
Table 22. Power-up characteristics[1]
T_{amb} = −40 °C to +85 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	at $t = t_1$: $0 < V_I \leq 400$ mV [2]	0	-	500	ms
t_{wait}	wait time	[2][3]	12	-	-	µs
V_I	input voltage	at $t = t_1$ on pin V_{DD}	0	-	400	mV

[1] Does not apply to the LPC1100XL series (LPC111x/103/203/303/323/333).

[2] See Figure 42.

[3] The wait time specifies the time the power supply must be at levels below 400 mV before ramping up.



Condition: $0 < V_I \leq 400$ mV at start of power-up ($t = t_1$)

Fig 42. Power-up ramp

11.2 Flash memory

Table 23. Flash characteristics
T_{amb} = −40 °C to +105 °C, unless otherwise specified. T_{amb} = 85 °C for flash programming.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{endu}	endurance	[1]	10000	100000	-	cycles
t_{ret}	retention time	powered	10	-	-	years
		unpowered	20	-	-	years
t_{er}	erase time	sector or multiple consecutive sectors	95	100	105	ms
t_{prog}	programming time	[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes. Flash programming operation temperature must not exceed T_{amb} = 85 °C.

11.6 I^{2}C-bus

Table 28. Dynamic characteristic: I^{2}C-bus pins[1]
T_{amb} = −40 °C to +105 °C.[2]

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency	Standard-mode	0	100	kHz
		Fast-mode	0	400	kHz
		Fast-mode Plus	0	1	MHz
t_f	fall time [4][5][6][7]	of both SDA and SCL signals Standard-mode	-	300	ns
		Fast-mode	$20 + 0.1 \times C_b$	300	ns
		Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock	Standard-mode	4.7	-	μs
		Fast-mode	1.3	-	μs
		Fast-mode Plus	0.5	-	μs
t_{HIGH}	HIGH period of the SCL clock	Standard-mode	4.0	-	μs
		Fast-mode	0.6	-	μs
		Fast-mode Plus	0.26	-	μs
$t_{HD;DAT}$	data hold time [3][4][8]	Standard-mode	0	-	μs
		Fast-mode	0	-	μs
		Fast-mode Plus	0	-	μs
$t_{SU;DAT}$	data set-up time [9][10]	Standard-mode	250	-	ns
		Fast-mode	100	-	ns
		Fast-mode Plus	50	-	ns

[1] See the I^{2}C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

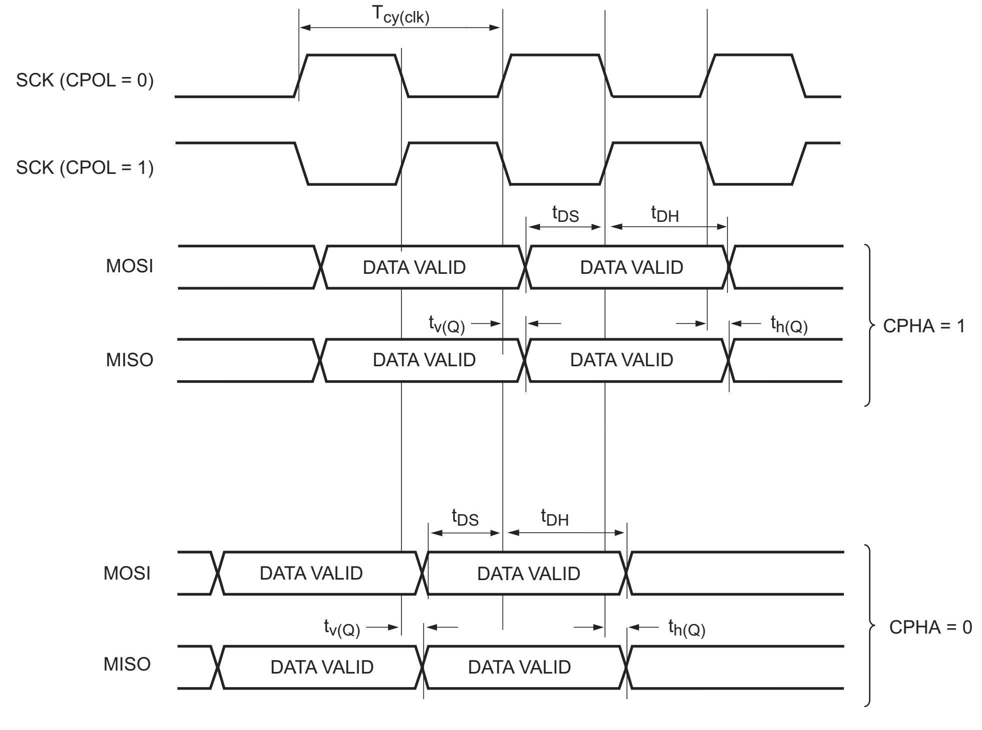
[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

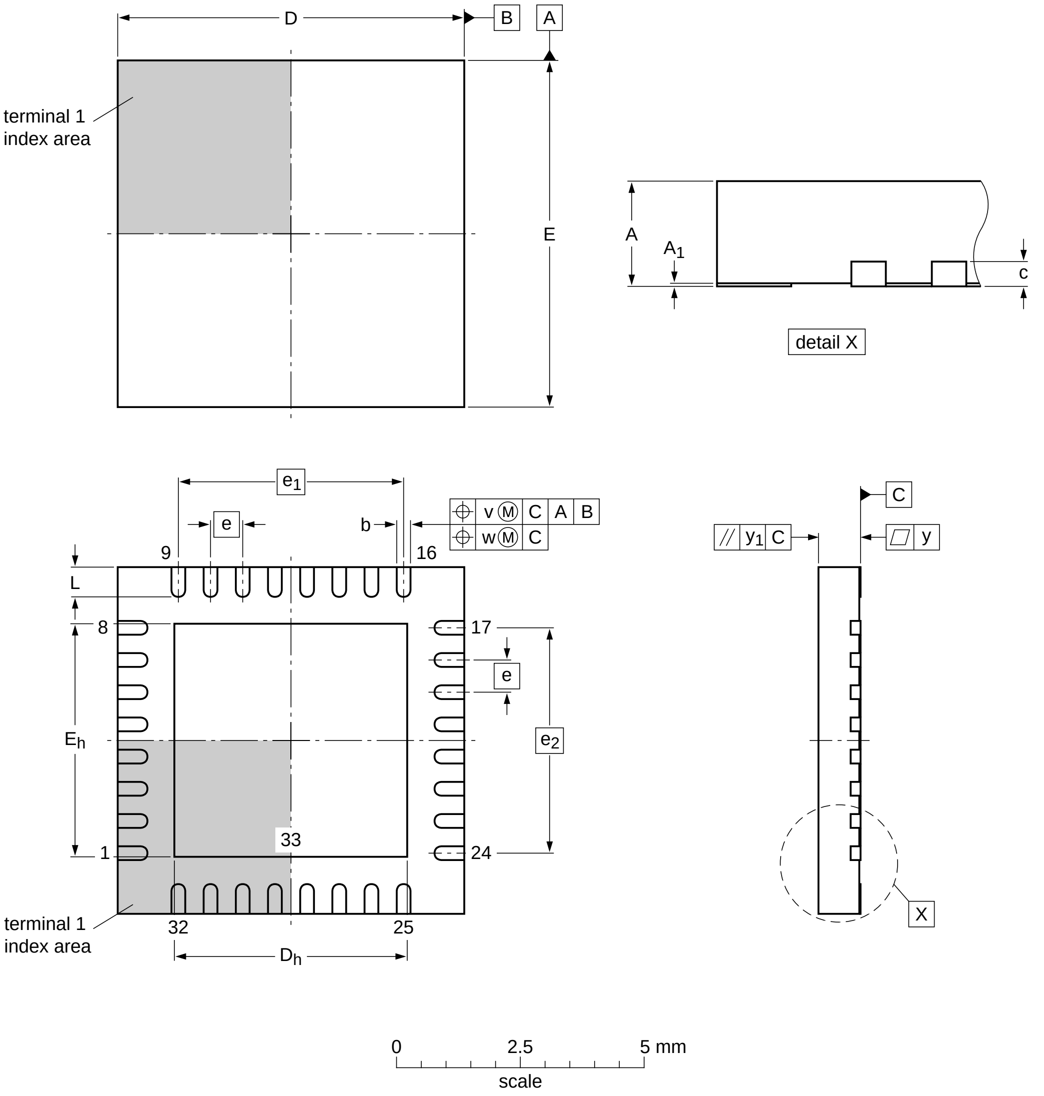
[10] A Fast-mode I^{2}C-bus device can be used in a Standard-mode I^{2}C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-mode I^{2}C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.



Pin names SCK, MISO, and MOSI refer to pins for both SPI peripherals, SPI0 and SPI1.

Fig 48. SPI slave timing in SPI mode

HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 x 7 x 0.85 mm



Dimensions

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	1.00	0.05	0.35		7.1	4.85	7.1	4.85				0.75				
	nom	0.85	0.02	0.28	0.2	7.0	4.70	7.0	4.70	0.65	4.55	4.55	0.60	0.1	0.05	0.08	0.1
	min	0.80	0.00	0.23		6.9	4.55	6.9	4.55				0.45				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

hvqfn33_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
			- - -			~~09-03-17~~ 09-03-23

Fig 59. Package outline (HVQFN33 7x7)

17. Revision history

Table 34. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC111X v.9.2	20140326	Product data sheet	-	LPC111X v.9.1
Modifications:	• Pin description tables for $\overline{\text{RESET}}$/PIO0_0 updated: In deep power-down mode, this pin must be pulled HIGH externally. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO pin if an external $\overline{\text{RESET}}$ function is not needed. See Section 6.2. • Pin description notes relating to open-drain I2C-bus pins updated for clarity in Section 6.2. • Pin description of the WAKEUP pin updated for clarity. See Section 6.2. • Parts added: LPC1114JHI33/303, LPC1111JHN33/103, LPC1112JHN33/203, LPC1113JHN33/203, LPC1114JHN33/303, LPC1114JBD48/333, LPC1112FHI33/102, LPC1114JBD48/303, LPC1114JBD48/323, LPC1113JBD48/303, LPC1113JHN33/303, LPC1112JHN33/103, LPC1111JHN33/203, LPC1114JHN33/203.			
LPC111X v.9.1	20131213	Product data sheet	-	LPC111X v.9
Modifications:	• Table 17 “Static characteristics (LPC1100XL series)”: – Added I_{DD} max spec for Deep-sleep and Deep power-down modes @ 25 °C and 105 °C. – Added Table note 11 “105 °C spec applies only to the LPC1112JHI33, LPC1114JHN33, LPC1115JBD48, and LPC1115JET48 parts.” – Updated Table note 12 “WAKEUP pin and RESET pin are pulled HIGH externally.” • Table 16 “Static characteristics (LPC1100, LPC1100L series)”: – Updated Table note 9 “WAKEUP pin and RESET pin are pulled HIGH externally.”			
LPC111X v.9	20131029	Product data sheet	-	LPC111X v.8.2
Modifications:	• Added LPC1112JHI33/203, LPC1114JHN33/333, LPC1115JBD48/303, and LPC1115JET48/303 parts. • Removed $t_{clk(H)}$ and $t_{clk(L)}$ from Figure 47 “SPI master timing in SPI mode” and Figure 48 “SPI slave timing in SPI mode”; spec not characterized. • Table 22 “Power-up characteristics[1]”: Added table note “Does not apply to LPC1100XL series”.			
LPC111X v.8.2	20130805	Product data sheet	-	LPC111X v.8.1
Modifications:	• Added LPC1115FET48/303.			
LPC111X v.8.1	20130524	Product data sheet	-	LPC111X v.8
Modifications:	• Table 4 thru Table 11: Added “5 V tolerant pad” to $\overline{\text{RESET}}$/PIO0_0 table note. • Added Section 9 “Thermal characteristics”. • SRAM size corrected for part LPC1112FHN24/202 (4 kB). See Table 2.			
LPC111X v.8	20130220	Product data sheet	-	LPC111X v.7.5
Modifications:	• Table 16 “Static characteristics” added Pin capacitance section. • Default pin state corrected for pins PIO0_4 and PIO0_5 (I; IA) in Table 11 “LPC1100XL series: LPC1111/12/13/14 pin description table (HVQFN33 package)”. • Table 12 “Limiting values” expanded for clarity. • Table 19 “ Power consumption at very low frequencies using the watchdog oscillator” added. • Added Section 12.2 “Use of ADC input trigger signals”. • Added Section 12.8 “ADC effective input impedance”.			
LPC111X v.7.5	20121002	Product data sheet	-	LPC111X v.7.4

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