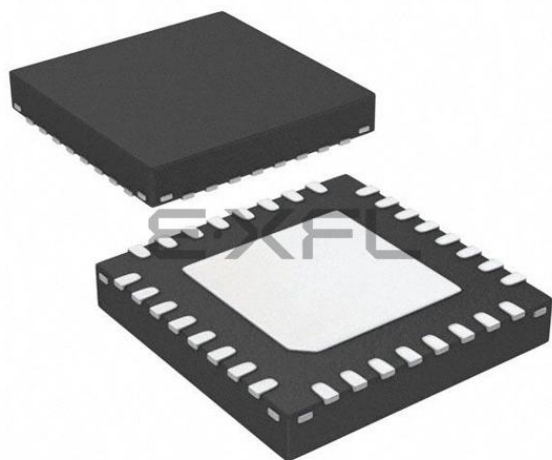




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Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	28
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VQFN Exposed Pad
Supplier Device Package	32-HVQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1113fhn33-302-5

Table 1. Ordering information ...continued

Type number	Package		
	Name	Description	Version
LPC1115JBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1115FET48/303	TFBGA48	plastic thin fine-pitch ball grid array package; 48 balls; body 4.5 × 4.5 × 0.7 mm	SOT1155-2
LPC1115JET48/303	TFBGA48	plastic thin fine-pitch ball grid array package; 48 balls; body 4.5 × 4.5 × 0.7 mm	SOT1155-2

4.1 Ordering options

Table 2. Ordering options

Type number	Series	Flash	Total SRAM	Power profiles	UART	I ² C/ Fast+	SPI	ADC channel	GPIO	Package	Temp ^[1]
LPC1110											
LPC1110FD20	LPC1100L	4 kB	1 kB	yes	1	1	1	5	16	SO20	F
LPC1111											
LPC1111FDH20/002	LPC1100L	8 kB	2 kB	yes	1	1	1	5	16	TSSOP20	F
LPC1111FHN33/101	LPC1100	8 kB	2 kB	no	1	1	1	8	28	HVQFN33	F
LPC1111FHN33/102	LPC1100L	8 kB	2 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1111FHN33/103	LPC1100XL	8 kB	2 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1111JHN33/103	LPC1100XL	8 kB	2 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1111FHN33/201	LPC1100	8 kB	4 kB	no	1	1	1	8	28	HVQFN33	F
LPC1111FHN33/202	LPC1100L	8 kB	4 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1111FHN33/203	LPC1100XL	8 kB	4 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1111JHN33/203	LPC1100XL	8 kB	4 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1112											
LPC1112FD20/102	LPC1100L	16 kB	4 kB	yes	1	1	1	5	16	SO20	F
LPC1112FDH20/102	LPC1100L	16 kB	4 kB	yes	1	-	1	5	14	TSSOP20	F
LPC1112FDH28/102	LPC1100L	16 kB	4 kB	yes	1	1	1	6	22	TSSOP28	F
LPC1112FHN24/202	LPC1100L	16 kB	4 kB	yes	1	1	1	6	19	HVQFN24	F
LPC1112FHN33/101	LPC1100	16 kB	2 kB	no	1	1	1	8	28	HVQFN33	F
LPC1112FHN33/102	LPC1100L	16 kB	2 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1112FHN33/103	LPC1100XL	16 kB	2 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1112JHN33/103	LPC1100XL	16 kB	2 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1112FHN33/201	LPC1100	16 kB	4 kB	no	1	1	1	8	28	HVQFN33	F
LPC1112FHN33/202	LPC1100L	16 kB	4 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1112FHN33/203	LPC1100XL	16 kB	4 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1112JHN33/203	LPC1100XL	16 kB	4 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1112FHI33/102	LPC1100L	16 kB	2 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1112FHI33/202	LPC1100L	16 kB	4 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1112FHI33/203	LPC1100XL	16 kB	4 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1112JHI33/203	LPC1100XL	16 kB	4 kB	yes	1	1	2	8	28	HVQFN33	J

Table 3. Pin description overview

Part	Pin description table	Pinning diagram
LPC1114FHN33/203	Table 11	Figure 7
LPC1114JHN33/203	Table 11	Figure 7
LPC1114FHN33/301	Table 9	Figure 6
LPC1114FHN33/302	Table 9	Figure 6
LPC1114JHN33/303	Table 11	Figure 7
LPC1114FHN33/303	Table 11	Figure 7
LPC1114FHN33/333	Table 11	Figure 7
LPC1114JHN33/333	Table 11	Figure 7
LPC1114FHI33/302	Table 9	Figure 6
LPC1114FHI33/303	Table 11	Figure 7
LPC1114JHI33/303	Table 11	Figure 7
LPC1113FBD48/301	Table 8	Figure 3
LPC1113FBD48/302	Table 8	Figure 3
LPC1113FBD48/303	Table 10	Figure 4
LPC1113JBD48/303	Table 10	Figure 4
LPC1114FBD48/301	Table 8	Figure 3
LPC1114FBD48/302	Table 8	Figure 3
LPC1114FBD48/303	Table 10	Figure 4
LPC1114JBD48/303	Table 10	Figure 4
LPC1114FBD48/323	Table 10	Figure 4
LPC1114JBD48/323	Table 10	Figure 4
LPC1114FBD48/333	Table 10	Figure 4
LPC1114JBD48/333	Table 10	Figure 4
LPC1115FBD48/303	Table 10	Figure 4
LPC1115JBD48/303	Table 10	Figure 4
LPC1115FET48/303	Table 10	Figure 5
LPC1115JET48/303	Table 10	Figure 5

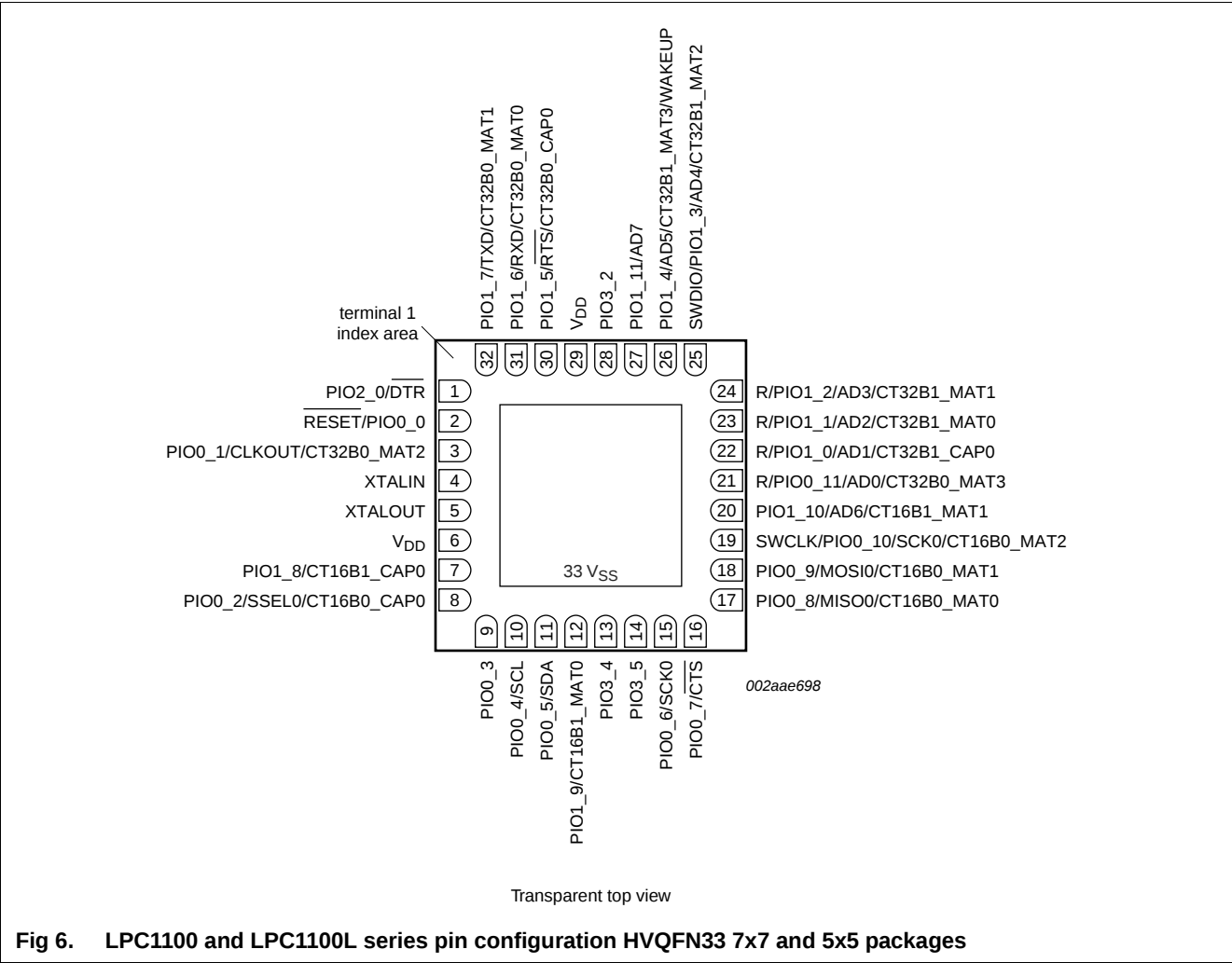
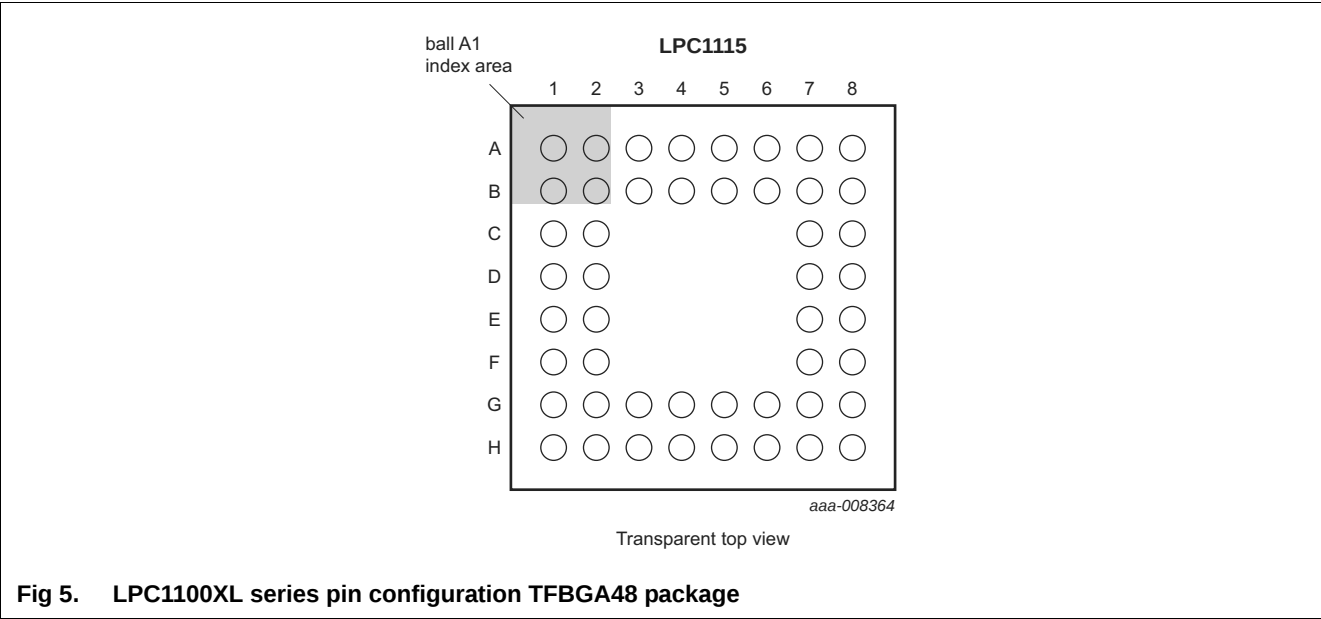


Table 8. LPC1100 and LPC1100L series: LPC1113/14 pin description table (LQFP48 package) ...continued

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2	29 ^[3]	yes	I	I; PU	SWCLK — Serial wire clock.
			I/O	-	PIO0_10 — General purpose digital input/output pin.
			I/O	-	SCK0 — Serial clock for SPI0.
			O	-	CT16B0_MAT2 — Match output 2 for 16-bit timer 0.
R/PIO0_11/ AD0/CT32B0_MAT3	32 ^[5]	yes	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO0_11 — General purpose digital input/output pin.
			I	-	AD0 — A/D converter, input 0.
			O	-	CT32B0_MAT3 — Match output 3 for 32-bit timer 0.
PIO1_0 to PIO1_11			I/O		Port 1 — Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block.
R/PIO1_0/ AD1/CT32B1_CAP0	33 ^[5]	yes	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_0 — General purpose digital input/output pin.
			I	-	AD1 — A/D converter, input 1.
			I	-	CT32B1_CAP0 — Capture input 0 for 32-bit timer 1.
R/PIO1_1/ AD2/CT32B1_MAT0	34 ^[5]	no	O	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_1 — General purpose digital input/output pin.
			I	-	AD2 — A/D converter, input 2.
			O	-	CT32B1_MAT0 — Match output 0 for 32-bit timer 1.
R/PIO1_2/ AD3/CT32B1_MAT1	35 ^[5]	no	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_2 — General purpose digital input/output pin.
			I	-	AD3 — A/D converter, input 3.
			O	-	CT32B1_MAT1 — Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ AD4/CT32B1_MAT2	39 ^[5]	no	I/O	I; PU	SWDIO — Serial wire debug input/output.
			I/O	-	PIO1_3 — General purpose digital input/output pin.
			I	-	AD4 — A/D converter, input 4.
			O	-	CT32B1_MAT2 — Match output 2 for 32-bit timer 1.
PIO1_4/AD5/ CT32B1_MAT3/ WAKEUP	40 ^[5]	no	I/O	I; PU	PIO1_4 — General purpose digital input/output pin with 10 ns glitch filter. In Deep power-down mode, this pin serves as the Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
			I	-	AD5 — A/D converter, input 5.
			O	-	CT32B1_MAT3 — Match output 3 for 32-bit timer 1.
PIO1_5/RTS/ CT32B0_CAP0	45 ^[3]	no	I/O	I; PU	PIO1_5 — General purpose digital input/output pin.
			O	-	RTS — Request To Send output for UART.
			I	-	CT32B0_CAP0 — Capture input 0 for 32-bit timer 0.

Table 8. LPC1100 and LPC1100L series: LPC1113/14 pin description table (LQFP48 package) ...continued

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO1_6/RXD/ CT32B0_MAT0	46 ^[3]	no	I/O	I; PU	PIO1_6 — General purpose digital input/output pin.
			I	-	RXD — Receiver input for UART.
			O	-	CT32B0_MAT0 — Match output 0 for 32-bit timer 0.
PIO1_7/TXD/ CT32B0_MAT1	47 ^[3]	no	I/O	I; PU	PIO1_7 — General purpose digital input/output pin.
			O	-	TXD — Transmitter output for UART.
			O	-	CT32B0_MAT1 — Match output 1 for 32-bit timer 0.
PIO1_8/ CT16B1_CAP0	9 ^[3]	no	I/O	I; PU	PIO1_8 — General purpose digital input/output pin.
			I	-	CT16B1_CAP0 — Capture input 0 for 16-bit timer 1.
PIO1_9/ CT16B1_MAT0	17 ^[3]	no	I/O	I; PU	PIO1_9 — General purpose digital input/output pin.
			O	-	CT16B1_MAT0 — Match output 0 for 16-bit timer 1.
PIO1_10/AD6/ CT16B1_MAT1	30 ^[5]	no	I/O	I; PU	PIO1_10 — General purpose digital input/output pin.
			I	-	AD6 — A/D converter, input 6.
			O	-	CT16B1_MAT1 — Match output 1 for 16-bit timer 1.
PIO1_11/AD7	42 ^[5]	no	I/O	I; PU	PIO1_11 — General purpose digital input/output pin.
			I	-	AD7 — A/D converter, input 7.
PIO2_0 to PIO2_11			I/O		Port 2 — Port 2 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 2 pins depends on the function selected through the IOCONFIG register block.
PIO2_0/DTR/SSEL1	2 ^[3]	no	I/O	I; PU	PIO2_0 — General purpose digital input/output pin.
			O	-	DTR — Data Terminal Ready output for UART.
			I/O	-	SSEL1 — Slave Select for SPI1.
PIO2_1/DSR/SCK1	13 ^[3]	no	I/O	I; PU	PIO2_1 — General purpose digital input/output pin.
			I	-	DSR — Data Set Ready input for UART.
			I/O	-	SCK1 — Serial clock for SPI1.
PIO2_2/DCD/MISO1	26 ^[3]	no	I/O	I; PU	PIO2_2 — General purpose digital input/output pin.
			I	-	DCD — Data Carrier Detect input for UART.
			I/O	-	MISO1 — Master In Slave Out for SPI1.
PIO2_3/RI/MOSI1	38 ^[3]	no	I/O	I; PU	PIO2_3 — General purpose digital input/output pin.
			I	-	RI — Ring Indicator input for UART.
			I/O	-	MOSI1 — Master Out Slave In for SPI1.
PIO2_4	19 ^[3]	no	I/O	I; PU	PIO2_4 — General purpose digital input/output pin.
PIO2_5	20 ^[3]	no	I/O	I; PU	PIO2_5 — General purpose digital input/output pin.
PIO2_6	1 ^[3]	no	I/O	I; PU	PIO2_6 — General purpose digital input/output pin.
PIO2_7	11 ^[3]	no	I/O	I; PU	PIO2_7 — General purpose digital input/output pin.
PIO2_8	12 ^[3]	no	I/O	I; PU	PIO2_8 — General purpose digital input/output pin.
PIO2_9	24 ^[3]	no	I/O	I; PU	PIO2_9 — General purpose digital input/output pin.
PIO2_10	25 ^[3]	no	I/O	I; PU	PIO2_10 — General purpose digital input/output pin.
PIO2_11/SCK0	31 ^[3]	no	I/O	I; PU	PIO2_11 — General purpose digital input/output pin.
			I/O	-	SCK0 — Serial clock for SPI0.

Table 10. LPC1100XL series: LPC1113/14/15 pin description table (LQFP48 and TFBGA48 package) ...continued

Symbol	LQFP48	TFBGA48	Start logic input	Type	Reset state [4]	Description
PIO1_4/AD5/ CT32B1_MAT3/ WAKEUP	40 ^[5]	A6 ^[5]	no	I/O	I; PU	PIO1_4 — General purpose digital input/output pin with 10 ns glitch filter. In Deep power-down mode, this pin serves as the Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
				I	-	AD5 — A/D converter, input 5.
				O	-	CT32B1_MAT3 — Match output 3 for 32-bit timer 1.
PIO1_5/RTS/ CT32B0_CAP0	45 ^[3]	A3 ^[3]	no	I/O	I; PU	PIO1_5 — General purpose digital input/output pin.
				O	-	RTS — Request To Send output for UART.
				I	-	CT32B0_CAP0 — Capture input 0 for 32-bit timer 0.
PIO1_6/RXD/ CT32B0_MAT0	46 ^[3]	B3 ^[3]	no	I/O	I; PU	PIO1_6 — General purpose digital input/output pin.
				I	-	RXD — Receiver input for UART.
				O	-	CT32B0_MAT0 — Match output 0 for 32-bit timer 0.
PIO1_7/TXD/ CT32B0_MAT1	47 ^[3]	B2 ^[3]	no	I/O	I; PU	PIO1_7 — General purpose digital input/output pin.
				O	-	TXD — Transmitter output for UART.
				O	-	CT32B0_MAT1 — Match output 1 for 32-bit timer 0.
PIO1_8/ CT16B1_CAP0	9 ^[3]	F2 ^[3]	no	I/O	I; PU	PIO1_8 — General purpose digital input/output pin.
				I	-	CT16B1_CAP0 — Capture input 0 for 16-bit timer 1.
PIO1_9/ CT16B1_MAT0/ MOSI1	17 ^[3]	G4 ^[3]	no	I/O	I; PU	PIO1_9 — General purpose digital input/output pin.
				O	-	CT16B1_MAT0 — Match output 0 for 16-bit timer 1.
				I/O	-	MOSI1 — Master Out Slave In for SPI1.
PIO1_10/AD6/ CT16B1_MAT1/ MISO1	30 ^[5]	E8 ^[5]	no	I/O	I; PU	PIO1_10 — General purpose digital input/output pin.
				I	-	AD6 — A/D converter, input 6.
				O	-	CT16B1_MAT1 — Match output 1 for 16-bit timer 1.
				I/O	-	MISO1 — Master In Slave Out for SPI1.
PIO1_11/AD7/ CT32B1_CAP1	42 ^[5]	A5 ^[5]	no	I/O	I; PU	PIO1_11 — General purpose digital input/output pin.
				I	-	AD7 — A/D converter, input 7.
				I	-	CT32B1_CAP1 — Capture input 1 for 32-bit timer 1.
PIO2_0 to PIO2_11				I/O		Port 2 — Port 2 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 2 pins depends on the function selected through the IOCONFIG register block.
PIO2_0/DTR/SSEL1	2 ^[3]	B1 ^[3]	no	I/O	I; PU	PIO2_0 — General purpose digital input/output pin.
				O	-	DTR — Data Terminal Ready output for UART.
				I/O	-	SSEL1 — Slave Select for SPI1.
PIO2_1/DSR/SCK1	13 ^[3]	H1 ^[3]	no	I/O	I; PU	PIO2_1 — General purpose digital input/output pin.
				I	-	DSR — Data Set Ready input for UART.
				I/O	-	SCK1 — Serial clock for SPI1.

Table 11. LPC1100XL series: LPC1111/12/13/14 pin description table (HVQFN33 package) ...continued

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
V _{DD}	6; 29	-	I	-	3.3 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	4[6]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	5[6]	-	O	-	Output from the oscillator amplifier.
V _{SS}	33	-	-	-	Thermal pad. Connect to ground.

- [1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level (V_{DD} = 3.3 V)); IA = inactive, no pull-up/down enabled.
- [2] 5 V tolerant pad. **RESET** functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See [Figure 52](#) for the reset pad configuration.
- [3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see [Figure 51](#)).
- [4] I²C-bus pads compliant with the I²C-bus specification for I²C standard mode and I²C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.
- [5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled, and the pin is not 5 V tolerant (see [Figure 51](#)).
- [6] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

- In the LPC1110/11/12/13/14/15, the NVIC supports 32 vectored interrupts including up to 13 inputs to the start logic from individual GPIO pins.
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation.

7.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any GPIO pin (total of up to 42 pins) regardless of the selected function, can be programmed to generate an interrupt on a level, or rising edge or falling edge, or both.

7.6 IOCONFIG block

The IOCONFIG block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

7.7 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC1110/11/12/13/14/15 use accelerated GPIO functions:

- GPIO registers are a dedicated AHB peripheral so that the fastest possible I/O timing can be achieved.
- Entire port value can be written in one instruction.

Additionally, any GPIO pin (total of up to 42 pins) providing a digital function can be programmed to generate an interrupt on a level, a rising or falling edge, or both.

7.7.1 Features

- Bit level port registers allow a single instruction to set or clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to inputs with pull-ups enabled after reset with the exception of the I²C-bus pins PIO0_4 and PIO0_5.
- Pull-up/pull-down resistor configuration can be programmed through the IOCONFIG block for each GPIO pin (except for pins PIO0_4 and PIO0_5).
- On the LPC1100, all GPIO pins (except PIO0_4 and PIO0_5) are pulled up to 2.6 V ($V_{DD} = 3.3$ V) if their pull-up resistor is enabled in the IOCONFIG block.

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

7.16.5.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

7.16.5.3 Deep-sleep mode

In Deep-sleep mode, the chip is in Sleep mode, and in addition all analog blocks are shut down. As an exception, the user has the option to keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection. Deep-sleep mode allows for additional power savings.

Up to 13 pins total serve as external wake-up pins to the start logic to wake up the chip from Deep-sleep mode.

Unless the watchdog oscillator is selected to run in Deep-sleep mode, the clock source should be switched to IRC before entering Deep-sleep mode, because the IRC can be switched on and off glitch-free.

7.16.5.4 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip with the exception of the WAKEUP pin. The LPC1110/11/12/13/14/15 can wake up from Deep power-down mode via the WAKEUP pin.

A LOW-going pulse as short as 50 ns wakes up the part from Deep power-down mode.

When entering Deep power-down mode, an external pull-up resistor is required on the WAKEUP pin to hold it HIGH. The RESET pin must also be held HIGH to prevent it from floating while in Deep power-down mode.

7.17 System control

7.17.1 Start logic

The start logic connects external pins to corresponding interrupts in the NVIC. Each pin shown in [Table 8](#) to [Table 9](#) as input to the start logic has an individual interrupt in the NVIC interrupt vector table. The start logic pins can serve as external interrupt pins when the chip is running. In addition, an input signal on the start logic pins can wake up the chip from Deep-sleep mode when all clocks are shut down.

10.2 LPC1100XL series

Table 17. Static characteristics (LPC1100XL series)

 $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
V _{DD}	supply voltage (core and external rail)		1.8	3.3	3.6	V
LPC1100XL series (LPC111x/103/203/303/323/333) power consumption in low-current mode ^[2]						
I _{DD}	supply current	Active mode; code while(1){} executed from flash				
		system clock = 3 MHz ^{[3][4][5]} V _{DD} = 3.3 V ^{[6][7]}	-	600	-	μA
		system clock = 6 MHz ^{[3][4][5]} V _{DD} = 3.3 V ^{[6][7]}	-	850	-	μA
		system clock = 12 MHz ^{[3][4][6]} V _{DD} = 3.3 V ^{[7][8]}	-	1.4	-	mA
		system clock = 50 MHz ^{[3][4][6]} V _{DD} = 3.3 V ^{[7][9]}	-	5.8	-	mA
		Sleep mode; ^{[3][4][6]} system clock = 12 MHz ^{[7][8]} V _{DD} = 3.3 V	-	700	-	μA
		system clock = 50 MHz ^{[3][4][6]} V _{DD} = 3.3 V ^{[7][8]}	-	2.2	-	mA
		Deep-sleep mode; ^{[3][4]} V _{DD} = 3.3 V; 25 °C ^[10]	-	1.8	15	μA
		Deep-sleep mode; ^{[4][10]} V _{DD} = 3.3 V; 105 °C ^[11]	-	-	50	μA
		Deep power-down mode; ^{[3][12]} V _{DD} = 3.3 V; 25 °C	-	220	1000	nA
		Deep power-down mode; ^{[11][12]} V _{DD} = 3.3 V; 105 °C	-	-	3	μA
Standard port pins, RESET						
I _{IL}	LOW-level input current	V _I = 0 V; on-chip pull-up resistor disabled	-	0.5	10	nA
I _{IH}	HIGH-level input current	V _I = V _{DD} ; on-chip pull-down resistor disabled	-	0.5	10	nA
I _{OZ}	OFF-state output current	V _O = 0 V; V _O = V _{DD} ; on-chip pull-up/down resistors disabled	-	0.5	10	nA
V _I	input voltage	pin configured to provide a digital function ^{[13][14]} 				

11. Dynamic characteristics

11.1 Power-up ramp conditions

Table 22. Power-up characteristics^[1]

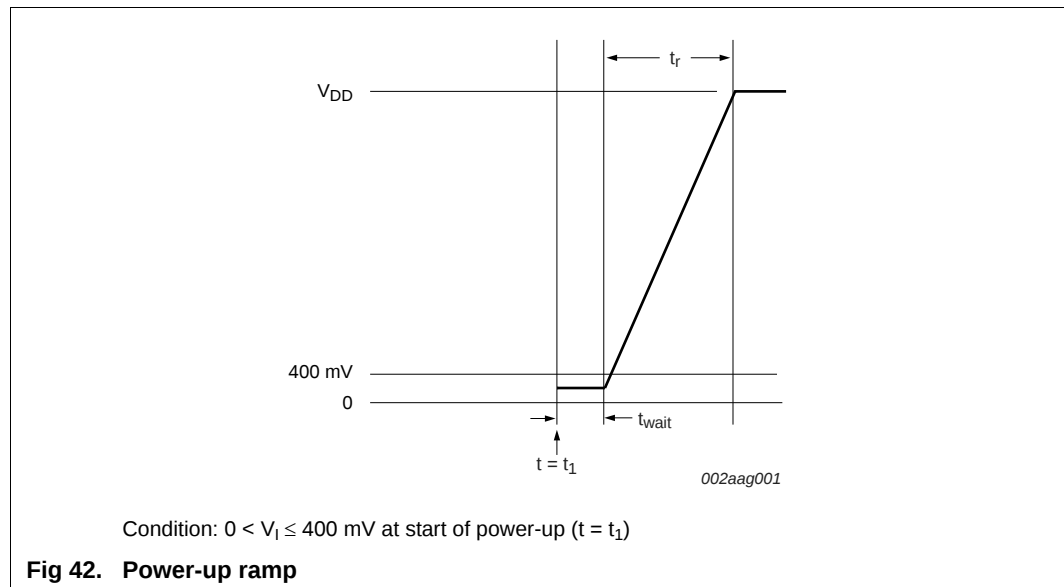
$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	at $t = t_1$: $0 < V_I \leq 400\text{ mV}$ ^[2]	0	-	500	ms
t_{wait}	wait time	^{[2][3]}	12	-	-	μs
V_I	input voltage	at $t = t_1$ on pin V_{DD}	0	-	400	mV

[1] Does not apply to the LPC1100XL series (LPC111x/103/203/303/323/333).

[2] See Figure 42.

[3] The wait time specifies the time the power supply must be at levels below 400 mV before ramping up.



11.2 Flash memory

Table 23. Flash characteristics

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$, unless otherwise specified. $T_{amb} = 85\text{ }^{\circ}\text{C}$ for flash programming.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{endu}	endurance	^[1]	10000	100000	-	cycles
t_{ret}	retention time	powered	10	-	-	years
		unpowered	20	-	-	years
t_{er}	erase time	sector or multiple consecutive sectors	95	100	105	ms
t_{prog}	programming time	^[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes. Flash programming operation temperature must not exceed $T_{amb} = 85\text{ }^{\circ}\text{C}$.

11.3 External clock

Table 24. Dynamic characteristic: external clock
T_{amb} = -40 °C to +105 °C; V_{DD} over specified ranges.^[1]

Symbol	Parameter	Conditions	Min	Typ ^[2]	Max	Unit
f _{osc}	oscillator frequency		1	-	25	MHz
T _{cy(clk)}	clock cycle time		40	-	1000	ns
t _{CHCX}	clock HIGH time		T _{cy(clk)} × 0.4	-	-	ns
t _{CLCX}	clock LOW time		T _{cy(clk)} × 0.4	-	-	ns
t _{CLCH}	clock rise time		-	-	5	ns
t _{CHCL}	clock fall time		-	-	5	ns

- [1] Parameters are valid over operating temperature range unless otherwise specified.
- [2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

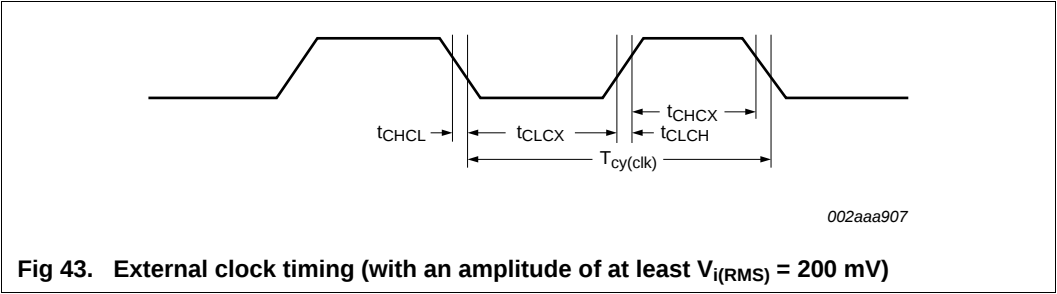


Table 26. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
$f_{\text{osc(int)}}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 ^{[2][3]} in the WDTOSCCTRL register;	-	9.4	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF ^{[2][3]} in the WDTOSCCTRL register	-	2300	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The typical frequency spread over processing and temperature ($T_{\text{amb}} = -40\text{ °C}$ to $+105\text{ °C}$) is $\pm 40\%$.

[3] See the LPC111x user manual.

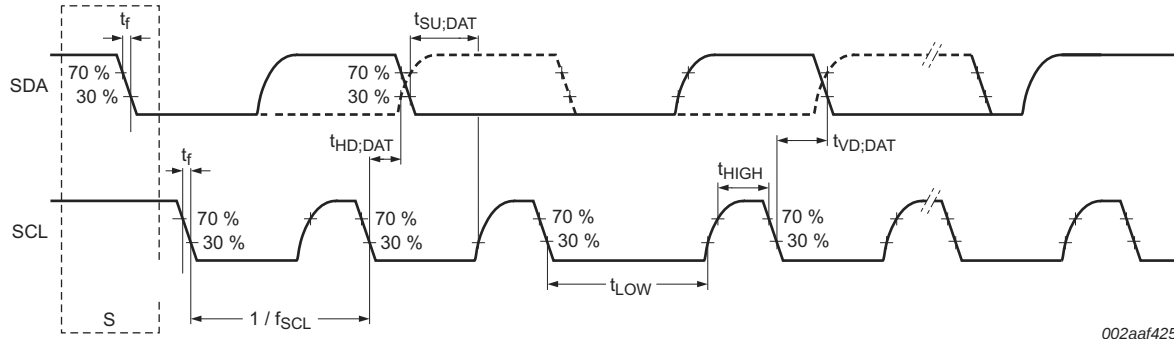
11.5 I/O pins

Table 27. Dynamic characteristic: I/O pins^[1]

$T_{\text{amb}} = -40\text{ °C}$ to $+105\text{ °C}$; $3.0\text{ V} \leq V_{\text{DD}} \leq 3.6\text{ V}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	pin configured as output	3.0	-	5.0	ns
t_f	fall time	pin configured as output	2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

Fig 46. I²C-bus pins clock timing

11.7 SPI interfaces

Table 29. Dynamic characteristics of SPI pins in SPI mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPI master (in SPI mode)						
$T_{cy(clk)}$	clock cycle time	full-duplex mode ^[1]	50	-	-	ns
		when only transmitting ^[1]	40			ns
t_{DS}	data set-up time	in SPI mode ^[2]	15	-	-	ns
		$2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$				
		$2.0\text{ V} \leq V_{DD} < 2.4\text{ V}$ ^[2]	20			ns
		$1.8\text{ V} \leq V_{DD} < 2.0\text{ V}$ ^[2]	24	-	-	ns
t_{DH}	data hold time	in SPI mode ^[2]	0	-	-	ns
$t_{V(Q)}$	data output valid time	in SPI mode ^[2]	-	-	10	ns
$t_{h(Q)}$	data output hold time	in SPI mode ^[2]	0	-	-	ns
SPI slave (in SPI mode)						
$T_{cy(PCLK)}$	PCLK cycle time		20	-	-	ns
t_{DS}	data set-up time	in SPI mode ^{[3][4]}	0	-	-	ns
t_{DH}	data hold time	in SPI mode ^{[3][4]}	$3 \times T_{cy(PCLK)} + 4$	-	-	ns
$t_{V(Q)}$	data output valid time	in SPI mode ^{[3][4]}	-	-	$3 \times T_{cy(PCLK)} + 11$	ns
$t_{h(Q)}$	data output hold time	in SPI mode ^{[3][4]}	-	-	$2 \times T_{cy(PCLK)} + 5$	ns

[1] $T_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPSPVSR) / f_{main}$. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main} , the SPI peripheral clock divider (SSPCLKDIV), the SPI SCR parameter (specified in the SSP0CR0 register), and the SPI CPSPVSR parameter (specified in the SPI clock prescale register).

[2] $T_{amb} = -40\text{ °C to }105\text{ °C}$.

[3] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$.

[4] $T_{amb} = 25\text{ °C}$; for normal voltage supply range: $V_{DD} = 3.3\text{ V}$.

12. Application information

12.1 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in [Table 18](#):

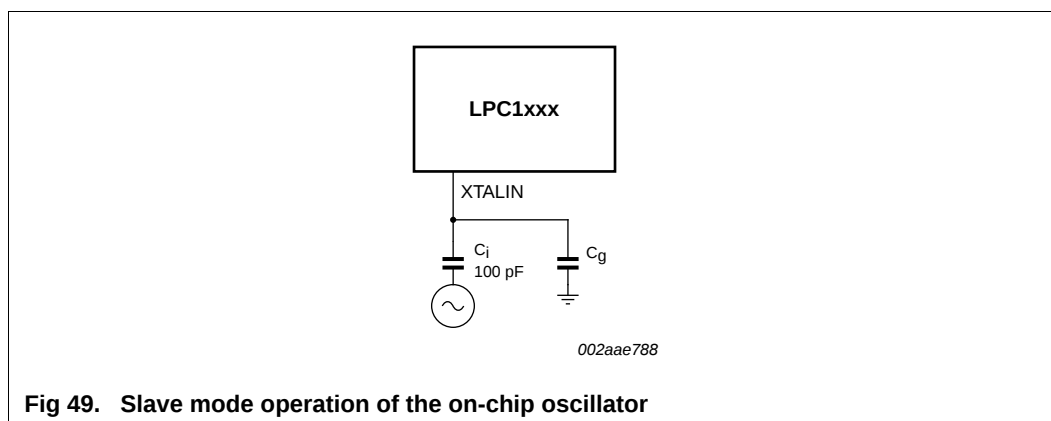
- The ADC input trace must be short and as close as possible to the LPC1110/11/12/13/14/15 chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- Because the ADC and the digital core share the same power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

12.2 Use of ADC input trigger signals

For applications that use trigger signals to start conversions and require a precise sample frequency, ensure that the period of the trigger signal is an integral multiple of the period of the ADC clock.

12.3 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with $C_i = 100$ pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV (RMS) is needed.



In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF ([Figure 49](#)), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in [Figure 50](#) and in [Table 30](#) and [Table 31](#). Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of

12.8 ADC effective input impedance

A simplified diagram of the ADC input channels can be used to determine the effective input impedance seen from an external voltage source. See [Figure 53](#).

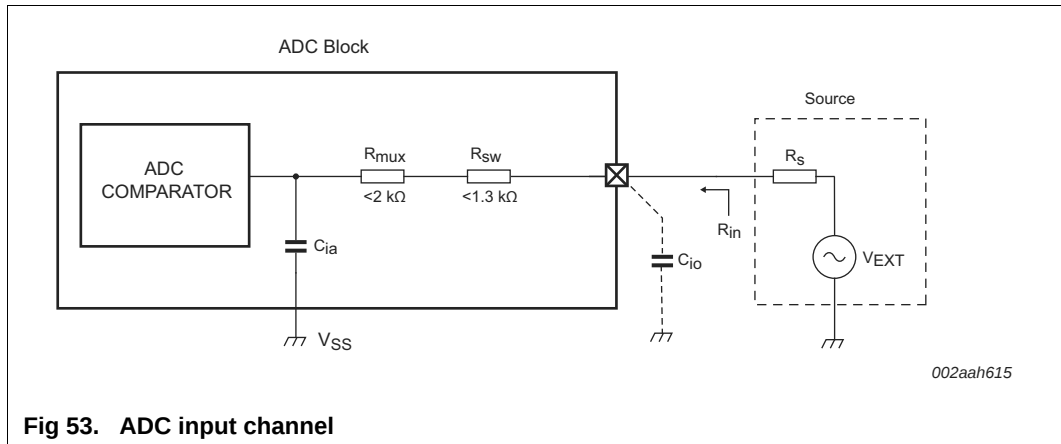


Fig 53. ADC input channel

The effective input impedance, R_{in} , seen by the external voltage source, V_{EXT} , is the parallel impedance of $((1/f_s \times C_{ia}) + R_{mux} + R_{sw})$ and $(1/f_s \times C_{io})$, and can be calculated using [Equation 2](#) with

f_s = sampling frequency

C_{ia} = ADC analog input capacitance

R_{mux} = analog mux resistance

R_{sw} = switch resistance

C_{io} = pin capacitance

$$R_{in} = \left(\frac{1}{f_s \times C_{ia}} + R_{mux} + R_{sw} \right) \parallel \left(\frac{1}{f_s \times C_{io}} \right) \quad (2)$$

Under nominal operating condition $V_{DD} = 3.3$ V and with the maximum sampling frequency $f_s = 400$ kHz, the parameters assume the following values:

$C_{ia} = 1$ pF (max)

$R_{mux} = 2$ kΩ (max)

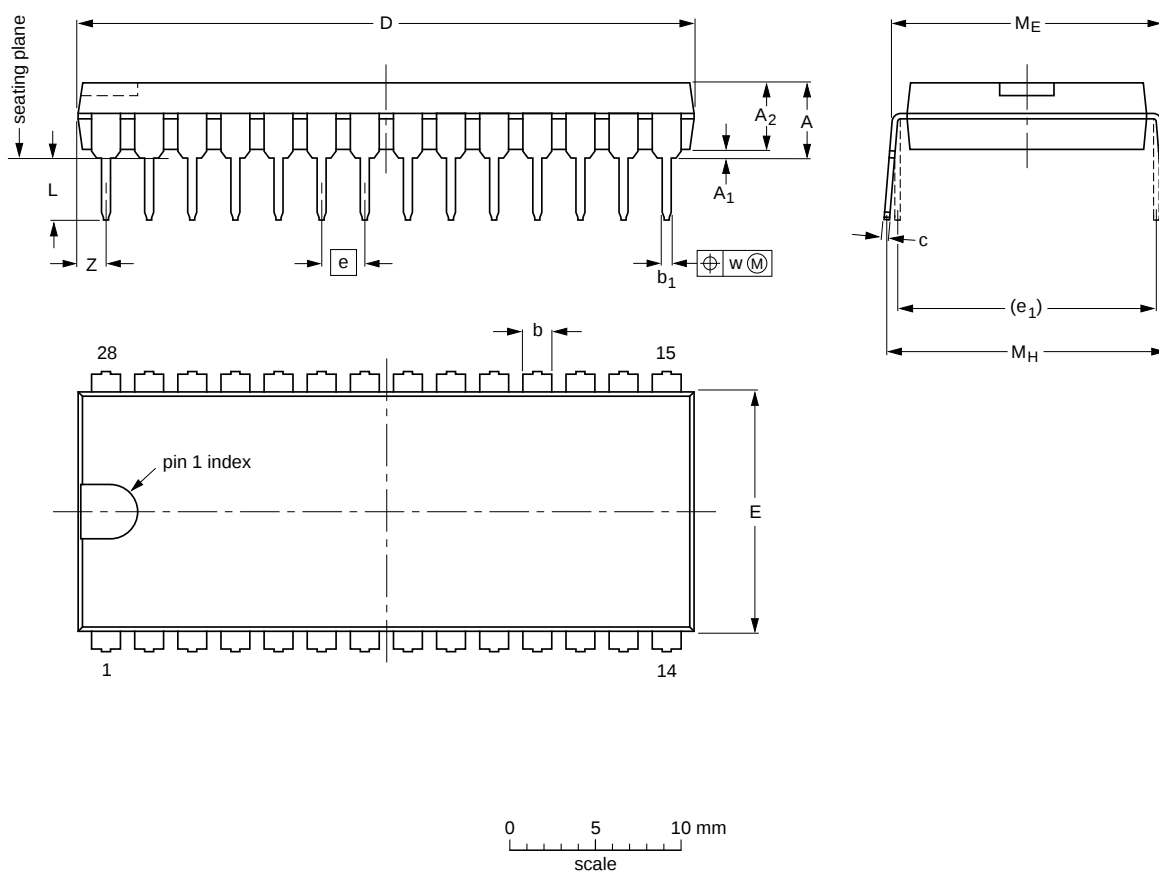
$R_{sw} = 1.3$ kΩ (max)

$C_{io} = 7.1$ pF (max)

The effective input impedance with these parameters is $R_{in} = 308$ kΩ.

DIP28: plastic dual in-line package; 28 leads (600 mil)

SOT117-1



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	5.1	0.51	4	1.7 1.3	0.53 0.38	0.32 0.23	36 35	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.2	0.02	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.1	0.6	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

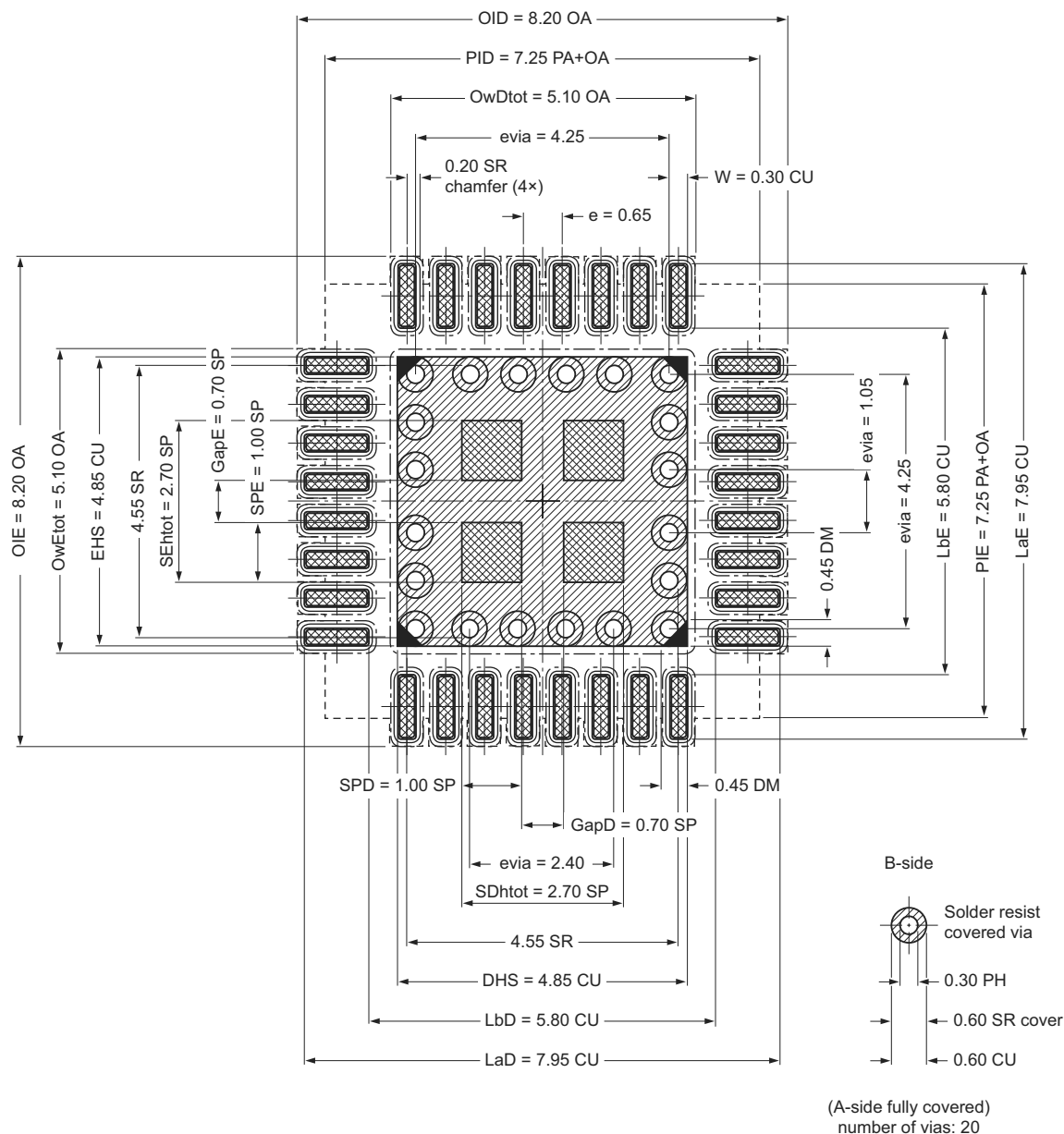
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT117-1	051G05	MO-015	SC-510-28			99-12-27 03-02-13

Fig 57. Package outline SOT117-1 (DIP28)

Footprint information for reflow soldering of HVQFN33 package



	solder land		solder land plus solder paste
	solder paste deposit		solder resist
----	occupied area		Dimensions in mm

Remark:
Stencil thickness: 0.125 mm

001aao134

Fig 68. Reflow soldering of the HVQFN33 package (7x7)

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