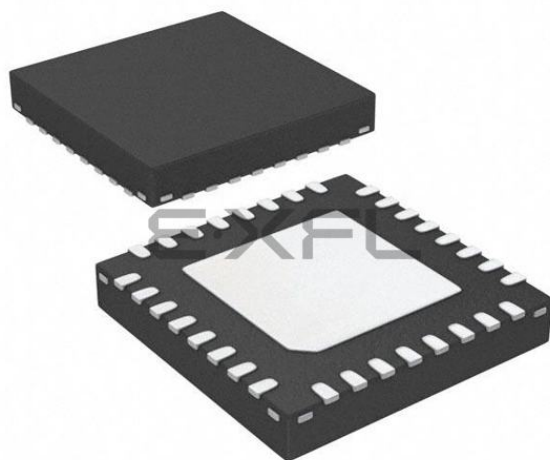




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	28
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VQFN Exposed Pad
Supplier Device Package	32-HVQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1113fhn33-303-5

Table 1. Ordering information ...continued

Type number	Package		
	Name	Description	Version
LPC1114FHI33/302	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC1114FHI33/303	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC1114JHI33/303	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	n/a
LPC1114FHN33/203	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1114JHN33/203	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1114FHN33/303	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1114JHN33/303	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1114FHN33/333	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1114JHN33/333	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1113FBD48/301	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1113FBD48/302	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1113FBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1113JBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114FBD48/301	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114FBD48/302	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114FBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114JBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114FBD48/323	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114JBD48/323	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114FBD48/333	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1114JBD48/333	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1115FBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

Table 3. Pin description overview

Part	Pin description table	Pinning diagram
LPC1114FHN33/203	Table 11	Figure 7
LPC1114JHN33/203	Table 11	Figure 7
LPC1114FHN33/301	Table 9	Figure 6
LPC1114FHN33/302	Table 9	Figure 6
LPC1114JHN33/303	Table 11	Figure 7
LPC1114FHN33/303	Table 11	Figure 7
LPC1114FHN33/333	Table 11	Figure 7
LPC1114JHN33/333	Table 11	Figure 7
LPC1114FHI33/302	Table 9	Figure 6
LPC1114FHI33/303	Table 11	Figure 7
LPC1114JHI33/303	Table 11	Figure 7
LPC1113FBD48/301	Table 8	Figure 3
LPC1113FBD48/302	Table 8	Figure 3
LPC1113FBD48/303	Table 10	Figure 4
LPC1113JBD48/303	Table 10	Figure 4
LPC1114FBD48/301	Table 8	Figure 3
LPC1114FBD48/302	Table 8	Figure 3
LPC1114FBD48/303	Table 10	Figure 4
LPC1114JBD48/303	Table 10	Figure 4
LPC1114FBD48/323	Table 10	Figure 4
LPC1114JBD48/323	Table 10	Figure 4
LPC1114FBD48/333	Table 10	Figure 4
LPC1114JBD48/333	Table 10	Figure 4
LPC1115FBD48/303	Table 10	Figure 4
LPC1115JBD48/303	Table 10	Figure 4
LPC1115FET48/303	Table 10	Figure 5
LPC1115JET48/303	Table 10	Figure 5

6.2 Pin description

Table 4. LPC1100L series: LPC1110/11/12 pin description table (SO20 and TSSOP20 package with I²C-bus pins)

Symbol	Pin SO20/ TSSOP20	Start logic input	Type	Reset state [1]	Description
PIO0_0 to PIO0_11			I/O		Port 0 — Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.
RESET/PIO0_0	17 [2]	yes	I	I; PU	RESET — External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The RESET pin can be left unconnected or be used as a GPIO pin if an external RESET function is not needed and Deep power-down mode is not used.
			I/O	-	PIO0_0 — General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/ CT32B0_MAT2	18 [3]	yes	I/O	I; PU	PIO0_1 — General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
			O	-	CLKOUT — Clockout pin.
			O	-	CT32B0_MAT2 — Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	19 [3]	yes	I/O	I; PU	PIO0_2 — General purpose digital input/output pin.
			I/O	-	SSEL0 — Slave Select for SPI0.
			I	-	CT16B0_CAP0 — Capture input 0 for 16-bit timer 0.
PIO0_4/SCL	20 [4]	yes	I/O	I; IA	PIO0_4 — General purpose digital input/output pin (open-drain).
			I/O	-	SCL — I ² C-bus, open-drain clock input/output. High-current sink only if I ² C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	5 [4]	yes	I/O	I; IA	PIO0_5 — General purpose digital input/output pin (open-drain).
			I/O	-	SDA — I ² C-bus, open-drain data input/output. High-current sink only if I ² C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	6 [3]	yes	I/O	I; PU	PIO0_6 — General purpose digital input/output pin.
			I/O	-	SCK0 — Serial clock for SPI0.
PIO0_8/MISO0/ CT16B0_MAT0	1 [3]	yes	I/O	I; PU	PIO0_8 — General purpose digital input/output pin.
			I/O	-	MISO0 — Master In Slave Out for SPI0.
			O	-	CT16B0_MAT0 — Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	2 [3]	yes	I/O	I; PU	PIO0_9 — General purpose digital input/output pin.
			I/O	-	MOSI0 — Master Out Slave In for SPI0.
			O	-	CT16B0_MAT1 — Match output 1 for 16-bit timer 0.
SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2	3 [3]	yes	I	I; PU	SWCLK — Serial wire clock.
			I/O	-	PIO0_10 — General purpose digital input/output pin.
			I/O	-	SCK0 — Serial clock for SPI0.
			O	-	CT16B0_MAT2 — Match output 2 for 16-bit timer 0.

Table 5. LPC1100L series: LPC1112 pin description table (TSSOP20 with V_{DDA} and V_{SSA} pins) ...continued

Symbol	Pin TSSOP20	Start logic input	Type	Reset state [1]	Description
V _{DDA}	5	-	I	-	3.3 V supply voltage to the ADC. Also used as the ADC reference voltage.
XTALIN	14 [5]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	13 [5]	-	O	-	Output from the oscillator amplifier.
V _{SS}	16	-	I	-	Ground.
V _{SSA}	6	-	I	-	Analog ground.

- [1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level); IA = inactive, no pull-up/down enabled.
- [2] 5 V tolerant pad. RESET functionality is not available in Deep power-down mode.
- [3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 51).
- [4] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 51).
- [5] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

Table 6. LPC1100L series: LPC1112 (HVQFN24 package)

Symbol	HVQFN pin	Start logic input	Type	Reset state [1]	Description
RESET/PIO0_0	1[2]	yes	I	I; PU	RESET — External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The RESET pin can be left unconnected or be used as a GPIO pin if an external RESET function is not needed and Deep power-down mode is not used.
			I/O	-	PIO0_0 — General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/CT32B0_MAT2	2[3]	yes	I/O	I; PU	PIO0_1 — General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
			O	-	CLKOUT — Clockout pin.
			O	-	CT32B0_MAT2 — Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/CT16B0_CAP0	7[3]	yes	I/O	I; PU	PIO0_2 — General purpose digital input/output pin.
			I/O	-	SSEL0 — Slave Select for SPI0.
			I	-	CT16B0_CAP0 — Capture input 0 for 16-bit timer 0.
PIO0_4/SCL	8[4]	yes	I/O	I; IA	PIO0_4 — General purpose digital input/output pin (open-drain).
			I/O	-	SCL — I ² C-bus, open-drain clock input/output. High-current sink only if I ² C Fast-mode Plus is selected in the I/O configuration register.

Table 7. LPC1100L series: LPC1112/14 pin description table (TSSOP28 and DIP28 packages) ...continued

Symbol	Pin TSSOP28/ DIP28	Start logic input	Type	Reset state [1]	Description
SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2	3 [3]	yes	I	I; PU	SWCLK — Serial wire clock.
			I/O	-	PIO0_10 — General purpose digital input/output pin.
			I/O	-	SCK0 — Serial clock for SPI0.
			O	-	CT16B0_MAT2 — Match output 2 for 16-bit timer 0.
R/PIO0_11/ AD0/CT32B0_MAT3	4 [5]	yes	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO0_11 — General purpose digital input/output pin.
			I	-	AD0 — A/D converter, input 0.
			O	-	CT32B0_MAT3 — Match output 3 for 32-bit timer 0.
PIO1_0 to PIO1_9			I/O		Port 1 — Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block.
R/PIO1_0/ AD1/CT32B1_CAP0	9 [5]	yes	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_0 — General purpose digital input/output pin.
			I	-	AD1 — A/D converter, input 1.
			I	-	CT32B1_CAP0 — Capture input 0 for 32-bit timer 1.
R/PIO1_1/ AD2/CT32B1_MAT0	10 [5]	no	O	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_1 — General purpose digital input/output pin.
			I	-	AD2 — A/D converter, input 2.
			O	-	CT32B1_MAT0 — Match output 0 for 32-bit timer 1.
R/PIO1_2/ AD3/CT32B1_MAT1	11 [5]	no	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_2 — General purpose digital input/output pin.
			I	-	AD3 — A/D converter, input 3.
			O	-	CT32B1_MAT1 — Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ AD4/CT32B1_MAT2	12 [5]	no	I/O	I; PU	SWDIO — Serial wire debug input/output.
			I/O	-	PIO1_3 — General purpose digital input/output pin.
			I	-	AD4 — A/D converter, input 4.
			O	-	CT32B1_MAT2 — Match output 2 for 32-bit timer 1.
PIO1_4/AD5/ CT32B1_MAT3/ WAKEUP	13 [5]	no	I/O	I; PU	PIO1_4 — General purpose digital input/output pin with 10 ns glitch filter. In Deep power-down mode, this pin serves as the Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
			I	-	AD5 — A/D converter, input 5.
			O	-	CT32B1_MAT3 — Match output 3 for 32-bit timer 1.

Table 8. LPC1100 and LPC1100L series: LPC1113/14 pin description table (LQFP48 package) ...continued

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2	29 ^[3]	yes	I	I; PU	SWCLK — Serial wire clock.
			I/O	-	PIO0_10 — General purpose digital input/output pin.
			I/O	-	SCK0 — Serial clock for SPI0.
			O	-	CT16B0_MAT2 — Match output 2 for 16-bit timer 0.
R/PIO0_11/ AD0/CT32B0_MAT3	32 ^[5]	yes	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO0_11 — General purpose digital input/output pin.
			I	-	AD0 — A/D converter, input 0.
			O	-	CT32B0_MAT3 — Match output 3 for 32-bit timer 0.
PIO1_0 to PIO1_11			I/O		Port 1 — Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block.
R/PIO1_0/ AD1/CT32B1_CAP0	33 ^[5]	yes	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_0 — General purpose digital input/output pin.
			I	-	AD1 — A/D converter, input 1.
			I	-	CT32B1_CAP0 — Capture input 0 for 32-bit timer 1.
R/PIO1_1/ AD2/CT32B1_MAT0	34 ^[5]	no	O	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_1 — General purpose digital input/output pin.
			I	-	AD2 — A/D converter, input 2.
			O	-	CT32B1_MAT0 — Match output 0 for 32-bit timer 1.
R/PIO1_2/ AD3/CT32B1_MAT1	35 ^[5]	no	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_2 — General purpose digital input/output pin.
			I	-	AD3 — A/D converter, input 3.
			O	-	CT32B1_MAT1 — Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ AD4/CT32B1_MAT2	39 ^[5]	no	I/O	I; PU	SWDIO — Serial wire debug input/output.
			I/O	-	PIO1_3 — General purpose digital input/output pin.
			I	-	AD4 — A/D converter, input 4.
			O	-	CT32B1_MAT2 — Match output 2 for 32-bit timer 1.
PIO1_4/AD5/ CT32B1_MAT3/ WAKEUP	40 ^[5]	no	I/O	I; PU	PIO1_4 — General purpose digital input/output pin with 10 ns glitch filter. In Deep power-down mode, this pin serves as the Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
			I	-	AD5 — A/D converter, input 5.
			O	-	CT32B1_MAT3 — Match output 3 for 32-bit timer 1.
PIO1_5/RTS/ CT32B0_CAP0	45 ^[3]	no	I/O	I; PU	PIO1_5 — General purpose digital input/output pin.
			O	-	RTS — Request To Send output for UART.
			I	-	CT32B0_CAP0 — Capture input 0 for 32-bit timer 0.

Table 8. LPC1100 and LPC1100L series: LPC1113/14 pin description table (LQFP48 package) ...continued

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO3_0 to PIO3_5			I/O		Port 3 — Port 3 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 3 pins depends on the function selected through the IOCONFIG register block. Pins PIO3_6 to PIO3_11 are not available.
PIO3_0/ $\overline{\text{DTR}}$	36 ^[3]	no	I/O	I; PU	PIO3_0 — General purpose digital input/output pin.
			O	-	DTR — Data Terminal Ready output for UART.
PIO3_1/ $\overline{\text{DSR}}$	37 ^[3]	no	I/O	I; PU	PIO3_1 — General purpose digital input/output pin.
			I	-	DSR — Data Set Ready input for UART.
PIO3_2/ $\overline{\text{DCD}}$	43 ^[3]	no	I/O	I; PU	PIO3_2 — General purpose digital input/output pin.
			I	-	DCD — Data Carrier Detect input for UART.
PIO3_3/ $\overline{\text{RI}}$	48 ^[3]	no	I/O	I; PU	PIO3_3 — General purpose digital input/output pin.
			I	-	RI — Ring Indicator input for UART.
PIO3_4	18 ^[3]	no	I/O	I; PU	PIO3_4 — General purpose digital input/output pin.
PIO3_5	21 ^[3]	no	I/O	I; PU	PIO3_5 — General purpose digital input/output pin.
V _{DD}	8; 44	-	I	-	3.3 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	6 ^[6]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	7 ^[6]	-	O	-	Output from the oscillator amplifier.
V _{SS}	5; 41	-	I	-	Ground.

- [1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to 2.6 V for LPC111x/101/201/301, pins pulled up to full V_{DD} level on LPC111x/002/102/202/302 (V_{DD} = 3.3 V)); IA = inactive, no pull-up/down enabled.
- [2] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See [Figure 52](#) for the reset pad configuration.
- [3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see [Figure 51](#)).
- [4] I²C-bus pads compliant with the I²C-bus specification for I²C standard mode and I²C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I²C lines. Open-drain configuration applies to all functions on this pin.
- [5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see [Figure 51](#)).
- [6] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

Table 9. LPC1100 and LPC1100L series: LPC1111/12/13/14 pin description table (HVQFN33 package) ...continued

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO1_7/TXD/ CT32B0_MAT1	32 ^[3]	no	I/O	I;PU	PIO1_7 — General purpose digital input/output pin.
			O	-	TXD — Transmitter output for UART.
			O	-	CT32B0_MAT1 — Match output 1 for 32-bit timer 0.
PIO1_8/ CT16B1_CAP0	7 ^[3]	no	I/O	I;PU	PIO1_8 — General purpose digital input/output pin.
			I	-	CT16B1_CAP0 — Capture input 0 for 16-bit timer 1.
PIO1_9/ CT16B1_MAT0	12 ^[3]	no	I/O	I;PU	PIO1_9 — General purpose digital input/output pin.
			O	-	CT16B1_MAT0 — Match output 0 for 16-bit timer 1.
PIO1_10/AD6/ CT16B1_MAT1	20 ^[5]	no	I/O	I;PU	PIO1_10 — General purpose digital input/output pin.
			I	-	AD6 — A/D converter, input 6.
			O	-	CT16B1_MAT1 — Match output 1 for 16-bit timer 1.
PIO1_11/AD7	27 ^[5]	no	I/O	I;PU	PIO1_11 — General purpose digital input/output pin.
			I	-	AD7 — A/D converter, input 7.
PIO2_0					Port 2 — Port 2 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 2 pins depends on the function selected through the IOCONFIG register block. Pins PIO2_1 to PIO2_11 are not available.
PIO2_0/DTR	1 ^[3]	no	I/O	I;PU	PIO2_0 — General purpose digital input/output pin.
			O	-	DTR — Data Terminal Ready output for UART.
PIO3_0 to PIO3_5					Port 3 — Port 3 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 3 pins depends on the function selected through the IOCONFIG register block. Pins PIO3_0, PIO3_1, PIO3_3 and PIO3_6 to PIO3_11 are not available.
PIO3_2	28 ^[3]	no	I/O	I;PU	PIO3_2 — General purpose digital input/output pin.
PIO3_4	13 ^[3]	no	I/O	I;PU	PIO3_4 — General purpose digital input/output pin.
PIO3_5	14 ^[3]	no	I/O	I;PU	PIO3_5 — General purpose digital input/output pin.
V _{DD}	6; 29	-	I	-	3.3 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	4 ^[6]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	5 ^[6]	-	O	-	Output from the oscillator amplifier.
V _{SS}	33	-	-	-	Thermal pad. Connect to ground.

- [1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to 2.6 V for LPC111x/101/201/301, pins pulled up to full V_{DD} level on LPC111x/002/102/202/302 (V_{DD} = 3.3 V)); IA = inactive, no pull-up/down enabled.
- [2] 5 V tolerant pad. **RESET** functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See [Figure 52](#) for the reset pad configuration.
- [3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see [Figure 51](#)).
- [4] I²C-bus pads compliant with the I²C-bus specification for I²C standard mode and I²C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.
- [5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled, and the pin is not 5 V tolerant (see [Figure 51](#)).

[6] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

Table 10. LPC1100XL series: LPC1113/14/15 pin description table (LQFP48 and TFBGA48 package)

Symbol	LQFP48	TFBGA48	Start logic input	Type	Reset state [1]	Description
PIO0_0 to PIO0_11				I/O		Port 0 — Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.
RESET/PIO0_0	3[2]	C1[2]	yes	I	I; PU	RESET — External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The RESET pin can be left unconnected or be used as a GPIO pin if an external RESET function is not needed and Deep power-down mode is not used.
				I/O	-	PIO0_0 — General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/CT32B0_MAT2	4[3]	C2[3]	yes	I/O	I; PU	PIO0_1 — General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
				O	-	CLKOUT — Clockout pin.
				O	-	CT32B0_MAT2 — Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/CT16B0_CAP0	10[3]	F1[3]	yes	I/O	I; PU	PIO0_2 — General purpose digital input/output pin.
				I/O	-	SSEL0 — Slave Select for SPI0.
				I	-	CT16B0_CAP0 — Capture input 0 for 16-bit timer 0.
PIO0_3	14[3]	H2[3]	yes	I/O	I; PU	PIO0_3 — General purpose digital input/output pin.
PIO0_4/SCL	15[4]	G3[4]	yes	I/O	I; IA	PIO0_4 — General purpose digital input/output pin (open-drain).
				I/O	-	SCL — I ² C-bus, open-drain clock input/output. High-current sink only if I ² C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	16[4]	H3[4]	yes	I/O	I; IA	PIO0_5 — General purpose digital input/output pin (open-drain).
				I/O	-	SDA — I ² C-bus, open-drain data input/output. High-current sink only if I ² C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	22[3]	H6[3]	yes	I/O	I; PU	PIO0_6 — General purpose digital input/output pin.
				I/O	-	SCK0 — Serial clock for SPI0.
PIO0_7/CTS	23[3]	G7[3]	yes	I/O	I; PU	PIO0_7 — General purpose digital input/output pin (high-current output driver).
				I	-	CTS — Clear To Send input for UART.

Table 10. LPC1100XL series: LPC1113/14/15 pin description table (LQFP48 and TFBGA48 package) ...continued

Symbol	LQFP48	TFBGA48	Start logic input	Type	Reset state [1]	Description
PIO1_4/AD5/ CT32B1_MAT3/ WAKEUP	40 ^[5]	A6 ^[5]	no	I/O	I; PU	PIO1_4 — General purpose digital input/output pin with 10 ns glitch filter. In Deep power-down mode, this pin serves as the Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
				I	-	AD5 — A/D converter, input 5.
				O	-	CT32B1_MAT3 — Match output 3 for 32-bit timer 1.
PIO1_5/RTS/ CT32B0_CAP0	45 ^[3]	A3 ^[3]	no	I/O	I; PU	PIO1_5 — General purpose digital input/output pin.
				O	-	RTS — Request To Send output for UART.
				I	-	CT32B0_CAP0 — Capture input 0 for 32-bit timer 0.
PIO1_6/RXD/ CT32B0_MAT0	46 ^[3]	B3 ^[3]	no	I/O	I; PU	PIO1_6 — General purpose digital input/output pin.
				I	-	RXD — Receiver input for UART.
				O	-	CT32B0_MAT0 — Match output 0 for 32-bit timer 0.
PIO1_7/TXD/ CT32B0_MAT1	47 ^[3]	B2 ^[3]	no	I/O	I; PU	PIO1_7 — General purpose digital input/output pin.
				O	-	TXD — Transmitter output for UART.
				O	-	CT32B0_MAT1 — Match output 1 for 32-bit timer 0.
PIO1_8/ CT16B1_CAP0	9 ^[3]	F2 ^[3]	no	I/O	I; PU	PIO1_8 — General purpose digital input/output pin.
				I	-	CT16B1_CAP0 — Capture input 0 for 16-bit timer 1.
PIO1_9/ CT16B1_MAT0/ MOSI1	17 ^[3]	G4 ^[3]	no	I/O	I; PU	PIO1_9 — General purpose digital input/output pin.
				O	-	CT16B1_MAT0 — Match output 0 for 16-bit timer 1.
				I/O	-	MOSI1 — Master Out Slave In for SPI1.
PIO1_10/AD6/ CT16B1_MAT1/ MISO1	30 ^[5]	E8 ^[5]	no	I/O	I; PU	PIO1_10 — General purpose digital input/output pin.
				I	-	AD6 — A/D converter, input 6.
				O	-	CT16B1_MAT1 — Match output 1 for 16-bit timer 1.
				I/O	-	MISO1 — Master In Slave Out for SPI1.
PIO1_11/AD7/ CT32B1_CAP1	42 ^[5]	A5 ^[5]	no	I/O	I; PU	PIO1_11 — General purpose digital input/output pin.
				I	-	AD7 — A/D converter, input 7.
				I	-	CT32B1_CAP1 — Capture input 1 for 32-bit timer 1.
PIO2_0 to PIO2_11				I/O		Port 2 — Port 2 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 2 pins depends on the function selected through the IOCONFIG register block.
PIO2_0/DTR/SSEL1	2 ^[3]	B1 ^[3]	no	I/O	I; PU	PIO2_0 — General purpose digital input/output pin.
				O	-	DTR — Data Terminal Ready output for UART.
				I/O	-	SSEL1 — Slave Select for SPI1.
PIO2_1/DSR/SCK1	13 ^[3]	H1 ^[3]	no	I/O	I; PU	PIO2_1 — General purpose digital input/output pin.
				I	-	DSR — Data Set Ready input for UART.
				I/O	-	SCK1 — Serial clock for SPI1.

Table 11. LPC1100XL series: LPC1111/12/13/14 pin description table (HVQFN33 package) ...continued

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
V _{DD}	6; 29	-	I	-	3.3 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	4[6]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	5[6]	-	O	-	Output from the oscillator amplifier.
V _{SS}	33	-	-	-	Thermal pad. Connect to ground.

- [1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level (V_{DD} = 3.3 V)); IA = inactive, no pull-up/down enabled.
- [2] 5 V tolerant pad. **RESET** functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See [Figure 52](#) for the reset pad configuration.
- [3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see [Figure 51](#)).
- [4] I²C-bus pads compliant with the I²C-bus specification for I²C standard mode and I²C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.
- [5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled, and the pin is not 5 V tolerant (see [Figure 51](#)).
- [6] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

10.2 LPC1100XL series

Table 17. Static characteristics (LPC1100XL series)

 $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
V _{DD}	supply voltage (core and external rail)		1.8	3.3	3.6	V
LPC1100XL series (LPC111x/103/203/303/323/333) power consumption in low-current mode ^[2]						
I _{DD}	supply current	Active mode; code while(1){} executed from flash				
		system clock = 3 MHz ^{[3][4][5]} V _{DD} = 3.3 V ^{[6][7]}	-	600	-	μA
		system clock = 6 MHz ^{[3][4][5]} V _{DD} = 3.3 V ^{[6][7]}	-	850	-	μA
		system clock = 12 MHz ^{[3][4][6]} V _{DD} = 3.3 V ^{[7][8]}	-	1.4	-	mA
		system clock = 50 MHz ^{[3][4][6]} V _{DD} = 3.3 V ^{[7][9]}	-	5.8	-	mA
		Sleep mode; ^{[3][4][6]} system clock = 12 MHz ^{[7][8]} V _{DD} = 3.3 V	-	700	-	μA
		system clock = 50 MHz ^{[3][4][6]} V _{DD} = 3.3 V ^{[7][8]}	-	2.2	-	mA
		Deep-sleep mode; ^{[3][4]} V _{DD} = 3.3 V; 25 °C ^[10]	-	1.8	15	μA
		Deep-sleep mode; ^{[4][10]} V _{DD} = 3.3 V; 105 °C ^[11]	-	-	50	μA
		Deep power-down mode; ^{[3][12]} V _{DD} = 3.3 V; 25 °C	-	220	1000	nA
		Deep power-down mode; ^{[11][12]} V _{DD} = 3.3 V; 105 °C	-	-	3	μA
Standard port pins, RESET						
I _{IL}	LOW-level input current	V _I = 0 V; on-chip pull-up resistor disabled	-	0.5	10	nA
I _{IH}	HIGH-level input current	V _I = V _{DD} ; on-chip pull-down resistor disabled	-	0.5	10	nA
I _{OZ}	OFF-state output current	V _O = 0 V; V _O = V _{DD} ; on-chip pull-up/down resistors disabled	-	0.5	10	nA
V _I	input voltage	pin configured to provide a digital function ^{[13][14]} 				

10.3 ADC static characteristics

Table 18. ADC static characteristics

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$ unless otherwise specified; ADC frequency 4.5 MHz, $V_{DD} = 2.5\text{ V}$ to 3.6 V .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		0	-	V_{DD}	V
C_{ia}	analog input capacitance		-	-	1	pF
E_D	differential linearity error	[1][2]	-	-	± 1	LSB
$E_{L(adj)}$	integral non-linearity	[3]	-	-	± 1.5	LSB
E_O	offset error	[4]	-	-	± 3.5	LSB
E_G	gain error	[5]	-	-	0.6	%
E_T	absolute error	[6]	-	-	± 4	LSB
R_{vsi}	voltage source interface resistance		-	-	40	k Ω
R_i	input resistance	[7][8]	-	-	2.5	M Ω

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See [Figure 17](#).

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See [Figure 17](#).

[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See [Figure 17](#).

[5] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See [Figure 17](#).

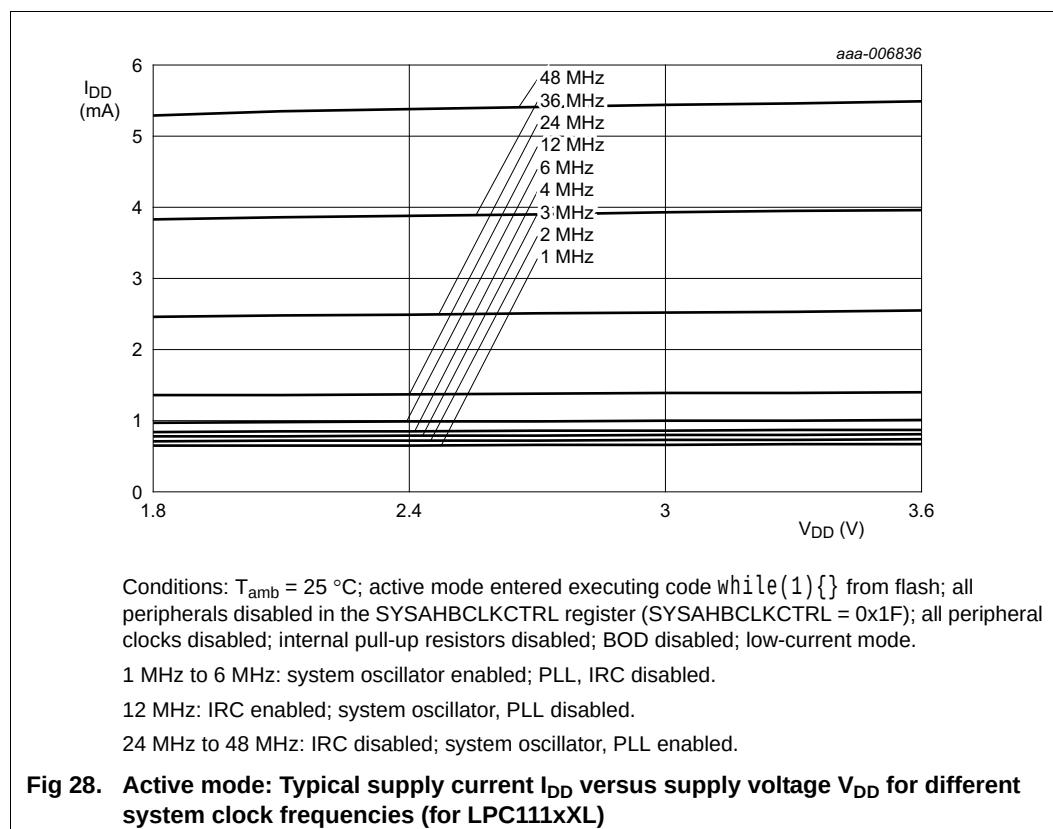
[6] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See [Figure 17](#).

[7] $T_{amb} = 25\text{ }^{\circ}\text{C}$; maximum sampling frequency $f_s = 400\text{ kSamples/s}$ and analog input capacitance $C_{ia} = 1\text{ pF}$.

[8] Input resistance R_i depends on the sampling frequency f_s : $R_i = 1 / (f_s \times C_{ia})$.

Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see *LPC111x user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCONFIG block.
- Configure GPIO pins as outputs using the GPIO_nDIR registers.
- Write 0 to all GPIO_nDATA registers to drive the outputs LOW.

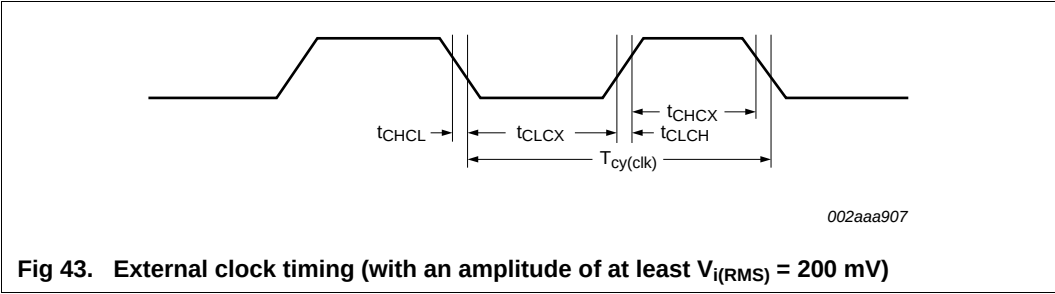


11.3 External clock

Table 24. Dynamic characteristic: external clock
T_{amb} = -40 °C to +105 °C; V_{DD} over specified ranges.^[1]

Symbol	Parameter	Conditions	Min	Typ ^[2]	Max	Unit
f _{osc}	oscillator frequency		1	-	25	MHz
T _{cy(clk)}	clock cycle time		40	-	1000	ns
t _{CHCX}	clock HIGH time		T _{cy(clk)} × 0.4	-	-	ns
t _{CLCX}	clock LOW time		T _{cy(clk)} × 0.4	-	-	ns
t _{CLCH}	clock rise time		-	-	5	ns
t _{CHCL}	clock fall time		-	-	5	ns

- [1] Parameters are valid over operating temperature range unless otherwise specified.
- [2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.



TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

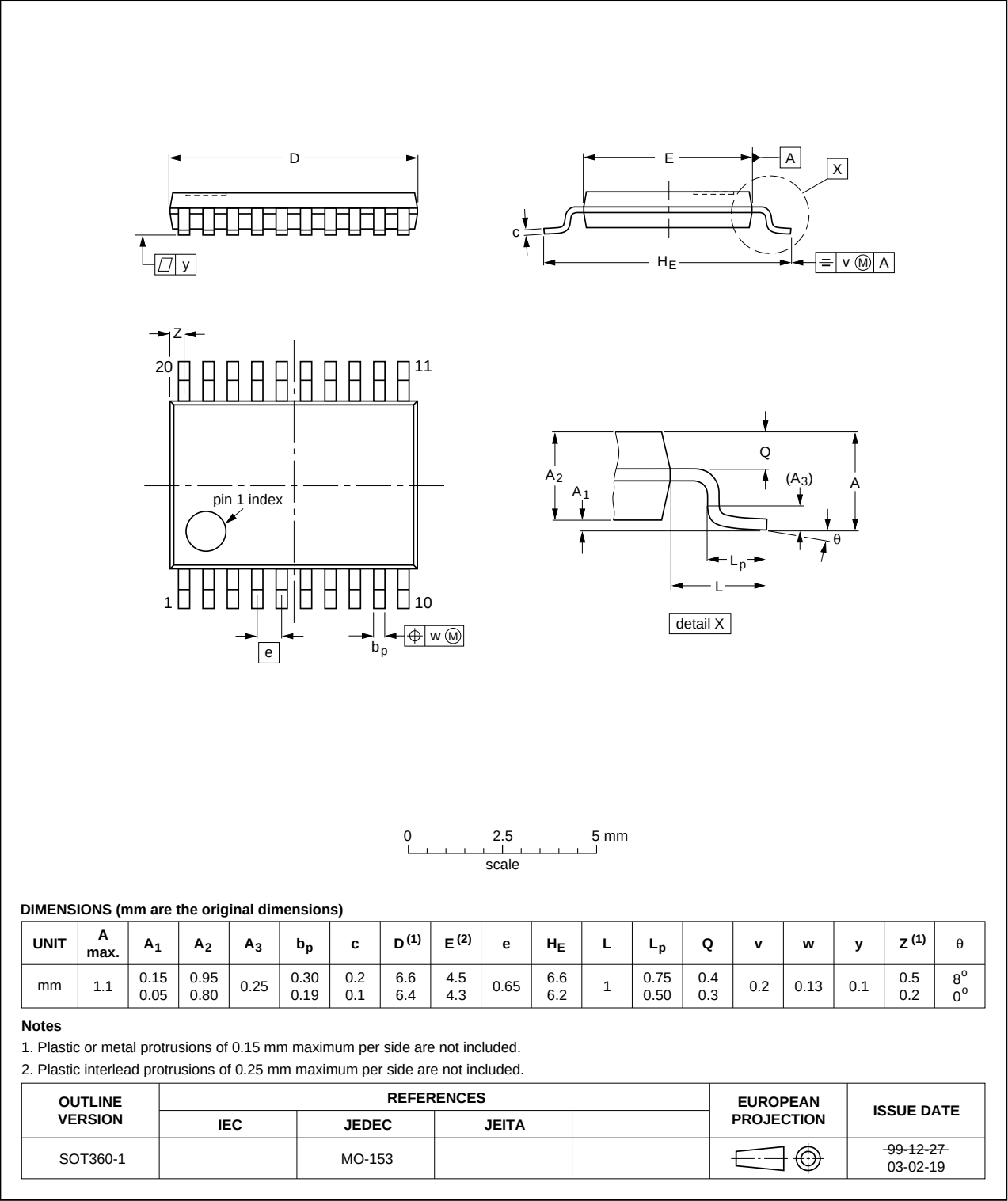


Fig 55. Package outline SOT360-1 (TSSOP20)

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads;
24 terminals; body 4 x 4 x 0.85 mm

SOT616-3

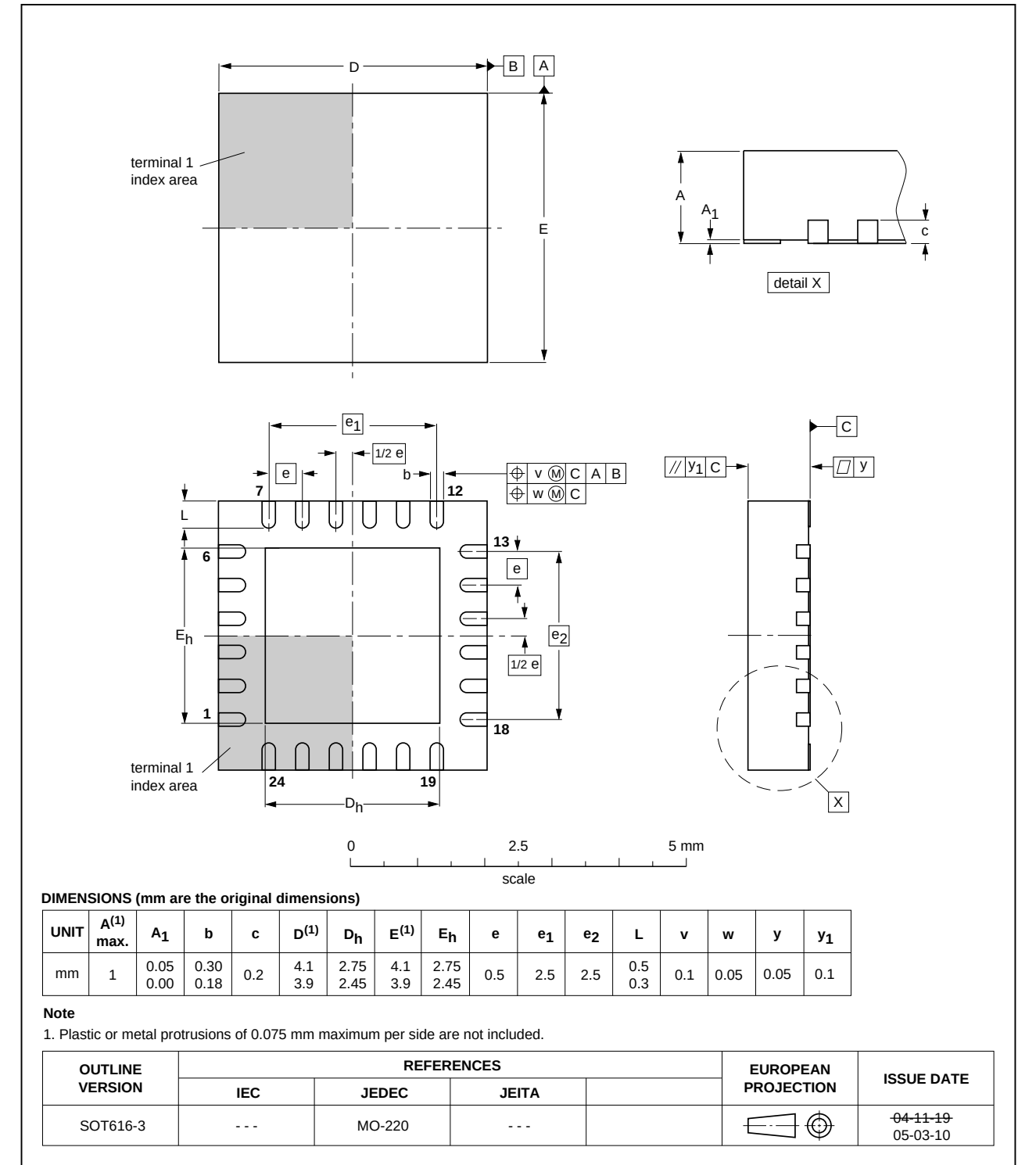


Fig 61. Package outline SOT616-3 (HVQFN24)

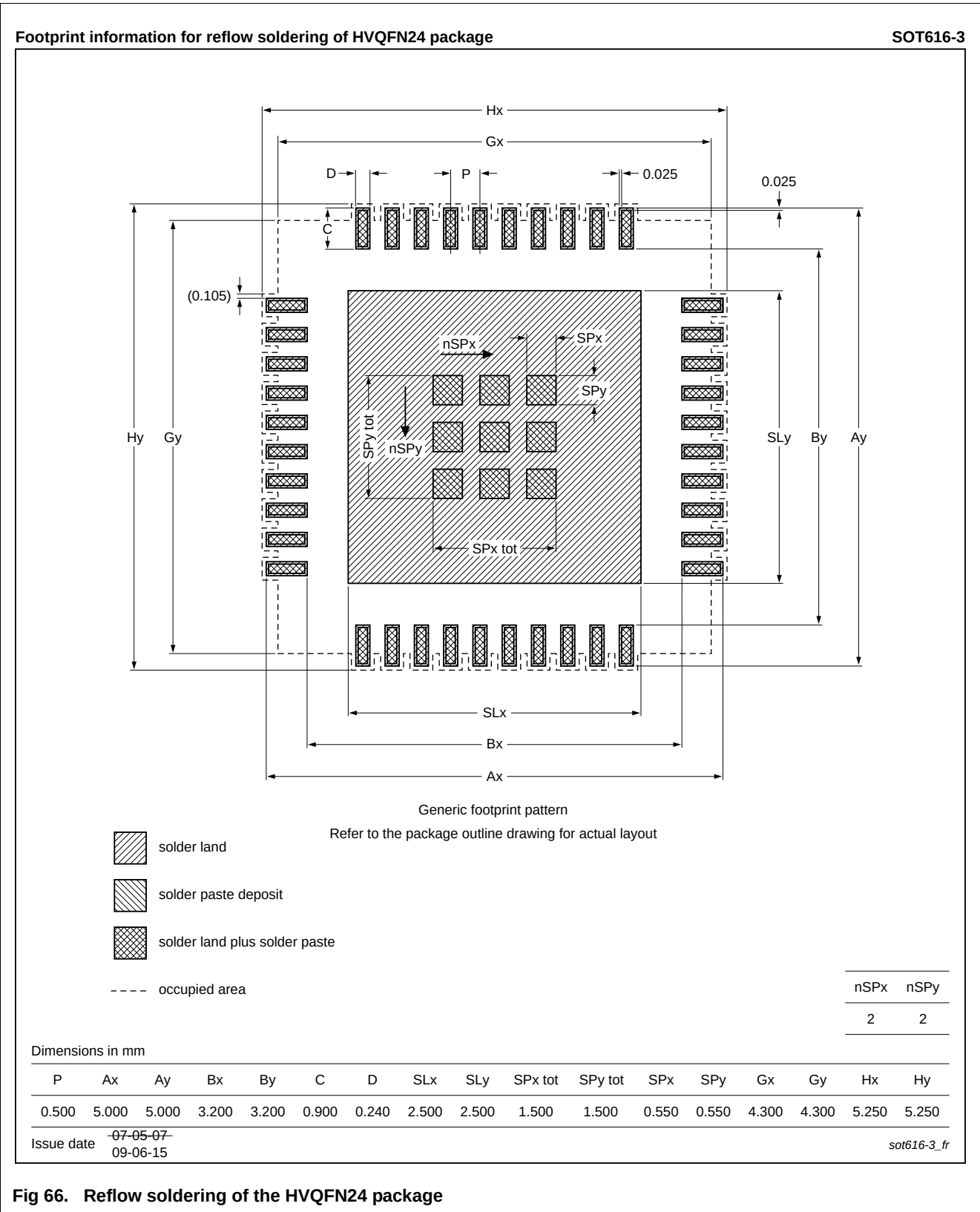


Fig 66. Reflow soldering of the HVQFN24 package

17. Revision history

Table 34. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC111X v.9.2	20140326	Product data sheet	-	LPC111X v.9.1
Modifications:	- Pin description tables for RESET/PIO0_0 updated: In deep power-down mode, this pin must be pulled HIGH externally. The RESET pin can be left unconnected or be used as a GPIO pin if an external RESET function is not needed. See Section 6.2. - Pin description notes relating to open-drain I2C-bus pins updated for clarity in Section 6.2. - Pin description of the WAKEUP pin updated for clarity. See Section 6.2. - Parts added: LPC1114JHI33/303, LPC1111JHN33/103, LPC1112JHN33/203, LPC1113JHN33/203, LPC1114JHN33/303, LPC1114JBD48/333, LPC1112FHI33/102, LPC1114JBD48/303, LPC1114JBD48/323, LPC1113JBD48/303, LPC1113JHN33/303, LPC1112JHN33/103, LPC1111JHN33/203, LPC1114JHN33/203.			
LPC111X v.9.1	20131213	Product data sheet	-	LPC111X v.9
Modifications:	- Table 17 "Static characteristics (LPC1100XL series)": - Added I_{DD} max spec for Deep-sleep and Deep power-down modes @ 25 °C and 105 °C. - Added Table note 11 "105 °C spec applies only to the LPC1112JHI33, LPC1114JHN33, LPC1115JBD48, and LPC1115JET48 parts." - Updated Table note 12 "WAKEUP pin and RESET pin are pulled HIGH externally." - Table 16 "Static characteristics (LPC1100, LPC1100L series)": - Updated Table note 9 "WAKEUP pin and RESET pin are pulled HIGH externally."			
LPC111X v.9	20131029	Product data sheet	-	LPC111X v.8.2
Modifications:	- Added LPC1112JHI33/203, LPC1114JHN33/333, LPC1115JBD48/303, and LPC1115JET48/303 parts. - Removed t_{clk(H)} and t_{clk(L)} from Figure 47 "SPI master timing in SPI mode" and Figure 48 "SPI slave timing in SPI mode"; spec not characterized. - Table 22 "Power-up characteristics[1]": Added table note "Does not apply to LPC1100XL series".			
LPC111X v.8.2	20130805	Product data sheet	-	LPC111X v.8.1
Modifications:	Added LPC1115FET48/303.			
LPC111X v.8.1	20130524	Product data sheet	-	LPC111X v.8
Modifications:	- Table 4 thru Table 11: Added "5 V tolerant pad" to RESET/PIO0_0 table note. - Added Section 9 "Thermal characteristics". - SRAM size corrected for part LPC1112FHN24/202 (4 kB). See Table 2.			
LPC111X v.8	20130220	Product data sheet	-	LPC111X v.7.5
Modifications:	- Table 16 "Static characteristics" added Pin capacitance section. - Default pin state corrected for pins PIO0_4 and PIO0_5 (I; IA) in Table 11 "LPC1100XL series: LPC1111/12/13/14 pin description table (HVQFN33 package)". - Table 12 "Limiting values" expanded for clarity. - Table 19 "Power consumption at very low frequencies using the watchdog oscillator" added. - Added Section 12.2 "Use of ADC input trigger signals". - Added Section 12.8 "ADC effective input impedance".			
LPC111X v.7.5	20121002	Product data sheet	-	LPC111X v.7.4