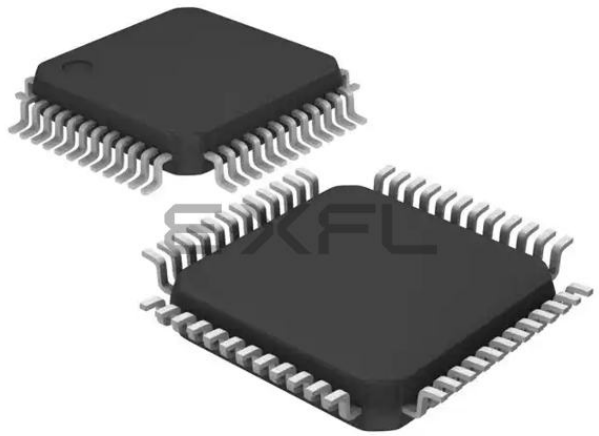

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Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	42
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1114fbd48-323j

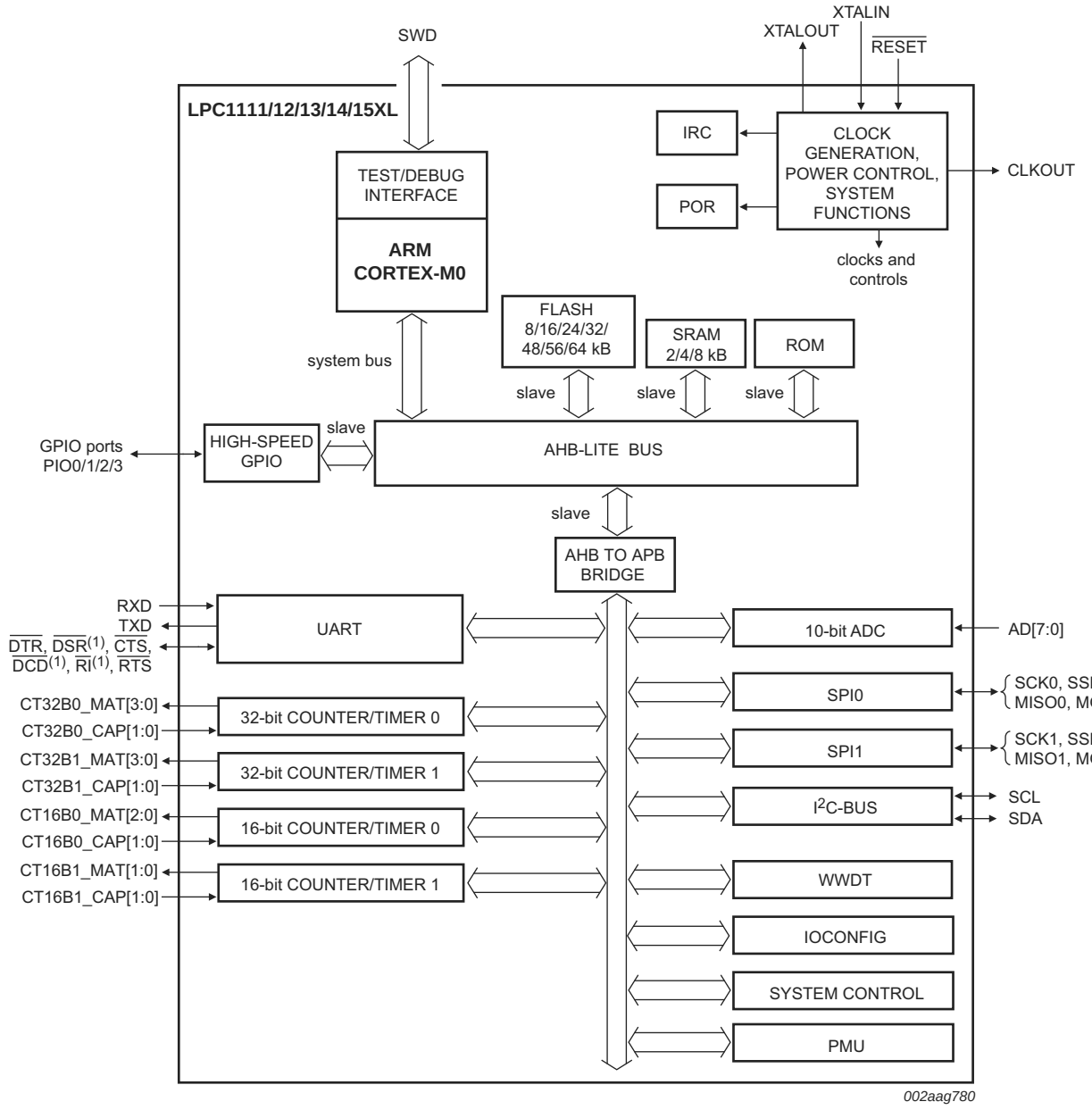
Table 1. Ordering information *…continued*

Type number	Package		
	Name	Description	Version
LPC1115JBD48/303	LQFP48	LQFP48: plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1115FET48/303	TFBGA48	plastic thin fine-pitch ball grid array package; 48 balls; body 4.5 × 4.5 × 0.7 mm	SOT1155-2
LPC1115JET48/303	TFBGA48	plastic thin fine-pitch ball grid array package; 48 balls; body 4.5 × 4.5 × 0.7 mm	SOT1155-2

4.1 Ordering options

Table 2. Ordering options

Type number	Series	Flash	Total SRAM	Power profiles	UART	I^2C/ Fast+	SPI	ADC channel	GPIO	Package	Temp[1]
LPC1110											
LPC1110FD20	LPC1100L	4 kB	1 kB	yes	1	1	1	5	16	SO20	F
LPC1111											
LPC1111FDH20/002	LPC1100L	8 kB	2 kB	yes	1	1	1	5	16	TSSOP20	F
LPC1111FHN33/101	LPC1100	8 kB	2 kB	no	1	1	1	8	28	HVQFN33	F
LPC1111FHN33/102	LPC1100L	8 kB	2 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1111FHN33/103	LPC1100XL	8 kB	2 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1111JHN33/103	LPC1100XL	8 kB	2 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1111FHN33/201	LPC1100	8 kB	4 kB	no	1	1	1	8	28	HVQFN33	F
LPC1111FHN33/202	LPC1100L	8 kB	4 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1111FHN33/203	LPC1100XL	8 kB	4 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1111JHN33/203	LPC1100XL	8 kB	4 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1112											
LPC1112FD20/102	LPC1100L	16 kB	4 kB	yes	1	1	1	5	16	SO20	F
LPC1112FDH20/102	LPC1100L	16 kB	4 kB	yes	1	-	1	5	14	TSSOP20	F
LPC1112FDH28/102	LPC1100L	16 kB	4 kB	yes	1	1	1	6	22	TSSOP28	F
LPC1112FHN24/202	LPC1100L	16 kB	4 kB	yes	1	1	1	6	19	HVQFN24	F
LPC1112FHN33/101	LPC1100	16 kB	2 kB	no	1	1	1	8	28	HVQFN33	F
LPC1112FHN33/102	LPC1100L	16 kB	2 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1112FHN33/103	LPC1100XL	16 kB	2 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1112JHN33/103	LPC1100XL	16 kB	2 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1112FHN33/201	LPC1100	16 kB	4 kB	no	1	1	1	8	28	HVQFN33	F
LPC1112FHN33/202	LPC1100L	16 kB	4 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1112FHN33/203	LPC1100XL	16 kB	4 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1112JHN33/203	LPC1100XL	16 kB	4 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1112FHI33/102	LPC1100L	16 kB	2 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1112FHI33/202	LPC1100L	16 kB	4 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1112FHI33/203	LPC1100XL	16 kB	4 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1112JHI33/203	LPC1100XL	16 kB	4 kB	yes	1	1	2	8	28	HVQFN33	J



(1) LQFP48 and TFBGA48 only.

Fig 2. LPC1100XL series block diagram

Table 3. Pin description overview

Part	Pin description table	Pinning diagram
LPC1114FHN33/203	Table 11	Figure 7
LPC1114JHN33/203	Table 11	Figure 7
LPC1114FHN33/301	Table 9	Figure 6
LPC1114FHN33/302	Table 9	Figure 6
LPC1114JHN33/303	Table 11	Figure 7
LPC1114FHN33/303	Table 11	Figure 7
LPC1114FHN33/333	Table 11	Figure 7
LPC1114JHN33/333	Table 11	Figure 7
LPC1114FHI33/302	Table 9	Figure 6
LPC1114FHI33/303	Table 11	Figure 7
LPC1114JHI33/303	Table 11	Figure 7
LPC1113FBD48/301	Table 8	Figure 3
LPC1113FBD48/302	Table 8	Figure 3
LPC1113FBD48/303	Table 10	Figure 4
LPC1113JBD48/303	Table 10	Figure 4
LPC1114FBD48/301	Table 8	Figure 3
LPC1114FBD48/302	Table 8	Figure 3
LPC1114FBD48/303	Table 10	Figure 4
LPC1114JBD48/303	Table 10	Figure 4
LPC1114FBD48/323	Table 10	Figure 4
LPC1114JBD48/323	Table 10	Figure 4
LPC1114FBD48/333	Table 10	Figure 4
LPC1114JBD48/333	Table 10	Figure 4
LPC1115FBD48/303	Table 10	Figure 4
LPC1115JBD48/303	Table 10	Figure 4
LPC1115FET48/303	Table 10	Figure 5
LPC1115JET48/303	Table 10	Figure 5

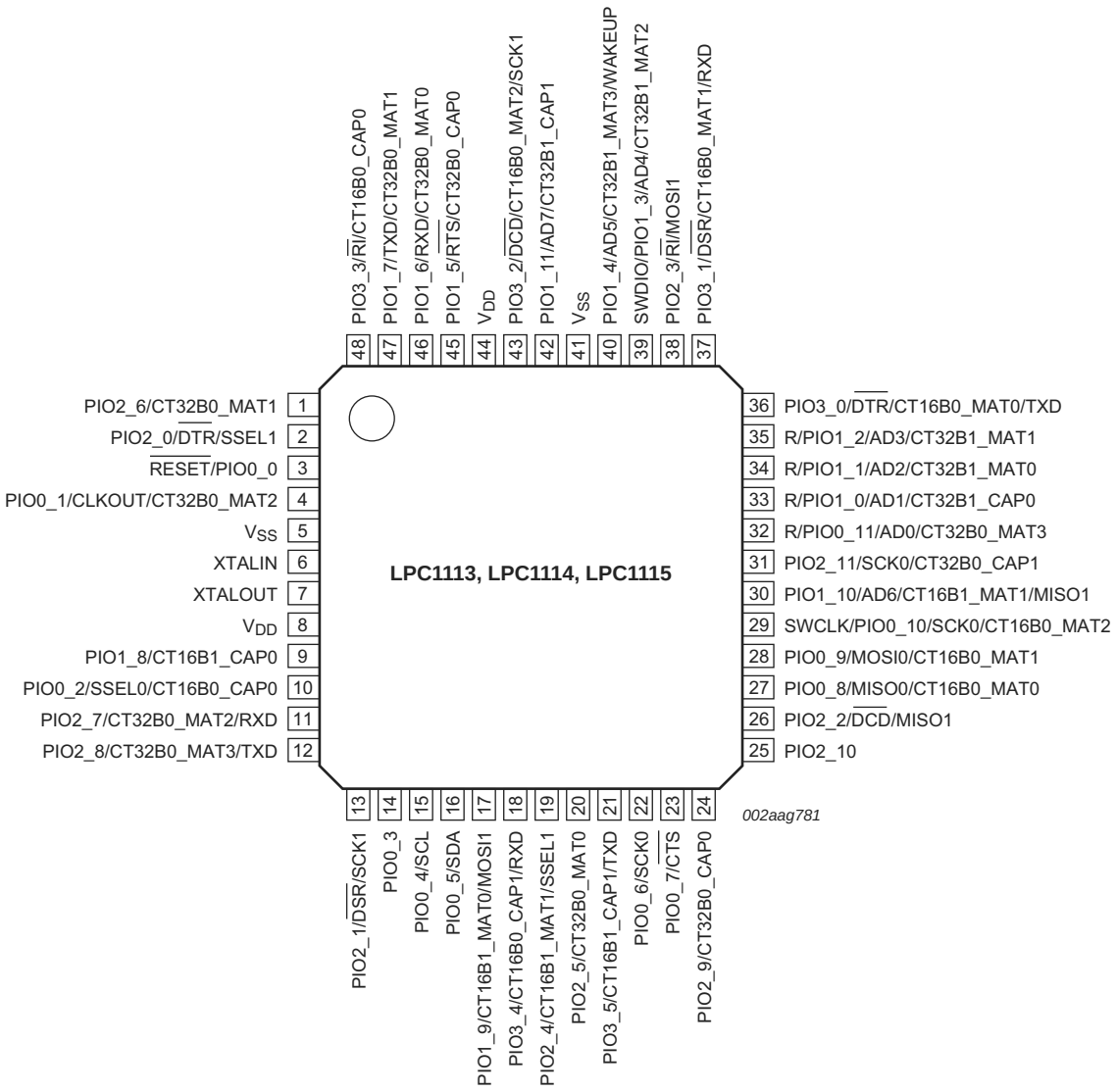


Fig 4. LPC1100XL series pin configuration LQFP48 package

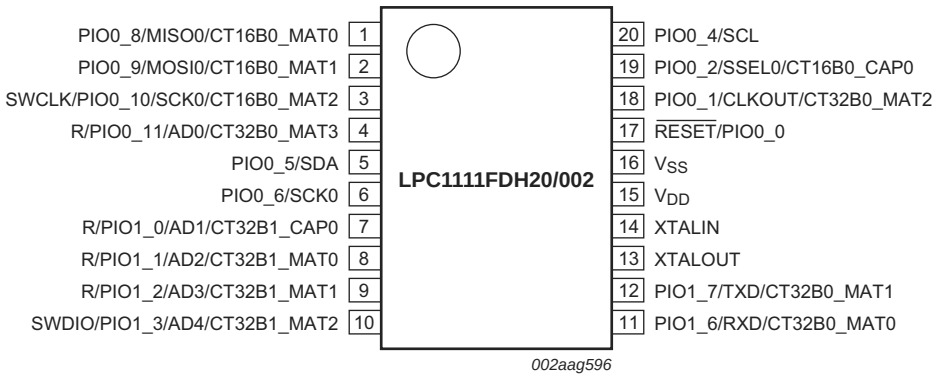


Fig 9. LPC1100L series pin configuration TSSOP20 package with I²C-bus pins

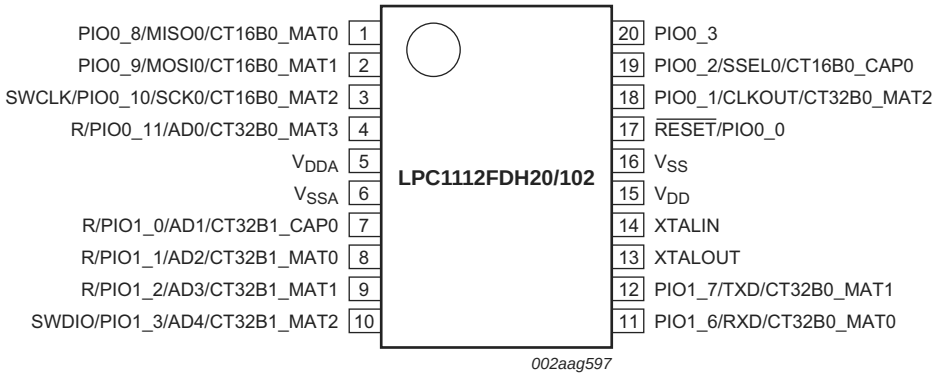


Fig 10. LPC1100L series pin configuration TSSOP20 package with V_{DDA} and V_{SSA} pins

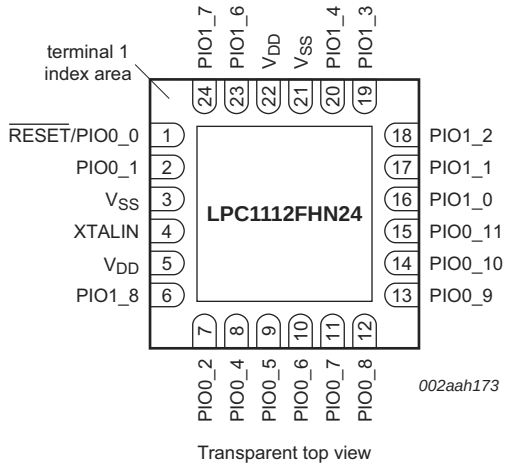


Fig 11. LPC1100L series pin configuration HVQFN24 package

Table 4. LPC1100L series: LPC1110/11/12 pin description table (SO20 and TSSOP20 package with I²C-bus pins) *…continued*

Symbol	Pin SO20/ TSSOP20	Start logic input	Type	Reset state [1]	Description
R/PIO0_11/ AD0/CT32B0_MAT3	4 [5]	yes	I	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO0_11 —** General purpose digital input/output pin.
			I	-	**AD0 —** A/D converter, input 0.
			O	-	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
PIO1_0 to PIO1_7			I/O		**Port 1 —** Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block.
R/PIO1_0/ AD1/CT32B1_CAP0	7 [5]	yes	I	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO1_0 —** General purpose digital input/output pin.
			I	-	**AD1 —** A/D converter, input 1.
			I	-	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
R/PIO1_1/ AD2/CT32B1_MAT0	8 [5]	no	O	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO1_1 —** General purpose digital input/output pin.
			I	-	**AD2 —** A/D converter, input 2.
			O	-	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
R/PIO1_2/ AD3/CT32B1_MAT1	9 [5]	no	I	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO1_2 —** General purpose digital input/output pin.
			I	-	**AD3 —** A/D converter, input 3.
			O	-	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ AD4/CT32B1_MAT2	10 [5]	no	I/O	I; PU	**SWDIO —** Serial wire debug input/output.
			I/O	-	**PIO1_3 —** General purpose digital input/output pin.
			I	-	**AD4 —** A/D converter, input 4.
			O	-	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
PIO1_6/RXD/ CT32B0_MAT0	11 [3]	no	I/O	I; PU	**PIO1_6 —** General purpose digital input/output pin.
			I	-	**RXD —** Receiver input for UART.
			O	-	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO1_7/TXD/ CT32B0_MAT1	12 [3]	no	I/O	I; PU	**PIO1_7 —** General purpose digital input/output pin.
			O	-	**TXD —** Transmitter output for UART.
			O	-	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
V_{DD}	15	-		-	3.3 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	14 [6]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	13 [6]	-	O	-	Output from the oscillator amplifier.
V_{SS}	16	-		-	Ground.

Table 8. LPC1100 and LPC1100L series: LPC1113/14 pin description table (LQFP48 package)

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO0_0 to PIO0_11			I/O		**Port 0 —** Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.
$\overline{\text{RESET}}$/PIO0_0	3[2]	yes	I	I; PU	**$\overline{\text{RESET}}$ —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO pin if an external $\overline{\text{RESET}}$ function is not needed and Deep power-down mode is not used.
			I/O	-	**PIO0_0 —** General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/ CT32B0_MAT2	4[3]	yes	I/O	I; PU	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
			O	-	**CLKOUT —** Clockout pin.
			O	-	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	10[3]	yes	I/O	I; PU	**PIO0_2 —** General purpose digital input/output pin.
			I/O	-	**SSEL0 —** Slave Select for SPI0.
			I	-	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO0_3	14[3]	yes	I/O	I; PU	**PIO0_3 —** General purpose digital input/output pin.
PIO0_4/SCL	15[4]	yes	I/O	I; IA	**PIO0_4 —** General purpose digital input/output pin (open-drain).
			I/O	-	**SCL —** I^2C-bus, open-drain clock input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	16[4]	yes	I/O	I; IA	**PIO0_5 —** General purpose digital input/output pin (open-drain).
			I/O	-	**SDA —** I^2C-bus, open-drain data input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	22[3]	yes	I/O	I; PU	**PIO0_6 —** General purpose digital input/output pin.
			I/O	-	**SCK0 —** Serial clock for SPI0.
PIO0_7/$\overline{\text{CTS}}$	23[3]	yes	I/O	I; PU	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
			I	-	**$\overline{\text{CTS}}$ —** Clear To Send input for UART.
PIO0_8/MISO0/ CT16B0_MAT0	27[3]	yes	I/O	I; PU	**PIO0_8 —** General purpose digital input/output pin.
			I/O	-	**MISO0 —** Master In Slave Out for SPI0.
			O	-	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	28[3]	yes	I/O	I; PU	**PIO0_9 —** General purpose digital input/output pin.
			I/O	-	**MOSI0 —** Master Out Slave In for SPI0.
			O	-	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.

Table 9. LPC1100 and LPC1100L series: LPC1111/12/13/14 pin description table (HVQFN33 package) *…continued*

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
R/PIO0_11/AD0/ CT32B0_MAT3	21[5]	yes	-	I;PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO0_11 —** General purpose digital input/output pin.
			I	-	**AD0 —** A/D converter, input 0.
			O	-	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
PIO1_0 to PIO1_11					**Port 1 —** Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block.
R/PIO1_0/AD1/ CT32B1_CAP0	22[5]	yes	-	I;PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO1_0 —** General purpose digital input/output pin.
			I	-	**AD1 —** A/D converter, input 1.
			I	-	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
R/PIO1_1/AD2/ CT32B1_MAT0	23[5]	no	-	I;PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO1_1 —** General purpose digital input/output pin.
			I	-	**AD2 —** A/D converter, input 2.
			O	-	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
R/PIO1_2/AD3/ CT32B1_MAT1	24[5]	no	-	I;PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO1_2 —** General purpose digital input/output pin.
			I	-	**AD3 —** A/D converter, input 3.
			O	-	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ AD4/CT32B1_MAT2	25[5]	no	I/O	I;PU	**SWDIO —** Serial wire debug input/output.
			I/O	-	**PIO1_3 —** General purpose digital input/output pin.
			I	-	**AD4 —** A/D converter, input 4.
			O	-	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
PIO1_4/AD5/ CT32B1_MAT3/ WAKEUP	26[5]	no	I/O	I;PU	**PIO1_4 —** General purpose digital input/output pin with 10 ns glitch filter. In Deep power-down mode, this pin serves as the Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
			I	-	**AD5 —** A/D converter, input 5.
			O	-	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
PIO1_5/$\overline{\text{RTS}}$/ CT32B0_CAP0	30[3]	no	I/O	I;PU	**PIO1_5 —** General purpose digital input/output pin.
			O	-	**$\overline{\text{RTS}}$ —** Request To Send output for UART.
			I	-	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
PIO1_6/RXD/ CT32B0_MAT0	31[3]	no	I/O	I;PU	**PIO1_6 —** General purpose digital input/output pin.
			I	-	**RXD —** Receiver input for UART.
			O	-	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.

Table 10. LPC1100XL series: LPC1113/14/15 pin description table (LQFP48 and TFBGA48 package) *…continued*

Symbol	LQFP48	TFBGA48	Start logic input	Type	Reset state [1]	Description
PIO0_8/MISO0/ CT16B0_MAT0	27[3]	F8[3]	yes	I/O	I; PU	**PIO0_8 —** General purpose digital input/output pin.
				I/O	-	**MISO0 —** Master In Slave Out for SPI0.
				O	-	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	28[3]	F7[3]	yes	I/O	I; PU	**PIO0_9 —** General purpose digital input/output pin.
				I/O	-	**MOSI0 —** Master Out Slave In for SPI0.
				O	-	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2	29[3]	E7[3]	yes	I	I; PU	**SWCLK —** Serial wire clock.
				I/O	-	**PIO0_10 —** General purpose digital input/output pin.
				I/O	-	**SCK0 —** Serial clock for SPI0.
				O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
R/PIO0_11/ AD0/CT32B0_MAT3	32[5]	D8[5]	yes	I	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
				I/O	-	**PIO0_11 —** General purpose digital input/output pin.
				I	-	**AD0 —** A/D converter, input 0.
				O	-	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
PIO1_0 to PIO1_11				I/O		**Port 1 —** Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block.
R/PIO1_0/ AD1/CT32B1_CAP0	33[5]	C7[5]	yes	I	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
				I/O	-	**PIO1_0 —** General purpose digital input/output pin.
				I	-	**AD1 —** A/D converter, input 1.
				I	-	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
R/PIO1_1/ AD2/CT32B1_MAT0	34[5]	C8[5]	no	O	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
				I/O	-	**PIO1_1 —** General purpose digital input/output pin.
				I	-	**AD2 —** A/D converter, input 2.
				O	-	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
R/PIO1_2/ AD3/CT32B1_MAT1	35[5]	B7[5]	no	I	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
				I/O	-	**PIO1_2 —** General purpose digital input/output pin.
				I	-	**AD3 —** A/D converter, input 3.
				O	-	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ AD4/CT32B1_MAT2	39[5]	B6[5]	no	I/O	I; PU	**SWDIO —** Serial wire debug input/output.
				I/O	-	**PIO1_3 —** General purpose digital input/output pin.
				I	-	**AD4 —** A/D converter, input 4.
				O	-	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.

Table 10. LPC1100XL series: LPC1113/14/15 pin description table (LQFP48 and TFBGA48 package) *…continued*

Symbol	LQFP48	TFBGA48	Start logic input	Type	Reset state [1]	Description
PIO1_4/AD5/ CT32B1_MAT3/ WAKEUP	40[5]	A6[5]	no	I/O	I; PU	**PIO1_4 —** General purpose digital input/output pin with 10 ns glitch filter. In Deep power-down mode, this pin serves as the Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
				I	-	**AD5 —** A/D converter, input 5.
				O	-	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
PIO1_5/$\overline{\text{RTS}}$/ CT32B0_CAP0	45[3]	A3[3]	no	I/O	I; PU	**PIO1_5 —** General purpose digital input/output pin.
				O	-	**$\overline{\text{RTS}}$ —** Request To Send output for UART.
				I	-	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
PIO1_6/RXD/ CT32B0_MAT0	46[3]	B3[3]	no	I/O	I; PU	**PIO1_6 —** General purpose digital input/output pin.
				I	-	**RXD —** Receiver input for UART.
				O	-	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO1_7/TXD/ CT32B0_MAT1	47[3]	B2[3]	no	I/O	I; PU	**PIO1_7 —** General purpose digital input/output pin.
				O	-	**TXD —** Transmitter output for UART.
				O	-	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO1_8/ CT16B1_CAP0	9[3]	F2[3]	no	I/O	I; PU	**PIO1_8 —** General purpose digital input/output pin.
				I	-	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
PIO1_9/ CT16B1_MAT0/ MOSI1	17[3]	G4[3]	no	I/O	I; PU	**PIO1_9 —** General purpose digital input/output pin.
				O	-	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
				I/O	-	**MOSI1 —** Master Out Slave In for SPI1.
PIO1_10/AD6/ CT16B1_MAT1/ MISO1	30[5]	E8[5]	no	I/O	I; PU	**PIO1_10 —** General purpose digital input/output pin.
				I	-	**AD6 —** A/D converter, input 6.
				O	-	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
				I/O	-	**MISO1 —** Master In Slave Out for SPI1.
PIO1_11/AD7/ CT32B1_CAP1	42[5]	A5[5]	no	I/O	I; PU	**PIO1_11 —** General purpose digital input/output pin.
				I	-	**AD7 —** A/D converter, input 7.
				I	-	**CT32B1_CAP1 —** Capture input 1 for 32-bit timer 1.
PIO2_0 to PIO2_11				I/O		**Port 2 —** Port 2 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 2 pins depends on the function selected through the IOCONFIG register block.
PIO2_0/$\overline{\text{DTR}}$/SSEL1	2[3]	B1[3]	no	I/O	I; PU	**PIO2_0 —** General purpose digital input/output pin.
				O	-	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for UART.
				I/O	-	**SSEL1 —** Slave Select for SPI1.
PIO2_1/$\overline{\text{DSR}}$/SCK1	13[3]	H1[3]	no	I/O	I; PU	**PIO2_1 —** General purpose digital input/output pin.
				I	-	**$\overline{\text{DSR}}$ —** Data Set Ready input for UART.
				I/O	-	**SCK1 —** Serial clock for SPI1.

Table 10. LPC1100XL series: LPC1113/14/15 pin description table (LQFP48 and TFBGA48 package) *…continued*

Symbol	LQFP48	TFBGA48	Start logic input	Type	Reset state [1]	Description
PIO2_2/$\overline{\text{DCD}}$/MISO1	26[3]	G8[3]	no	I/O	I; PU	**PIO2_2 —** General purpose digital input/output pin.
				I	-	**$\overline{\text{DCD}}$ —** Data Carrier Detect input for UART.
				I/O	-	**MISO1 —** Master In Slave Out for SPI1.
PIO2_3/$\overline{\text{RI}}$/MOSI1	38[3]	A7[3]	no	I/O	I; PU	**PIO2_3 —** General purpose digital input/output pin.
				I	-	**$\overline{\text{RI}}$ —** Ring Indicator input for UART.
				I/O	-	**MOSI1 —** Master Out Slave In for SPI1.
PIO2_4/ CT16B1_MAT1/ SSEL1	19[3]	G5[3]	no	I/O	I; PU	**PIO2_4 —** General purpose digital input/output pin.
				O	-	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
				O	-	**SSEL1 —** Slave Select for SPI1.
PIO2_5/ CT32B0_MAT0	20[3]	H5[3]	no	I/O	I; PU	**PIO2_5 —** General purpose digital input/output pin.
				O	-	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO2_6/ CT32B0_MAT1	1[3]	A1[3]	no	I/O	I; PU	**PIO2_6 —** General purpose digital input/output pin.
				O	-	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO2_7/ CT32B0_MAT2/RXD	11[3]	G2[3]	no	I/O	I; PU	**PIO2_7 —** General purpose digital input/output pin.
				O	-	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
				I	-	**RXD —** Receiver input for UART.
PIO2_8/ CT32B0_MAT3/TXD	12[3]	G1[3]	no	I/O	I; PU	**PIO2_8 —** General purpose digital input/output pin.
				O	-	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
				O	-	**TXD —** Transmitter output for UART.
PIO2_9/ CT32B0_CAP0	24[3]	H7[3]	no	I/O	I; PU	**PIO2_9 —** General purpose digital input/output pin.
				I	-	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
PIO2_10	25[3]	H8[3]	no	I/O	I; PU	**PIO2_10 —** General purpose digital input/output pin.
PIO2_11/SCK0/ CT32B0_CAP1	31[3]	D7[3]	no	I/O	I; PU	**PIO2_11 —** General purpose digital input/output pin.
				I/O	-	**SCK0 —** Serial clock for SPI0.
				I	-	**CT32B0_CAP1 —** Capture input for 32-bit timer 0.
PIO3_0 to PIO3_5				I/O		**Port 3 —** Port 3 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 3 pins depends on the function selected through the IOCONFIG register block. Pins PIO3_6 to PIO3_11 are not available.
PIO3_0/$\overline{\text{DTR}}$/ CT16B0_MAT0/TXD	36[3]	B8[3]	no	I/O	I; PU	**PIO3_0 —** General purpose digital input/output pin.
				O	-	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for UART.
				O	-	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
				O	-	**TXD —** Transmitter Output for UART.
PIO3_1/$\overline{\text{DSR}}$/ CT16B0_MAT1/RXD	37[3]	A8[3]	no	I/O	I; PU	**PIO3_1 —** General purpose digital input/output pin.
				I	-	**$\overline{\text{DSR}}$ —** Data Set Ready input for UART.
				O	-	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
				I	-	**RXD —** Receiver input for UART.

Table 10. LPC1100XL series: LPC1113/14/15 pin description table (LQFP48 and TFBGA48 package) *…continued*

Symbol	LQFP48	TFBGA48	Start logic input	Type	Reset state [1]	Description
PIO3_2/$\overline{\text{DCD}}$/ CT16B0_MAT2/ SCK1	43[3]	A4[3]	no	I/O	I; PU	**PIO3_2 —** General purpose digital input/output pin.
				I	-	**$\overline{\text{DCD}}$ —** Data Carrier Detect input for UART.
				O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
				I/O	-	**SCK1 —** Serial clock for SPI1.
PIO3_3/$\overline{\text{RI}}$/ CT16B0_CAP0	48[3]	A2[3]	no	I/O	I; PU	**PIO3_3 —** General purpose digital input/output pin.
				I	-	**$\overline{\text{RI}}$ —** Ring Indicator input for UART.
				I	-	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO3_4/ CT16B0_CAP1/RXD	18[3]	H4[3]	no	I/O	I; PU	**PIO3_4 —** General purpose digital input/output pin.
				I	-	**CT16B0_CAP1 —** Capture input 1 for 16-bit timer 0.
				I	-	**RXD —** Receiver input for UART
PIO3_5/ CT16B1_CAP1/TXD	21[3]	G6[3]	no	I/O	I; PU	**PIO3_5 —** General purpose digital input/output pin.
				I	-	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
				O	-	**TXD —** Transmitter output for UART
V_{DD}	8; 44	E2; B4	-	I	-	3.3 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	6[6]	D1[6]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	7[6]	E1[6]	-	O	-	Output from the oscillator amplifier.
V_{SS}	5; 41	D2; B5	-	I	-	Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level (V_{DD} = 3.3 V)); IA = inactive, no pull-up/down enabled.

[2] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See Figure 52 for the reset pad configuration.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 51).

[4] I^2C-bus pads compliant with the I^2C-bus specification for I^2C standard mode and I^2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 51).

[6] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

7.16.5.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

7.16.5.3 Deep-sleep mode

In Deep-sleep mode, the chip is in Sleep mode, and in addition all analog blocks are shut down. As an exception, the user has the option to keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection. Deep-sleep mode allows for additional power savings.

Up to 13 pins total serve as external wake-up pins to the start logic to wake up the chip from Deep-sleep mode.

Unless the watchdog oscillator is selected to run in Deep-sleep mode, the clock source should be switched to IRC before entering Deep-sleep mode, because the IRC can be switched on and off glitch-free.

7.16.5.4 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip with the exception of the WAKEUP pin. The LPC1110/11/12/13/14/15 can wake up from Deep power-down mode via the WAKEUP pin.

A LOW-going pulse as short as 50 ns wakes up the part from Deep power-down mode.

When entering Deep power-down mode, an external pull-up resistor is required on the WAKEUP pin to hold it HIGH. The $\overline{\text{RESET}}$ pin must also be held HIGH to prevent it from floating while in Deep power-down mode.

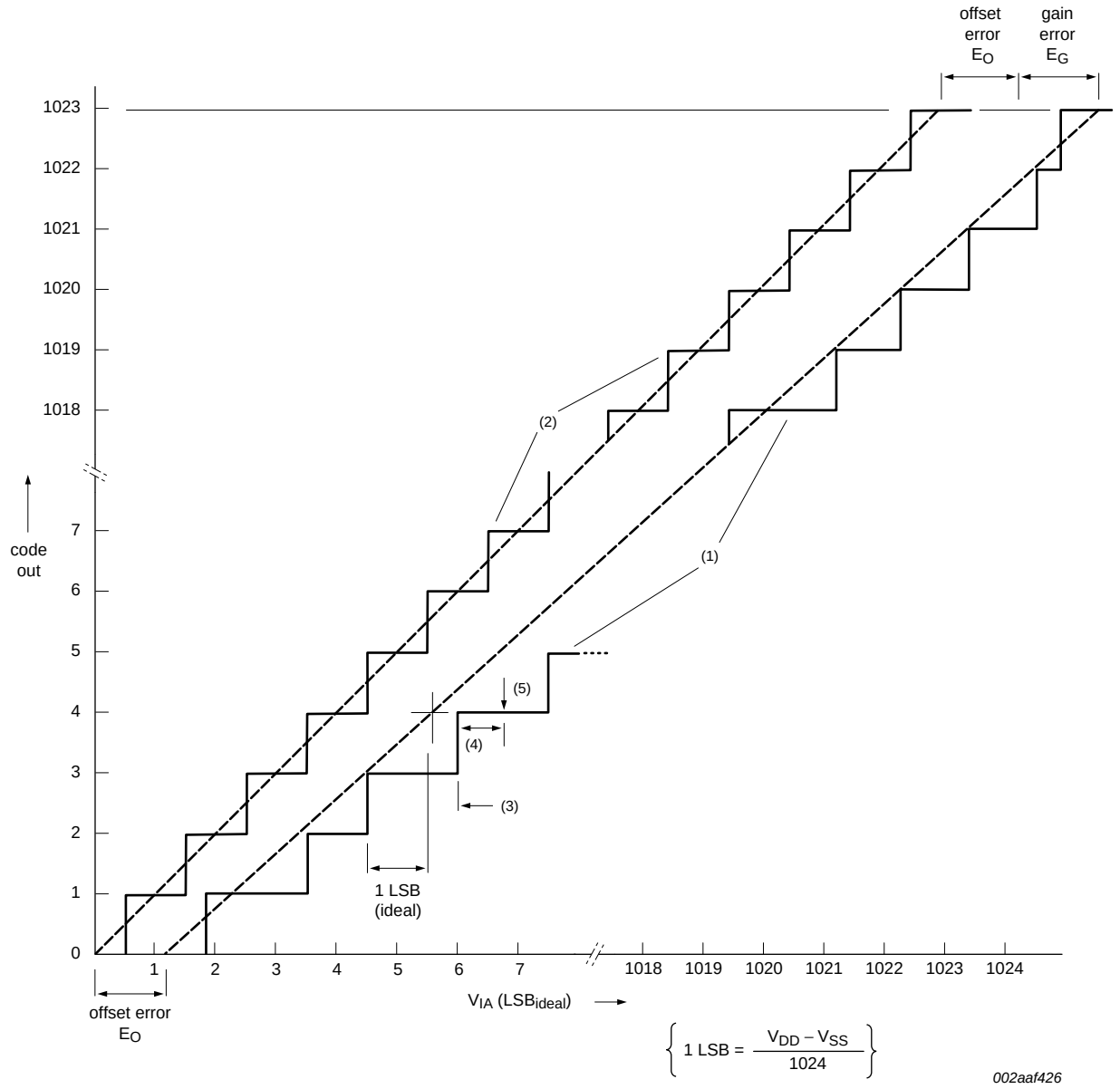
7.17 System control

7.17.1 Start logic

The start logic connects external pins to corresponding interrupts in the NVIC. Each pin shown in Table 8 to Table 9 as input to the start logic has an individual interrupt in the NVIC interrupt vector table. The start logic pins can serve as external interrupt pins when the chip is running. In addition, an input signal on the start logic pins can wake up the chip from Deep-sleep mode when all clocks are shut down.

Table 17. Static characteristics (LPC1100XL series) *…continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{OH}	HIGH-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OH} = −20 mA	V_{DD} − 0.4	-	-	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OH} = −12 mA	V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OL} = 4 mA	-	-	0.4	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OL} = 3 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V; 2.5 V ≤ V_{DD} ≤ 3.6 V	20	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V	12	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 2.5 V ≤ V_{DD} ≤ 3.6 V	4	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V	3	-	-	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD} [16]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V 2.0 V ≤ V_{DD} ≤ 3.6 V	−15	−50	−85	μA
		1.8 V ≤ V_{DD} < 2.0 V	−10	−50	−85	μA
		V_{DD} < V_I < 5 V	0	0	0	μA
I^2C-bus pins (PIO0_4 and PIO0_5)						
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage		-	0.05V_{DD}	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins 2.5 V ≤ V_{DD} ≤ 3.6 V	3.5	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V	3	-	-	
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as Fast-mode Plus pins 2.5 V ≤ V_{DD} ≤ 3.6 V	20	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V	16	-	-	
I_{LI}	input leakage current	V_I = V_{DD} [17]	-	2	4	μA
		V_I = 5 V	-	10	22	μA



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 17. ADC characteristics

10.9 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at T_{amb} = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 48 MHz.

Table 21. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	48 MHz	
IRC	0.27	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	0.22	-	-	IRC running; PLL off; independent of main clock frequency.
Watchdog oscillator at 500 kHz/2	0.004	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	0.051	-	-	Independent of main clock frequency.
Main PLL	-	0.21	-	
ADC	-	0.08	0.29	
CLKOUT	-	0.12	0.47	Main clock divided by 4 in the CLKOUTDIV register.
CT16B0	-	0.02	0.06	
CT16B1	-	0.02	0.06	
CT32B0	-	0.02	0.07	
CT32B1	-	0.02	0.06	
GPIO	-	0.23	0.88	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
IOCONFIG	-	0.03	0.10	
I2C	-	0.04	0.13	
ROM	-	0.04	0.15	
SPI0	-	0.12	0.45	
SPI1	-	0.12	0.45	
UART	-	0.22	0.82	
WDT/WWDT	-	0.02	0.06	Main clock selected as clock source for the WDT.

12.4 XTAL Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{X1}, C_{X2}, and C_{X3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{X1} and C_{X2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

12.5 Standard I/O pad configuration

Figure 51 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital output: Pseudo open-drain mode enable/disabled
- Analog input

14. Soldering

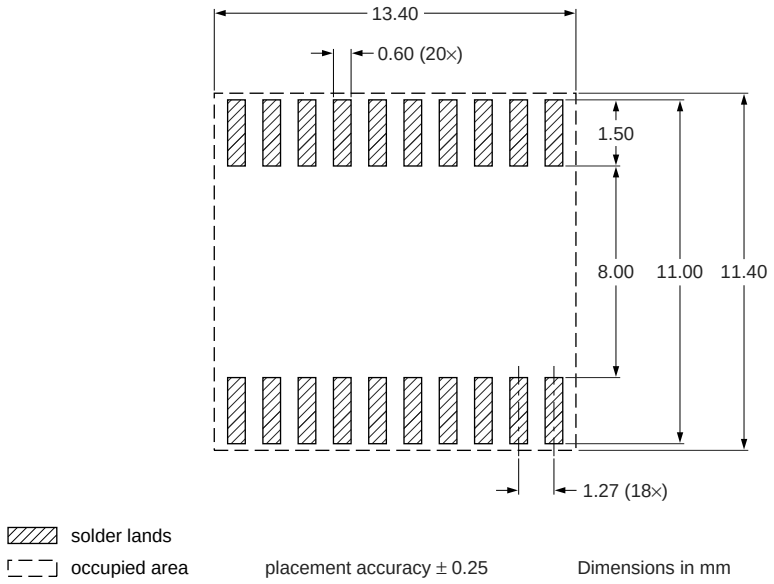


Fig 63. Reflow soldering of the SO20 package

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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