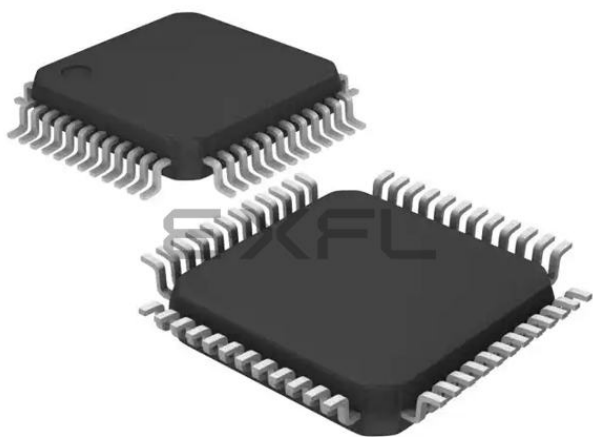




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	42
Program Memory Size	56KB (56K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1114fbd48-333-1

Table 2. Ordering options ...continued

Type number	Series	Flash	Total SRAM	Power profiles	UART	I ² C/ Fast+	SPI	ADC channel	GPIO	Package	Temp ^[1]
LPC1113											
LPC1113FHN33/201	LPC1100	24 kB	4 kB	no	1	1	1	8	28	HVQFN33	F
LPC1113FHN33/202	LPC1100L	24 kB	4 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1113FHN33/203	LPC1100XL	24 kB	4 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1113JHN33/203	LPC1100XL	24 kB	4 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1113FHN33/301	LPC1100	24 kB	8 kB	no	1	1	1	8	28	HVQFN33	F
LPC1113FHN33/302	LPC1100L	24 kB	8 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1113FHN33/303	LPC1100XL	24 kB	8 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1113JHN33/303	LPC1100XL	24 kB	8 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1113FBD48/301	LPC1100	24 kB	8 kB	no	1	1	2	8	42	LQFP48	F
LPC1113FBD48/302	LPC1100L	24 kB	8 kB	yes	1	1	2	8	42	LQFP48	F
LPC1113FBD48/303	LPC1100XL	24 kB	8 kB	yes	1	1	2	8	42	LQFP48	F
LPC1113JBD48/303	LPC1100XL	24 kB	8 kB	yes	1	1	2	8	42	LQFP48	J
LPC1114											
LPC1114FDH28/102	LPC1100L	32 kB	4 kB	yes	1	1	1	6	22	TSSOP28	F
LPC1114FN28/102	LPC1100L	32 kB	4 kB	yes	1	1	1	6	22	DIP28	F
LPC1114FHN33/201	LPC1100	32 kB	4 kB	no	1	1	1	8	28	HVQFN33	F
LPC1114FHN33/202	LPC1100L	32 kB	4 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1114FHN33/203	LPC1100XL	32 kB	4 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1114JHN33/203	LPC1100XL	32 kB	4 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1114FHN33/301	LPC1100	32 kB	8 kB	no	1	1	1	8	28	HVQFN33	F
LPC1114FHN33/302	LPC1100L	32 kB	8 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1114FHN33/303	LPC1100XL	32 kB	8 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1114JHN33/303	LPC1100XL	32 kB	8 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1114FHN33/333	LPC1100XL	56 kB	8 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1114JHN33/333	LPC1100XL	56 kB	8 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1114FHI33/302	LPC1100L	32 kB	8 kB	yes	1	1	1	8	28	HVQFN33	F
LPC1114FHI33/303	LPC1100XL	32 kB	8 kB	yes	1	1	2	8	28	HVQFN33	F
LPC1114JHI33/303	LPC1100XL	32 kB	8 kB	yes	1	1	2	8	28	HVQFN33	J
LPC1114FBD48/301	LPC1100	32 kB	8 kB	no	1	1	2	8	42	LQFP48	F
LPC1114FBD48/302	LPC1100L	32 kB	8 kB	yes	1	1	2	8	42	LQFP48	F
LPC1114FBD48/303	LPC1100XL	32 kB	8 kB	yes	1	1	2	8	42	LQFP48	F
LPC1114JBD48/303	LPC1100XL	32 kB	8 kB	yes	1	1	2	8	42	LQFP48	J
LPC1114FBD48/323	LPC1100XL	48 kB	8 kB	yes	1	1	2	8	42	LQFP48	F
LPC1114JBD48/323	LPC1100XL	48 kB	8 kB	yes	1	1	2	8	42	LQFP48	J
LPC1114FBD48/333	LPC1100XL	56 kB	8 kB	yes	1	1	2	8	42	LQFP48	F
LPC1114JBD48/333	LPC1100XL	56 kB	8 kB	yes	1	1	2	8	42	LQFP48	J
LPC1115											
LPC1115FBD48/303	LPC1100XL	64 kB	8 kB	yes	1	1	2	8	42	LQFP48	F

Table 5. LPC1100L series: LPC1112 pin description table (TSSOP20 with V_{DDA} and V_{SSA} pins) ...continued

Symbol	Pin TSSOP20	Start logic input	Type	Reset state [4]	Description
SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2	3 [3]	yes	I	I; PU	SWCLK — Serial wire clock.
			I/O	-	PIO0_10 — General purpose digital input/output pin.
			I/O	-	SCK0 — Serial clock for SPI0.
			O	-	CT16B0_MAT2 — Match output 2 for 16-bit timer 0.
R/PIO0_11/ AD0/CT32B0_MAT3	4 [4]	yes	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO0_11 — General purpose digital input/output pin.
			I	-	AD0 — A/D converter, input 0.
			O	-	CT32B0_MAT3 — Match output 3 for 32-bit timer 0.
PIO1_0 to PIO1_7			I/O		Port 1 — Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block.
R/PIO1_0/ AD1/CT32B1_CAP0	7 [4]	yes	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_0 — General purpose digital input/output pin.
			I	-	AD1 — A/D converter, input 1.
			I	-	CT32B1_CAP0 — Capture input 0 for 32-bit timer 1.
R/PIO1_1/ AD2/CT32B1_MAT0	8 [4]	no	O	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_1 — General purpose digital input/output pin.
			I	-	AD2 — A/D converter, input 2.
			O	-	CT32B1_MAT0 — Match output 0 for 32-bit timer 1.
R/PIO1_2/ AD3/CT32B1_MAT1	9 [4]	no	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_2 — General purpose digital input/output pin.
			I	-	AD3 — A/D converter, input 3.
			O	-	CT32B1_MAT1 — Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ AD4/CT32B1_MAT2	10 [4]	no	I/O	I; PU	SWDIO — Serial wire debug input/output.
			I/O	-	PIO1_3 — General purpose digital input/output pin.
			I	-	AD4 — A/D converter, input 4.
			O	-	CT32B1_MAT2 — Match output 2 for 32-bit timer 1.
PIO1_6/RXD/ CT32B0_MAT0	11 [3]	no	I/O	I; PU	PIO1_6 — General purpose digital input/output pin.
			I	-	RXD — Receiver input for UART.
			O	-	CT32B0_MAT0 — Match output 0 for 32-bit timer 0.
PIO1_7/TXD/ CT32B0_MAT1	12 [3]	no	I/O	I; PU	PIO1_7 — General purpose digital input/output pin.
			O	-	TXD — Transmitter output for UART.
			O	-	CT32B0_MAT1 — Match output 1 for 32-bit timer 0.
V _{DD}	15	-	I	-	3.3 V supply voltage to the internal regulator and the external rail.

Table 8. LPC1100 and LPC1100L series: LPC1113/14 pin description table (LQFP48 package)

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO0_0 to PIO0_11			I/O		Port 0 — Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.
RESET/PIO0_0	3 ^[2]	yes	I	I; PU	RESET — External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The RESET pin can be left unconnected or be used as a GPIO pin if an external RESET function is not needed and Deep power-down mode is not used.
			I/O	-	PIO0_0 — General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/ CT32B0_MAT2	4 ^[3]	yes	I/O	I; PU	PIO0_1 — General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
			O	-	CLKOUT — Clockout pin.
			O	-	CT32B0_MAT2 — Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	10 ^[3]	yes	I/O	I; PU	PIO0_2 — General purpose digital input/output pin.
			I/O	-	SSEL0 — Slave Select for SPI0.
			I	-	CT16B0_CAP0 — Capture input 0 for 16-bit timer 0.
PIO0_3	14 ^[3]	yes	I/O	I; PU	PIO0_3 — General purpose digital input/output pin.
PIO0_4/SCL	15 ^[4]	yes	I/O	I; IA	PIO0_4 — General purpose digital input/output pin (open-drain).
			I/O	-	SCL — I ² C-bus, open-drain clock input/output. High-current sink only if I ² C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	16 ^[4]	yes	I/O	I; IA	PIO0_5 — General purpose digital input/output pin (open-drain).
			I/O	-	SDA — I ² C-bus, open-drain data input/output. High-current sink only if I ² C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	22 ^[3]	yes	I/O	I; PU	PIO0_6 — General purpose digital input/output pin.
			I/O	-	SCK0 — Serial clock for SPI0.
PIO0_7/CTS	23 ^[3]	yes	I/O	I; PU	PIO0_7 — General purpose digital input/output pin (high-current output driver).
			I	-	CTS — Clear To Send input for UART.
PIO0_8/MISO0/ CT16B0_MAT0	27 ^[3]	yes	I/O	I; PU	PIO0_8 — General purpose digital input/output pin.
			I/O	-	MISO0 — Master In Slave Out for SPI0.
			O	-	CT16B0_MAT0 — Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	28 ^[3]	yes	I/O	I; PU	PIO0_9 — General purpose digital input/output pin.
			I/O	-	MOSI0 — Master Out Slave In for SPI0.
			O	-	CT16B0_MAT1 — Match output 1 for 16-bit timer 0.

Table 10. LPC1100XL series: LPC1113/14/15 pin description table (LQFP48 and TFBGA48 package) ...continued

Symbol	LQFP48	TFBGA48	Start logic input	Type	Reset state [1]	Description
PIO3_2/ $\overline{\text{DCD}}$ / CT16B0_MAT2/ SCK1	43 ^[3]	A4 ^[3]	no	I/O	I; PU	PIO3_2 — General purpose digital input/output pin.
				I	-	DCD — Data Carrier Detect input for UART.
				O	-	CT16B0_MAT2 — Match output 2 for 16-bit timer 0.
				I/O	-	SCK1 — Serial clock for SPI1.
PIO3_3/ $\overline{\text{RI}}$ / CT16B0_CAP0	48 ^[3]	A2 ^[3]	no	I/O	I; PU	PIO3_3 — General purpose digital input/output pin.
				I	-	RI — Ring Indicator input for UART.
				I	-	CT16B0_CAP0 — Capture input 0 for 16-bit timer 0.
PIO3_4/ CT16B0_CAP1/RXD	18 ^[3]	H4 ^[3]	no	I/O	I; PU	PIO3_4 — General purpose digital input/output pin.
				I	-	CT16B0_CAP1 — Capture input 1 for 16-bit timer 0.
				I	-	RXD — Receiver input for UART
PIO3_5/ CT16B1_CAP1/TXD	21 ^[3]	G6 ^[3]	no	I/O	I; PU	PIO3_5 — General purpose digital input/output pin.
				I	-	CT16B1_CAP1 — Capture input 1 for 16-bit timer 1.
				O	-	TXD — Transmitter output for UART
V _{DD}	8; 44	E2; B4	-	I	-	3.3 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	6 ^[6]	D1 ^[6]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	7 ^[6]	E1 ^[6]	-	O	-	Output from the oscillator amplifier.
V _{SS}	5; 41	D2; B5	-	I	-	Ground.

- [1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level (V_{DD} = 3.3 V)); IA = inactive, no pull-up/down enabled.
- [2] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See [Figure 52](#) for the reset pad configuration.
- [3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see [Figure 51](#)).
- [4] I²C-bus pads compliant with the I²C-bus specification for I²C standard mode and I²C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.
- [5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see [Figure 51](#)).
- [6] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

Table 11. LPC1100XL series: LPC1111/12/13/14 pin description table (HVQFN33 package)

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO0_0 to PIO0_11					Port 0 — Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.
RESET/PIO0_0	2[2]	yes	I	I;PU	RESET — External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The RESET pin can be left unconnected or be used as a GPIO pin if an external RESET function is not needed and Deep power-down mode is not used.
			I/O	-	PIO0_0 — General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/ CT32B0_MAT2	3[3]	yes	I/O	I;PU	PIO0_1 — General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
			O	-	CLKOUT — Clock out pin.
			O	-	CT32B0_MAT2 — Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	8[3]	yes	I/O	I;PU	PIO0_2 — General purpose digital input/output pin.
			I/O	-	SSEL0 — Slave select for SPI0.
			I	-	CT16B0_CAP0 — Capture input 0 for 16-bit timer 0.
PIO0_3	9[3]	yes	I/O	I;PU	PIO0_3 — General purpose digital input/output pin.
PIO0_4/SCL	10[4]	yes	I/O	I;IA	PIO0_4 — General purpose digital input/output pin (open-drain).
			I/O	-	SCL — I ² C-bus, open-drain clock input/output. High-current sink only if I ² C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	11[4]	yes	I/O	I;IA	PIO0_5 — General purpose digital input/output pin (open-drain).
			I/O	-	SDA — I ² C-bus, open-drain data input/output. High-current sink only if I ² C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	15[3]	yes	I/O	I;PU	PIO0_6 — General purpose digital input/output pin.
			I/O	-	SCK0 — Serial clock for SPI0.
PIO0_7/CTS	16[3]	yes	I/O	I;PU	PIO0_7 — General purpose digital input/output pin (high-current output driver).
			I	-	CTS — Clear To Send input for UART.
PIO0_8/MISO0/ CT16B0_MAT0	17[3]	yes	I/O	I;PU	PIO0_8 — General purpose digital input/output pin.
			I/O	-	MISO0 — Master In Slave Out for SPI0.
			O	-	CT16B0_MAT0 — Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	18[3]	yes	I/O	I;PU	PIO0_9 — General purpose digital input/output pin.
			I/O	-	MOSI0 — Master Out Slave In for SPI0.
			O	-	CT16B0_MAT1 — Match output 1 for 16-bit timer 0.
SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2	19[3]	yes	I	I;PU	SWCLK — Serial wire clock.
			I/O	-	PIO0_10 — General purpose digital input/output pin.
			I/O	-	SCK0 — Serial clock for SPI0.
			O	-	CT16B0_MAT2 — Match output 2 for 16-bit timer 0.

Table 11. LPC1100XL series: LPC1111/12/13/14 pin description table (HVQFN33 package) ...continued

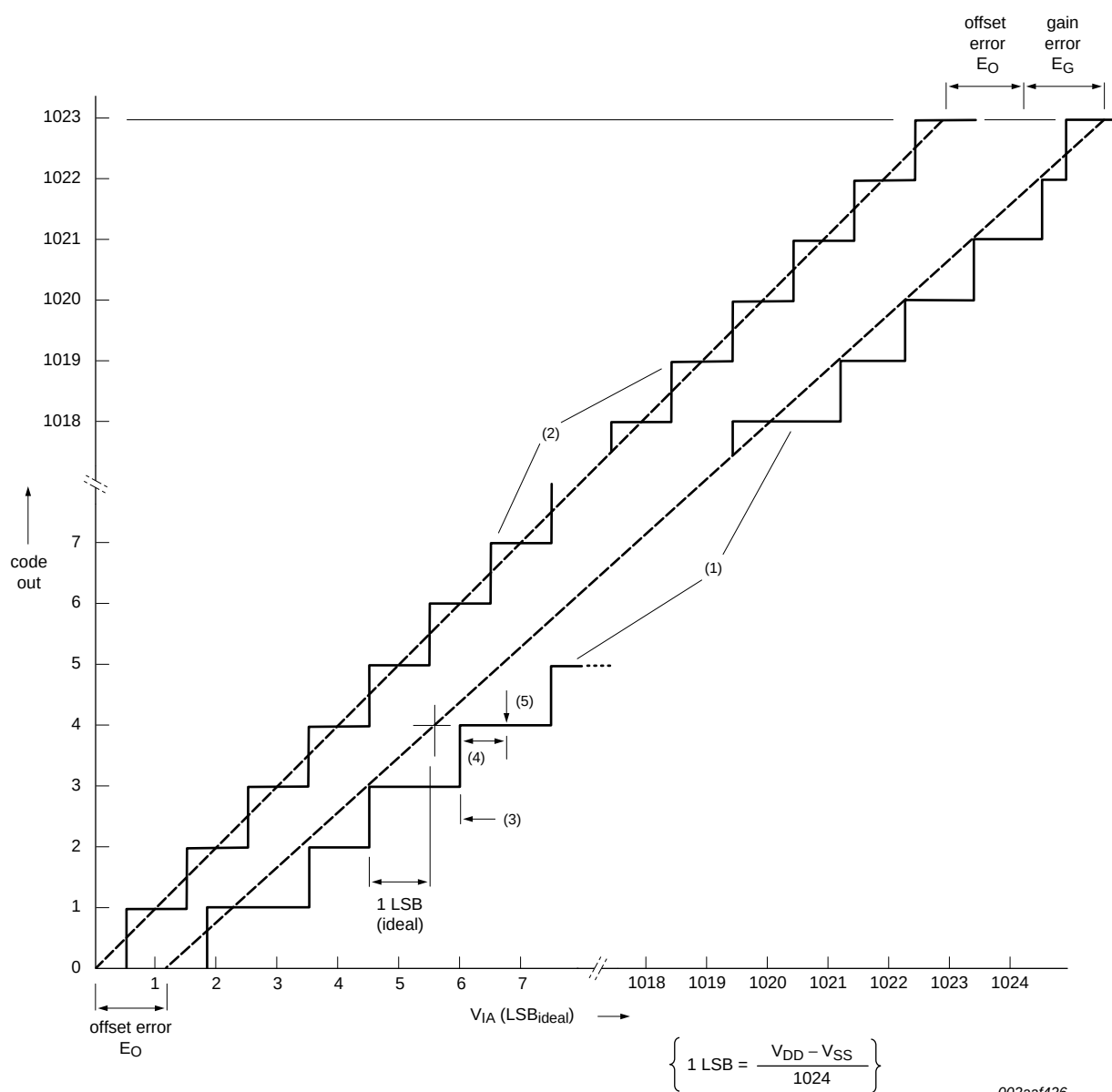
Symbol	Pin	Start logic input	Type	Reset state [1]	Description
R/PIO0_11/AD0/ CT32B0_MAT3	21 ^[5]	yes	-	I;PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO0_11 — General purpose digital input/output pin.
			I	-	AD0 — A/D converter, input 0.
			O	-	CT32B0_MAT3 — Match output 3 for 32-bit timer 0.
PIO1_0 to PIO1_11					Port 1 — Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block.
R/PIO1_0/AD1/ CT32B1_CAP0	22 ^[5]	yes	-	I;PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_0 — General purpose digital input/output pin.
			I	-	AD1 — A/D converter, input 1.
			I	-	CT32B1_CAP0 — Capture input 0 for 32-bit timer 1.
R/PIO1_1/AD2/ CT32B1_MAT0	23 ^[5]	no	-	I;PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_1 — General purpose digital input/output pin.
			I	-	AD2 — A/D converter, input 2.
			O	-	CT32B1_MAT0 — Match output 0 for 32-bit timer 1.
R/PIO1_2/AD3/ CT32B1_MAT1	24 ^[5]	no	-	I;PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_2 — General purpose digital input/output pin.
			I	-	AD3 — A/D converter, input 3.
			O	-	CT32B1_MAT1 — Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ AD4/CT32B1_MAT2	25 ^[5]	no	I/O	I;PU	SWDIO — Serial wire debug input/output.
			I/O	-	PIO1_3 — General purpose digital input/output pin.
			I	-	AD4 — A/D converter, input 4.
			O	-	CT32B1_MAT2 — Match output 2 for 32-bit timer 1.
PIO1_4/AD5/ CT32B1_MAT3/ WAKEUP	26 ^[5]	no	I/O	I;PU	PIO1_4 — General purpose digital input/output pin with 10 ns glitch filter. In Deep power-down mode, this pin serves as the Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
			I	-	AD5 — A/D converter, input 5.
			O	-	CT32B1_MAT3 — Match output 3 for 32-bit timer 1.
PIO1_5/RTS/ CT32B0_CAP0	30 ^[3]	no	I/O	I;PU	PIO1_5 — General purpose digital input/output pin.
			O	-	RTS — Request To Send output for UART.
			I	-	CT32B0_CAP0 — Capture input 0 for 32-bit timer 0.
PIO1_6/RXD/ CT32B0_MAT0	31 ^[3]	no	I/O	I;PU	PIO1_6 — General purpose digital input/output pin.
			I	-	RXD — Receiver input for UART.
			O	-	CT32B0_MAT0 — Match output 0 for 32-bit timer 0.

Table 15. LPC111x/x02 Thermal resistance value (C/W): $\pm 15\%$

HVQFN33		LQFP48	
θ_{ja}		θ_{ja}	
JEDEC (4.5 in $\times$ 4 in)		JEDEC (4.5 in $\times$ 4 in)	
0 m/s	40.8	0 m/s	83.3
1 m/s	33.1	1 m/s	74.9
2.5 m/s	28.7	2.5 m/s	69.4
Single-layer (4.5 in $\times$ 3 in)		8-layer (4.5 in $\times$ 3 in)	
0 m/s	85.2	0 m/s	116.3
1 m/s	62	1 m/s	96
2.5 m/s	53.5	2.5 m/s	87.5
θ_{jc}	17.9	θ_{jc}	28.3
θ_{jb}	1.5	θ_{jb}	35.5

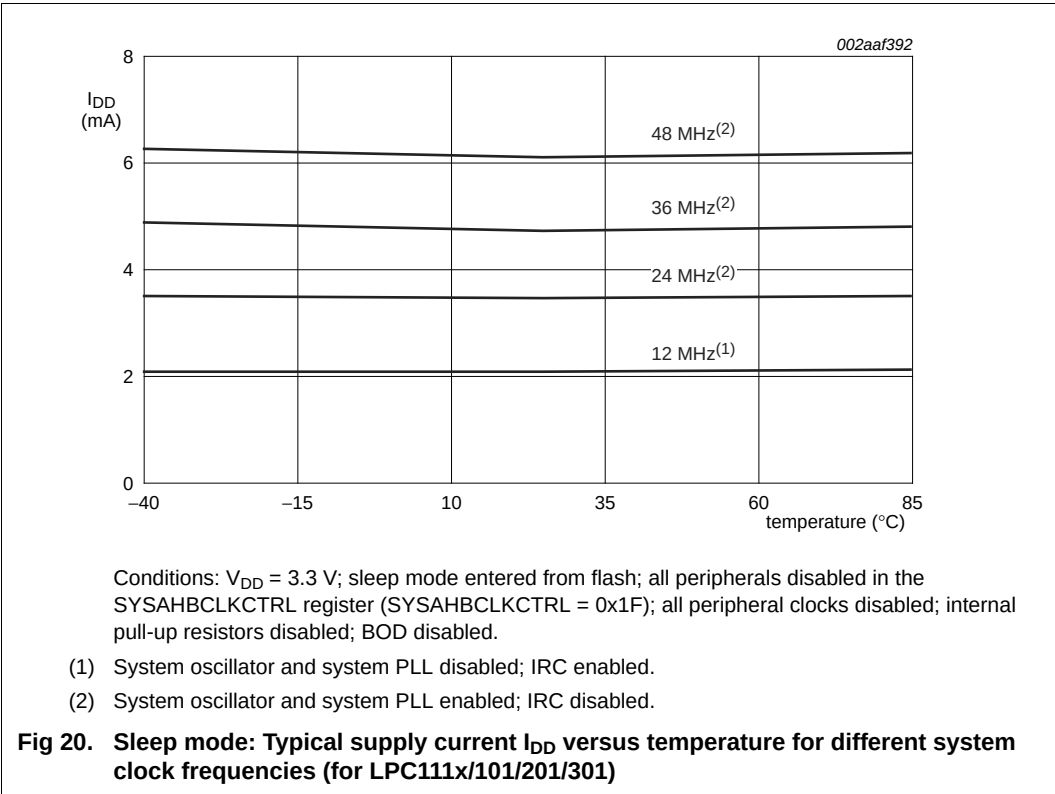
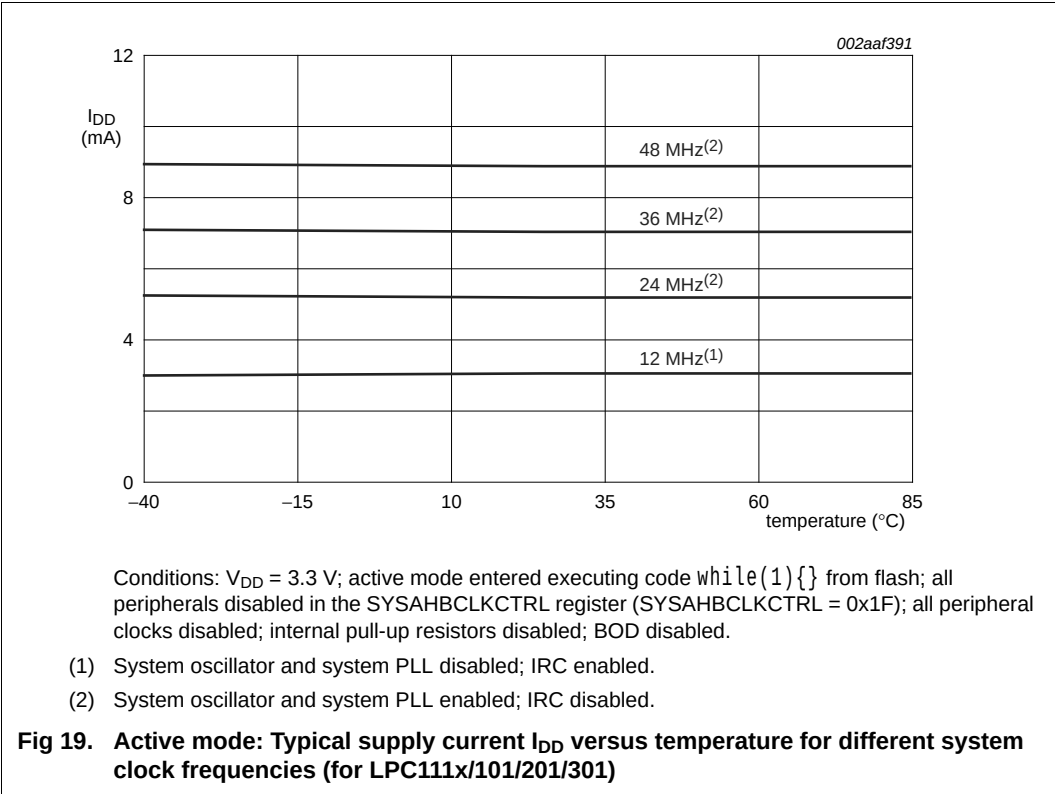
Table 17. Static characteristics (LPC1100XL series) ...continued $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$, unless otherwise specified.

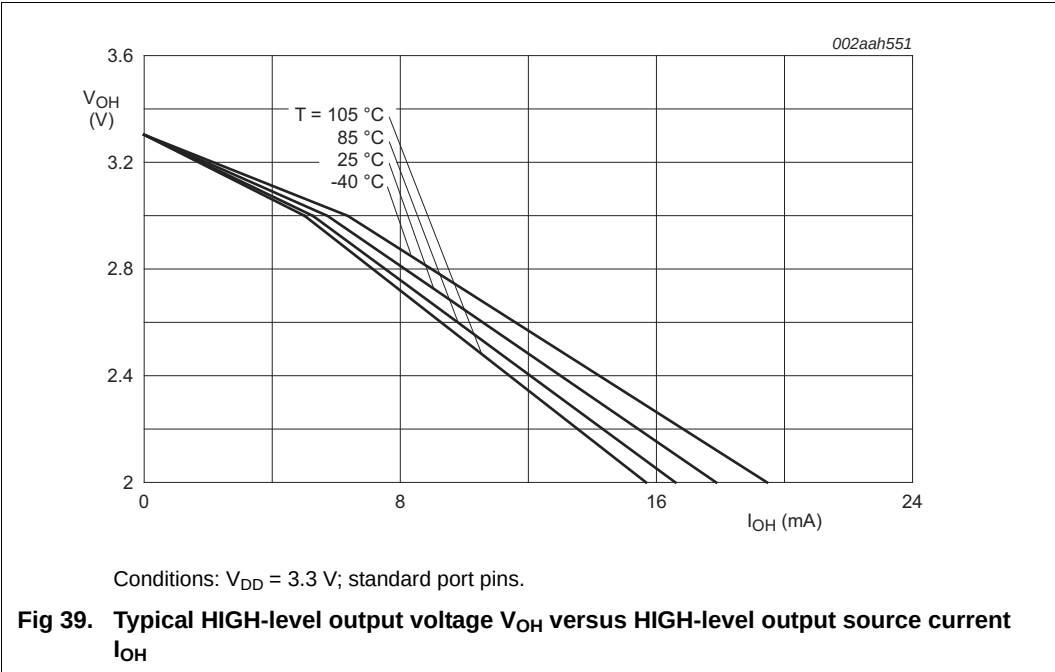
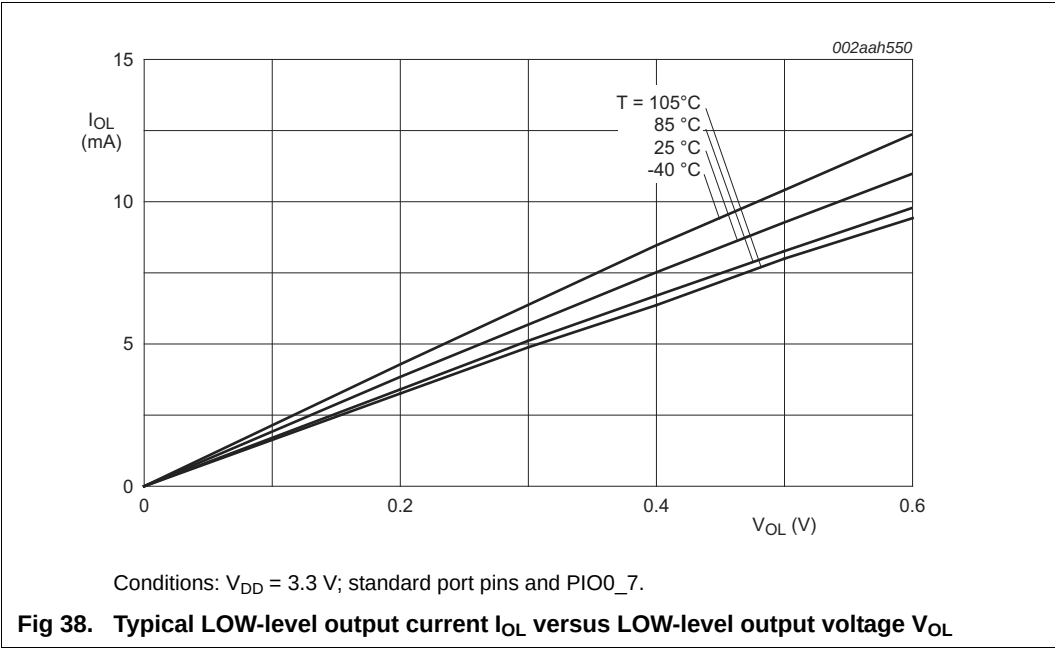
Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
V _{OH}	HIGH-level output voltage	2.5 V ≤ V _{DD} ≤ 3.6 V; I _{OH} = −20 mA	V _{DD} − 0.4	-	-	V
		1.8 V ≤ V _{DD} < 2.5 V; I _{OH} = −12 mA	V _{DD} − 0.4	-	-	V
V _{OL}	LOW-level output voltage	2.5 V ≤ V _{DD} ≤ 3.6 V; I _{OL} = 4 mA	-	-	0.4	V
		1.8 V ≤ V _{DD} < 2.5 V; I _{OL} = 3 mA	-	-	0.4	V
I _{OH}	HIGH-level output current	V _{OH} = V _{DD} − 0.4 V; 2.5 V ≤ V _{DD} ≤ 3.6 V	20	-	-	mA
		1.8 V ≤ V _{DD} < 2.5 V	12	-	-	mA
I _{OL}	LOW-level output current	V _{OL} = 0.4 V 2.5 V ≤ V _{DD} ≤ 3.6 V	4	-	-	mA
		1.8 V ≤ V _{DD} < 2.5 V	3	-	-	mA
I _{OLS}	LOW-level short-circuit output current	V _{OL} = V _{DD} ^[16]	-	-	50	mA
I _{pd}	pull-down current	V _I = 5 V	10	50	150	μA
I _{pu}	pull-up current	V _I = 0 V 2.0 V ≤ V _{DD} ≤ 3.6 V	−15	−50	−85	μA
		1.8 V ≤ V _{DD} < 2.0 V	−10	−50	−85	μA
		V _{DD} < V _I < 5 V	0	0	0	μA
I ² C-bus pins (PIO0_4 and PIO0_5)						
V _{IH}	HIGH-level input voltage		0.7V _{DD}	-	-	V
V _{IL}	LOW-level input voltage		-	-	0.3V _{DD}	V
V _{hys}	hysteresis voltage		-	0.05V _{DD}	-	V
I _{OL}	LOW-level output current	V _{OL} = 0.4 V; I ² C-bus pins configured as standard mode pins 2.5 V ≤ V _{DD} ≤ 3.6 V	3.5	-	-	mA
		1.8 V ≤ V _{DD} < 2.5 V	3	-	-	
I _{OL}	LOW-level output current	V _{OL} = 0.4 V; I ² C-bus pins configured as Fast-mode Plus pins 2.5 V ≤ V _{DD} ≤ 3.6 V	20	-	-	mA
		1.8 V ≤ V _{DD} < 2.5 V	16	-	-	
I _{LI}	input leakage current	V _I = V _{DD} ^[17]	-	2	4	μA
		V _I = 5 V	-	10	22	μA

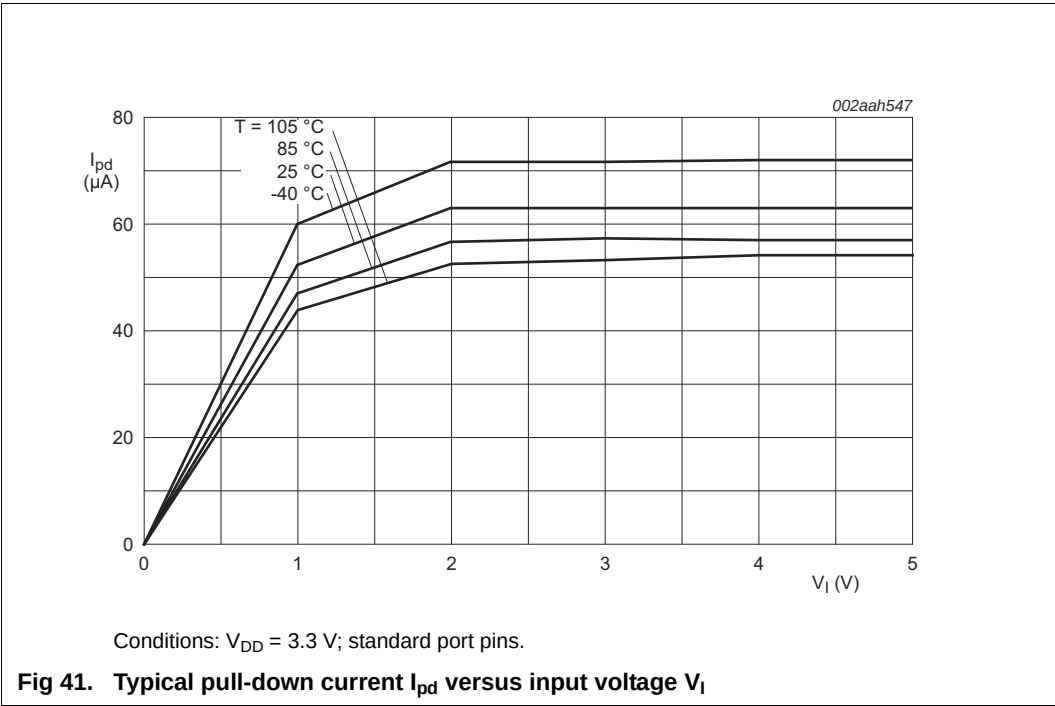
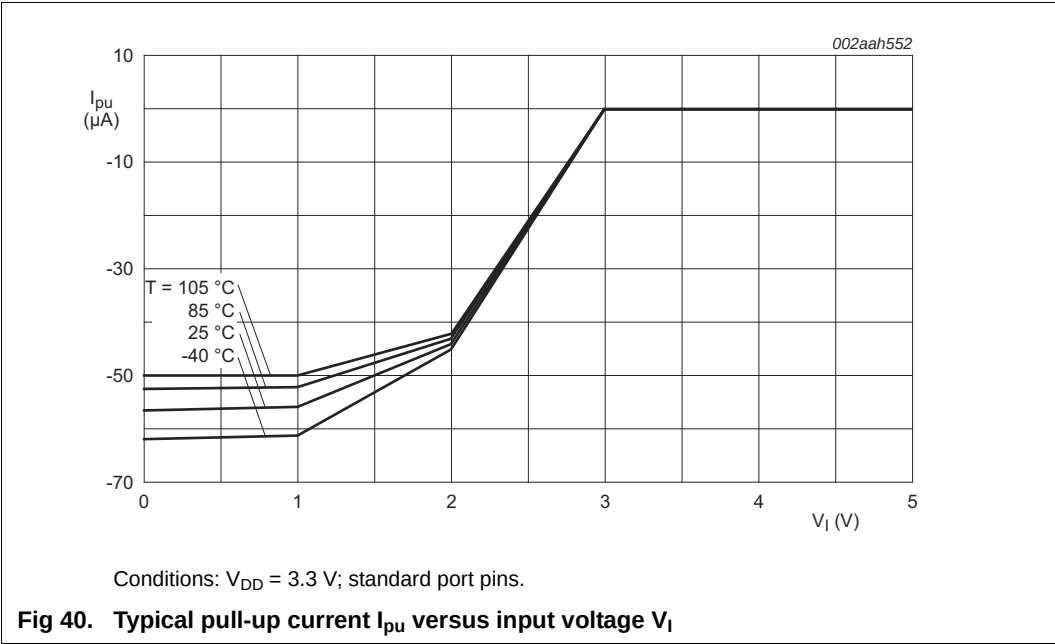


- (1) Example of an actual transfer curve.
- (2) The ideal transfer curve.
- (3) Differential linearity error (E_D).
- (4) Integral non-linearity ($E_{L(adj)}$).
- (5) Center of a step of the actual transfer curve.

Fig 17. ADC characteristics







11.3 External clock

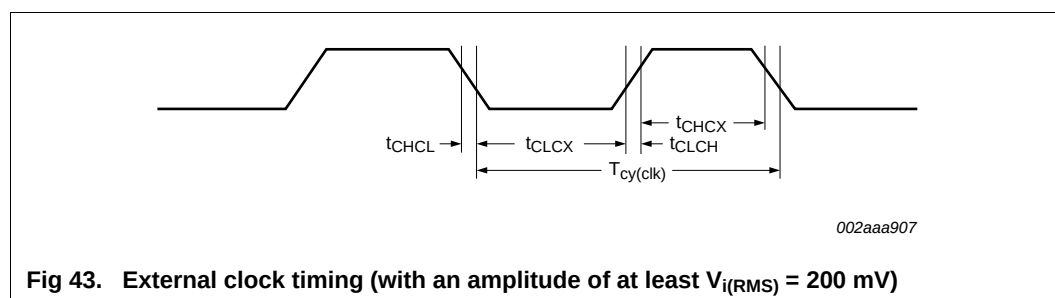
Table 24. Dynamic characteristic: external clock

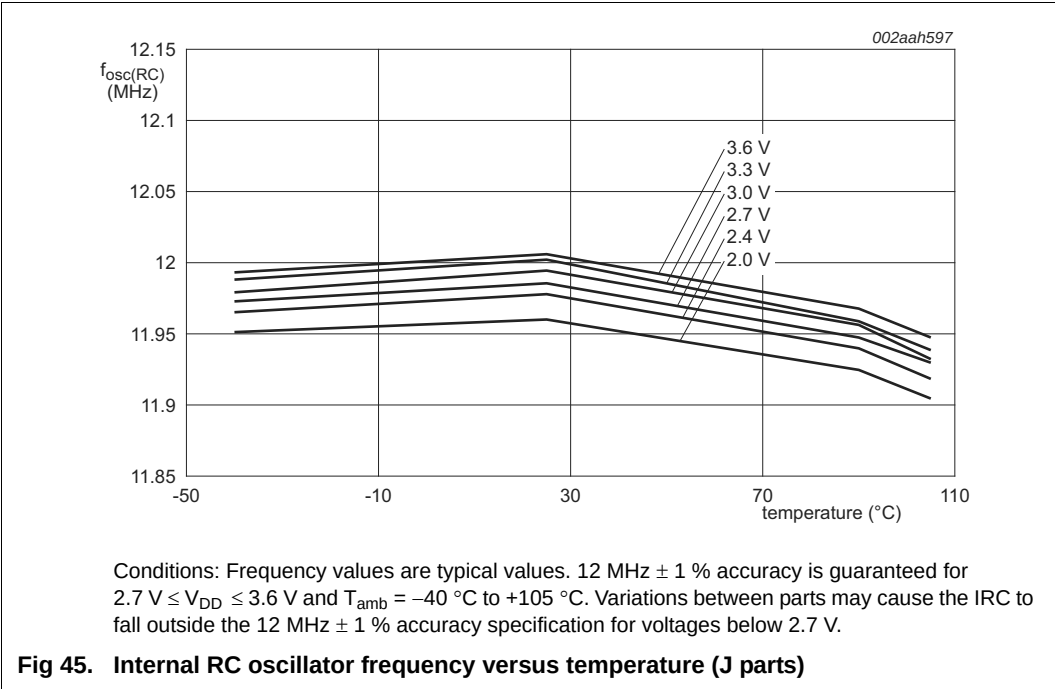
$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$; V_{DD} over specified ranges.^[1]

Symbol	Parameter	Conditions	Min	Typ ^[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.





11.6 I²C-bus

Table 28. Dynamic characteristic: I²C-bus pins^[1]

$T_{amb} = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$.^[2]

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency	Standard-mode	0	100	kHz
		Fast-mode	0	400	kHz
		Fast-mode Plus	0	1	MHz
t_f	fall time ^{[4][5][6][7]}	of both SDA and SCL signals Standard-mode	-	300	ns
		Fast-mode	$20 + 0.1 \times C_b$	300	ns
		Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock	Standard-mode	4.7	-	μs
		Fast-mode	1.3	-	μs
		Fast-mode Plus	0.5	-	μs
t_{HIGH}	HIGH period of the SCL clock	Standard-mode	4.0	-	μs
		Fast-mode	0.6	-	μs
		Fast-mode Plus	0.26	-	μs
$t_{HD;DAT}$	data hold time ^{[3][4][8]}	Standard-mode	0	-	μs
		Fast-mode	0	-	μs
		Fast-mode Plus	0	-	μs
$t_{SU;DAT}$	data set-up time ^{[9][10]}	Standard-mode	250	-	ns
		Fast-mode	100	-	ns
		Fast-mode Plus	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f .

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

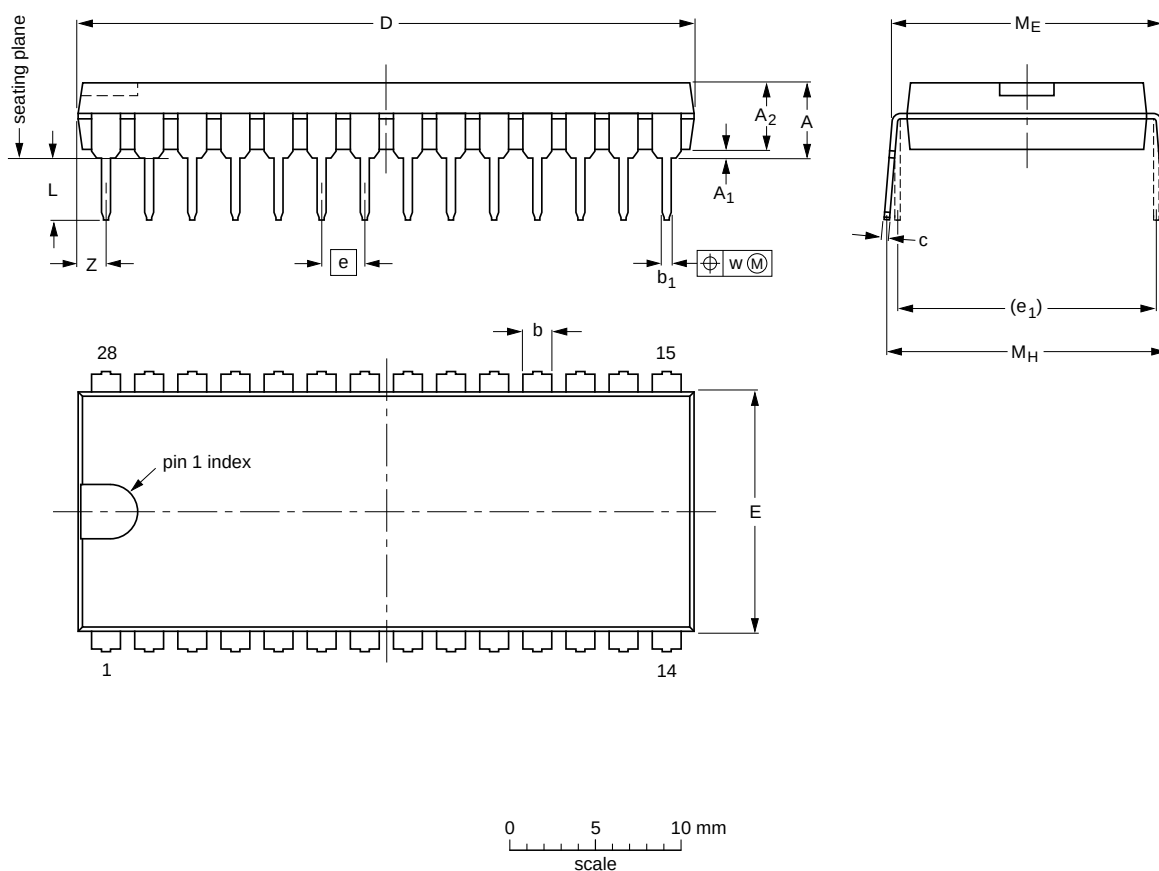
[8] The maximum $t_{HD;DAT}$ could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT} = 250\text{ ns}$ must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{f(max)} + t_{SU;DAT} = 1000 + 250 = 1250\text{ ns}$ (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

DIP28: plastic dual in-line package; 28 leads (600 mil)

SOT117-1



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	5.1	0.51	4	1.7 1.3	0.53 0.38	0.32 0.23	36 35	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.2	0.02	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.1	0.6	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

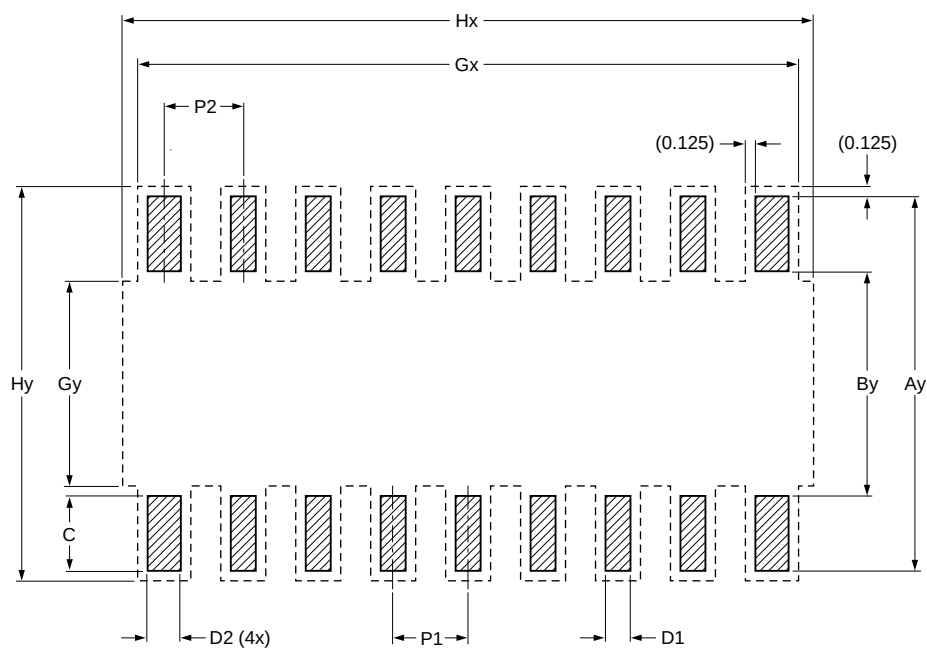
1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT117-1	051G05	MO-015	SC-510-28			99-12-27 03-02-13

Fig 57. Package outline SOT117-1 (DIP28)

Footprint information for reflow soldering of TSSOP28 package

SOT361-1



Generic footprint pattern
Refer to the package outline drawing for actual layout



solder land

--- occupied area

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	9.500	5.300	11.800	7.450

sot361-1 fr

Fig 65. Reflow soldering of the TSSOP28 package

15. Abbreviations

Table 33. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
GPIO	General Purpose Input/Output
PLL	Phase-Locked Loop
RC	Resistor-Capacitor
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
TEM	Transverse ElectroMagnetic
UART	Universal Asynchronous Receiver/Transmitter

16. References

- [1] LPC111x/LPC11Cxx User manual UM10398:
http://www.nxp.com/documents/user_manual/UM10398.pdf
- [2] LPC111x Errata sheet:
http://www.nxp.com/documents/errata_sheet/ES_LPC111X.pdf

17. Revision history

Table 34. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC111X v.9.2	20140326	Product data sheet	-	LPC111X v.9.1
Modifications:	- Pin description tables for RESET/PIO0_0 updated: In deep power-down mode, this pin must be pulled HIGH externally. The RESET pin can be left unconnected or be used as a GPIO pin if an external RESET function is not needed. See Section 6.2. - Pin description notes relating to open-drain I2C-bus pins updated for clarity in Section 6.2. - Pin description of the WAKEUP pin updated for clarity. See Section 6.2. - Parts added: LPC1114JHI33/303, LPC1111JHN33/103, LPC1112JHN33/203, LPC1113JHN33/203, LPC1114JHN33/303, LPC1114JBD48/333, LPC1112FHI33/102, LPC1114JBD48/303, LPC1114JBD48/323, LPC1113JBD48/303, LPC1113JHN33/303, LPC1112JHN33/103, LPC1111JHN33/203, LPC1114JHN33/203.			
LPC111X v.9.1	20131213	Product data sheet	-	LPC111X v.9
Modifications:	- Table 17 "Static characteristics (LPC1100XL series)": - Added I_{DD} max spec for Deep-sleep and Deep power-down modes @ 25 °C and 105 °C. - Added Table note 11 "105 °C spec applies only to the LPC1112JHI33, LPC1114JHN33, LPC1115JBD48, and LPC1115JET48 parts." - Updated Table note 12 "WAKEUP pin and RESET pin are pulled HIGH externally." - Table 16 "Static characteristics (LPC1100, LPC1100L series)": - Updated Table note 9 "WAKEUP pin and RESET pin are pulled HIGH externally."			
LPC111X v.9	20131029	Product data sheet	-	LPC111X v.8.2
Modifications:	- Added LPC1112JHI33/203, LPC1114JHN33/333, LPC1115JBD48/303, and LPC1115JET48/303 parts. - Removed t_{clk(H)} and t_{clk(L)} from Figure 47 "SPI master timing in SPI mode" and Figure 48 "SPI slave timing in SPI mode"; spec not characterized. - Table 22 "Power-up characteristics[1]": Added table note "Does not apply to LPC1100XL series".			
LPC111X v.8.2	20130805	Product data sheet	-	LPC111X v.8.1
Modifications:	Added LPC1115FET48/303.			
LPC111X v.8.1	20130524	Product data sheet	-	LPC111X v.8
Modifications:	- Table 4 thru Table 11: Added "5 V tolerant pad" to RESET/PIO0_0 table note. - Added Section 9 "Thermal characteristics". - SRAM size corrected for part LPC1112FHN24/202 (4 kB). See Table 2.			
LPC111X v.8	20130220	Product data sheet	-	LPC111X v.7.5
Modifications:	- Table 16 "Static characteristics" added Pin capacitance section. - Default pin state corrected for pins PIO0_4 and PIO0_5 (I; IA) in Table 11 "LPC1100XL series: LPC1111/12/13/14 pin description table (HVQFN33 package)". - Table 12 "Limiting values" expanded for clarity. - Table 19 "Power consumption at very low frequencies using the watchdog oscillator" added. - Added Section 12.2 "Use of ADC input trigger signals". - Added Section 12.8 "ADC effective input impedance".			
LPC111X v.7.5	20121002	Product data sheet	-	LPC111X v.7.4

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