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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	42
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1115fbd48-303-1

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NXP Semiconductors

LPC1110/11/12/13/14/15



NXP Semiconductors

LPC1110/11/12/13/14/15





- [1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level); IA = inactive, no pull-up/down enabled.
- [2] 5 V tolerant pad. RESET functionality is not available in Deep power-down mode.
- [3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 51).
- [4] I²C-bus pin compliant with the I²C-bus specification for I²C standard mode and I²C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.
- [5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 51).
- [6] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

Table 5. LPC1100L series: LPC1112 pin description table (TSSOP20 with V_{DDA} and V_{SSA} pins)

Symbol	Pin TSSOP20		Start logic input	Туре	Reset state [1]	Description			
PIO0_0 to PIO0_11				I/O		Port 0 — Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.			
RESET/PIO0_0	17	[2]	yes	I	I; PU	J RESET — External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address of In deep power-down mode, this pin must be pulled HIGH externally. The RESET pin can be left unconnected or be used as a GPIO pin if an external RESET function is not needed and Deep power-down mode is not used.			
				I/O	-	PIO0_0 — General purpose digital input/output pin with 10 ns glitch filter.			
PIO0_1/CLKOUT/ CT32B0_MAT2	18	[3]	yes	I/O	I; PU	PIO0_1 — General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.			
				0	-	CLKOUT — Clockout pin.			
				0	-	CT32B0_MAT2 — Match output 2 for 32-bit timer 0.			
PIO0_2/SSEL0/	19	[3]	yes	I/O	I; PU	PIO0_2 — General purpose digital input/output pin.			
CT16B0_CAP0				I/O	-	SSEL0 — Slave Select for SPI0.			
				I	-	CT16B0_CAP0 — Capture input 0 for 16-bit timer 0.			
PIO0_3	20	[3]	yes	I/O	I; PU	PIO0_3 — General purpose digital input/output pin.			
PIO0_8/MISO0/	1	[3]	yes	I/O	I; PU	PIO0_8 — General purpose digital input/output pin.			
C116B0_MAT0				I/O	-	MISO0 — Master In Slave Out for SPI0.			
				0	-	CT16B0_MAT0 — Match output 0 for 16-bit timer 0.			
PIO0_9/MOSI0/	2	[3]	yes	I/O	I; PU	PIO0_9 — General purpose digital input/output pin.			
C116B0_MA11				I/O	-	MOSI0 — Master Out Slave In for SPI0.			
				0	-	CT16B0_MAT1 — Match output 1 for 16-bit timer 0.			

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Symbol	HVQFN pin	Start logic input	Туре	Reset state [1]	Description
SWDIO/PIO1_3/	19 <u>^[5]</u>	no	I/O	I; PU	SWDIO — Serial wire debug input/output.
AD4/CT32B1_MAT2			I/O	-	PIO1_3 — General purpose digital input/output pin.
			I	-	AD4 — A/D converter, input 4.
			0	-	CT32B1_MAT2 — Match output 2 for 32-bit timer 1.
PIO1_4/AD5/ CT32B1_MAT3/ WAKEUP	20 <u>[5]</u>	no	I/O I; PU PIO1_4 — General purpose digital input/ glitch filter. In Deep power-down mode, th Deep power-down mode wake-up pin wit Pull this pin HIGH externally before enteri mode. Pull this pin LOW to exit Deep pow LOW-going pulse as short as 50 ns wake I - AD5 — A/D converter, input 5.		PIO1_4 — General purpose digital input/output pin with 10 ns glitch filter. In Deep power-down mode, this pin serves as the Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
			I	-	AD5 — A/D converter, input 5.
			0	-	CT32B1_MAT3 — Match output 3 for 32-bit timer 1.
PIO1_6/RXD/ 23 ^[3]		no	I/O	I; PU	PIO1_6 — General purpose digital input/output pin.
CT32B0_MAT0			I	-	RXD — Receiver input for UART.
			0	-	CT32B0_MAT0 — Match output 0 for 32-bit timer 0.
PIO1_7/TXD/	24 <u>[3]</u>	no	I/O	I; PU	PIO1_7 — General purpose digital input/output pin.
CT32B0_MAT1			0	-	TXD — Transmitter output for UART.
			0	-	CT32B0_MAT1 — Match output 1 for 32-bit timer 0.
PIO1_8/	6 <u>[3]</u>	no	I/O	I; PU	PIO1_8 — General purpose digital input/output pin.
CT16B1_CAP0			I	-	CT16B1_CAP0 — Capture input 0 for 16-bit timer 1.
XTALIN	4 <u>[6]</u>	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
V _{DD}	5; 22	-	I	-	1.8 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
V _{SS}	3; 21	-	I	-	Ground.

Table 6. LPC1100L series: LPC1112 (HVQFN24 package) ... continued

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level); IA = inactive, no pull-up/down enabled.

[2] 5 V tolerant pad. RESET functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See <u>Figure 52</u> for the reset pad configuration.

[3] Pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 51).

[4] I²C-bus pads compliant with the I²C-bus specification for I²C standard mode and I²C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[5] Pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled (see Figure 51).

[6] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

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Symbol	Pin	Start logic input	Туре	Reset state [1]	Description			
PIO0_0 to PIO0_11					Port 0 — Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.			
RESET/PIO0_0	2 <u>[2]</u>	yes	1	I;PU	RESET — External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states and processor execution to begin at address 0.			
					In deep power-down mode, this pin must be pulled HIGH externally. The RESET pin can be left unconnected or be used as a GPIO pin if an external RESET function is not needed and Deep power-down mode is not used.			
			I/O	-	PIO0_0 — General purpose digital input/output pin with 10 ns glitch filter.			
PIO0_1/CLKOUT/ CT32B0_MAT2	3 <u>[3]</u>	yes	I/O	I;PU	PIO0_1 — General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.			
			0	-	CLKOUT — Clock out pin.			
			0	-	CT32B0_MAT2 — Match output 2 for 32-bit timer 0.			
PIO0_2/SSEL0/	8 <u>[3]</u>	yes	I/O	I;PU	PIO0_2 — General purpose digital input/output pin.			
CI16B0_CAP0			I/O	-	SSEL0 — Slave select for SPI0.			
			I	-	CT16B0_CAP0 — Capture input 0 for 16-bit timer 0.			
PIO0_3	9 <u>[3]</u>	yes	I/O	I;PU	PIO0_3 — General purpose digital input/output pin.			
PIO0_4/SCL	10 <u>^[4]</u>	yes	I/O	I;IA	PIO0_4 — General purpose digital input/output pin (open-drain).			
			I/O	-	SCL — I ² C-bus, open-drain clock input/output. High-current sink only if I ² C Fast-mode Plus is selected in the I/O configuration register.			
PIO0_5/SDA	11 <u>[4]</u>	yes	I/O	I;IA	PIO0_5 — General purpose digital input/output pin (open-drain).			
			I/O	-	SDA — I^2C -bus, open-drain data input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.			
PIO0_6/SCK0	15 <u>[3]</u>	yes	I/O	I;PU	PIO0_6 — General purpose digital input/output pin.			
			I/O	-	SCK0 — Serial clock for SPI0.			
PIO0_7/CTS	16 <u>[3]</u>	yes	I/O	I;PU	PIO0_7 — General purpose digital input/output pin (high-current output driver).			
			I	-	CTS — Clear To Send input for UART.			
PIO0_8/MISO0/	17 <u>[3]</u>	yes	I/O	I;PU	PIO0_8 — General purpose digital input/output pin.			
CT16B0_MAT0			I/O	-	MISO0 — Master In Slave Out for SPI0.			
			0	-	CT16B0_MAT0 — Match output 0 for 16-bit timer 0.			
PIO0_9/MOSI0/	18 <u>[3]</u>	yes	I/O	I;PU	PIO0_9 — General purpose digital input/output pin.			
CT16B0_MAT1			I/O	-	MOSI0 — Master Out Slave In for SPI0.			
			0	-	CT16B0_MAT1 — Match output 1 for 16-bit timer 0.			
SWCLK/PIO0_10/	19 <u>[3]</u>	yes	I	I;PU	SWCLK — Serial wire clock.			
SCK0/			I/O	-	PIO0_10 — General purpose digital input/output pin.			
CTTODU_WATZ			I/O	-	SCK0 — Serial clock for SPI0.			
			0	-	CT16B0_MAT2 — Match output 2 for 16-bit timer 0.			

Table 9. LPC1100 and LPC1100L series: LPC1111/12/13/14 pin description table (HVQFN33 package)

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Symbol	Pin	Start logic input	Туре	Reset state [1]	Description		
PIO1_7/TXD/	32 <u>[3]</u>	no	I/O	I;PU	PIO1_7 — General purpose digital input/output pin.		
CT32B0_MAT1			0	-	TXD — Transmitter output for UART.		
			0	-	CT32B0_MAT1 — Match output 1 for 32-bit timer 0.		
PIO1_8/	7 <u>[3]</u>	no	I/O	I;PU	PIO1_8 — General purpose digital input/output pin.		
CT16B1_CAP0			I	-	CT16B1_CAP0 — Capture input 0 for 16-bit timer 1.		
PIO1_9/	12 <u>[3]</u>	no	I/O	I;PU	PIO1_9 — General purpose digital input/output pin.		
CT16B1_MAT0			0	-	CT16B1_MAT0 — Match output 0 for 16-bit timer 1.		
PIO1_10/AD6/	20 <u>^[5]</u>	no	I/O	I;PU	PIO1_10 — General purpose digital input/output pin.		
CT16B1_MAT1			I	-	AD6 — A/D converter, input 6.		
			0	-	CT16B1_MAT1 — Match output 1 for 16-bit timer 1.		
PIO1_11/AD7	27 <u>[5]</u>	no	I/O	I;PU	PIO1_11 — General purpose digital input/output pin.		
			I	-	AD7 — A/D converter, input 7.		
PIO2_0					Port 2 — Port 2 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 2 pins depends of the function selected through the IOCONFIG register block. Pins PIO2_1 to PIO2_11 are not available.		
PIO2_0/DTR	1 <u>[3]</u>	no	I/O	I;PU	PIO2_0 — General purpose digital input/output pin.		
			0	-	DTR — Data Terminal Ready output for UART.		
PIO3_0 to PIO3_5					Port 3 — Port 3 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 3 pins depends on the function selected through the IOCONFIG register block. Pins PIO3_0, PIO3_1, PIO3_3 and PIO3_6 to PIO3_11 are not available.		
PIO3_2	28 <u>[3]</u>	no	I/O	I;PU	PIO3_2 — General purpose digital input/output pin.		
PIO3_4	13 <u>[3]</u>	no	I/O	I;PU	PIO3_4 — General purpose digital input/output pin.		
PIO3_5	14 <u>[3]</u>	no	I/O	I;PU	PIO3_5 — General purpose digital input/output pin.		
V _{DD}	6; 29	-	1	-	3.3 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.		
XTALIN	4 <u>[6]</u>	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.		
XTALOUT	5 <u>[6]</u>	-	0	-	Output from the oscillator amplifier.		
V _{SS}	33	-	-	-	Thermal pad. Connect to ground.		

Table 9. LPC1100 and LPC1100L series: LPC1111/12/13/14 pin description table (HVQFN33 package) ...continued

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to 2.6 V for LPC111x/101/201/301, pins pulled up to full V_{DD} level on LPC111x/002/102/202/302 (V_{DD} = 3.3 V)); IA = inactive, no pull-up/down enabled.

[2] 5 V tolerant pad. RESET functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See <u>Figure 52</u> for the reset pad configuration.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 51).

[4] I²C-bus pads compliant with the I²C-bus specification for I²C standard mode and I²C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled, and the pin is not 5 V tolerant (see Figure 51).

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7.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

Controls system exceptions and peripheral interrupts.

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The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

7.16.1.3 Watchdog oscillator

The watchdog oscillator can be used as a clock source that directly drives the CPU, the watchdog timer, or the CLKOUT pin. The watchdog oscillator nominal frequency is programmable between 9.4 kHz and 2.3 MHz. The frequency spread over processing and temperature is \pm 40 %.

7.16.2 System PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The PLL output frequency must be lower than 100 MHz. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μ s.

7.16.3 Clock output

The LPC1110/11/12/13/14/15 features a clock output function that routes the IRC oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin.

7.16.4 Wake-up process

The LPC1110/11/12/13/14/15 begin operation at power-up and when awakened from Deep power-down mode by using the 12 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the system oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

7.16.5 Power control

The LPC1110/11/12/13/14/15 support a variety of power control features. There are three special modes of processor power reduction: Sleep mode, Deep-sleep mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

7.16.5.1 Power profiles (LPC1100L and LPC1100XL series only)

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC1110/11/12/13/14/15 for one of the following power modes:

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9. Thermal characteristics

The average chip junction temperature, $T_{j}\,(^{\circ}C),$ can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \tag{1}$$

- T_{amb} = ambient temperature (°C),
- R_{th(j-a)} = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD} . The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 13. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
T _{j(max)}	maximum junction		-	-	125	°C
	temperature					

Table 14. LPC111x/x01 Thermal resistance value (°C/W): ±15 %

HVQFN33		LQFP48			
θја		θја			
JEDEC (4.5 in × 4 in)		JEDEC (4.5 in \times 4 in)			
0 m/s	40.4	0 m/s	82.1		
1 m/s	32.7	1 m/s	73.7		
2.5 m/s	28.3	2.5 m/s	68.2		
Single-layer (4.5 in $ imes$ 3 in)		8-layer (4.5 in × 3 in)			
0 m/s	84.8	0 m/s	115.2		
1 m/s	61.6	1 m/s	94.7		
2.5 m/s	53.1	2.5 m/s	86.3		
θјс	20.3	өјс	29.6		
θjb	1.1	θjb	34.2		

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Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see *LPC111x user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCONFIG block.
- Configure GPIO pins as outputs using the GPIOnDIR registers.
- Write 0 to all GPIOnDATA registers to drive the outputs LOW.



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10.9 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at $T_{amb} = 25$ °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 48 MHz.

Peripheral	Typical s mA	upply cur	rent in	Notes	
	n/a	12 MHz	48 MHz		
IRC	0.27	-	-	System oscillator running; PLL off; independent of main clock frequency.	
System oscillator at 12 MHz	0.22	-	-	IRC running; PLL off; independent of main clock frequency.	
Watchdog oscillator at 500 kHz/2	0.004	-	-	System oscillator running; PLL off; independent of main clock frequency.	
BOD	0.051	-	-	Independent of main clock frequency.	
Main PLL	-	0.21	-		
ADC	-	0.08	0.29		
CLKOUT	-	0.12	0.47	Main clock divided by 4 in the CLKOUTDIV register.	
CT16B0	-	0.02	0.06		
CT16B1	-	0.02	0.06		
CT32B0	-	0.02	0.07		
CT32B1	-	0.02	0.06		
GPIO	-	0.23	0.88	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.	
IOCONFIG	-	0.03	0.10		
12C	-	0.04	0.13		
ROM	-	0.04	0.15		
SPI0	-	0.12	0.45		
SPI1	-	0.12	0.45		
UART	-	0.22	0.82		
WDT/WWDT	-	0.02	0.06	Main clock selected as clock source for the WDT.	

 Table 21.
 Power consumption for individual analog and digital blocks

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Product data sheet

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11.6 I²C-bus

Table 28. Dynamic characteristic: I²C-bus pins^[1]

 $T_{amb} = -40 \ ^{\circ}C \ to +105 \ ^{\circ}C.$

Symbol	Parameter		Conditions	Min	Max	Unit
f _{SCL}	SCL clock		Standard-mode	0	100	kHz
	frequency		Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t _f	fall time	[4][5][6][7]	of both SDA and SCL signals	-	300	ns
			Standard-mode			
			Fast-mode	$20 + 0.1 \times C_b$	300	ns
			Fast-mode Plus	-	120	ns
t _{LOW} L	LOW period of		Standard-mode	4.7	-	μS
	the SCL clock		Fast-mode	1.3	-	μS
			Fast-mode Plus	0.5	-	μS
t _{HIGH} HIG the	HIGH period of		Standard-mode	4.0	-	μS
	the SCL clock		Fast-mode	0.6	-	μS
			Fast-mode Plus	0.26	-	μS
t _{HD;DAT}	data hold time	[3][4][8]	Standard-mode	0	-	μS
			Fast-mode	0	-	μS
			Fast-mode Plus	0	-	μS
t _{SU;DAT}	data set-up	[9][10]	Standard-mode	250	-	ns
	time		Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] See the I²C-bus specification UM10204 for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

- [3] t_{HD;DAT} is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.
- [5] C_b = total capacitance of one bus line in pF.
- [6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
- [7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
- [8] The maximum $t_{HD;DAT}$ could be 3.45 μ s and 0.9 μ s for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.
- [9] t_{SU;DAT} is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.
- [10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT} = 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

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12.7 ElectroMagnetic Compatibility (EMC)

Radiated emission measurements according to the IEC61967-2 standard using the TEM-cell method are shown for the LPC1114FBD48/302 in Table 32.

Table 32. ElectroMagnetic Compatibility (EMC) for part LPC1114FBD48/302 (TEM-cell method)

 $V_{DD} = 3.3 V; T_{amb} = 25 °C.$

Parameter	Frequency band	System clock =	Unit				
		12 MHz	24 MHz	48 MHz			
Input clock: IRC (12 MHz)							
maximum peak level	150 kHz to 30 MHz	-7	-5	-7	dBμV		
	30 MHz to 150 MHz	-2	1	10	dBμV		
	150 MHz to 1 GHz	4	8	16	dBμV		
IEC level ^[1]	-	0	N	М	-		
Input clock: o	crystal oscillator (12 N	lHz)					
maximum peak level	150 kHz to 30 MHz	-7	-7	-7	dBμV		
	30 MHz to 150 MHz	-2	1	8	dBμV		
	150 MHz to 1 GHz	4	7	14	dBμV		
IEC level ^[1]	-	0	Ν	Μ	-		

[1] IEC levels refer to Appendix D in the IEC61967-2 Specification.

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HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm

Fig 58. Package outline (HVQFN33 5x5)

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