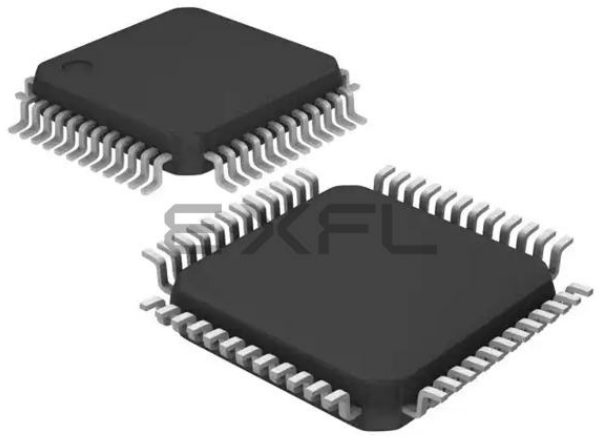

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	42
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1115jbd48-303ql

- Digital peripherals:
  - Up to 42 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors. In addition, a configurable open-drain mode is supported on the LPC1100L and LPC1100XL series.
  - GPIO pins can be used as edge and level sensitive interrupt sources.
  - High-current output driver (20 mA) on one pin.
  - High-current sink drivers (20 mA) on two I^2C-bus pins in Fast-mode Plus (not on LPC1112FDH20/102).
  - Four general purpose counter/timers with up to eight capture inputs and up to 13 match outputs.
  - Programmable WatchDog Timer (WDT) the LPC1100 series only.
  - Programmable windowed WDT on the LPC1100L and LPC1100XL series only.
- Analog peripherals:
  - 10-bit ADC with input multiplexing among 5, 6, or 8 pins depending on package size.
- Serial interfaces:
  - UART with fractional baud rate generation, internal FIFO, and RS-485 support.
  - Two SPI controllers with SSP features and with FIFO and multi-protocol capabilities (second SPI on LPC1100 and LPC1100L series LQFP48 package only).
  - I^2C-bus interface supporting full I^2C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode (not on LPC1112FDH20/102).
- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as a system clock.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - Programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.
  - PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator or the internal RC oscillator.
  - Clock output function with divider that can reflect the system oscillator clock, IRC clock, CPU clock, and the Watchdog clock.
- Power control:
  - Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, and Deep power-down modes.
  - Power profiles residing in boot ROM allowing to optimize performance and minimize power consumption for any given application through one simple function call. (LPC1100L and LPC1100XL series only.)
  - Three reduced power modes: Sleep, Deep-sleep, and Deep power-down.
  - Processor wake-up from Deep-sleep mode via a dedicated start logic using up to 13 of the functional pins.
  - Power-On Reset (POR).
  - Brownout detect with up to four separate thresholds for interrupt and forced reset.
- Unique device serial number for identification.
- Single power supply (1.8 V to 3.6 V).
- Available as LQFP48 package, HVQFN33 package, and TFBGA48 package.

- LPC1100L series available as TSSOP28 package, DIP28 package, TSSOP20 package, and SO20 package.
- Extended temperature (−40 °C to +105 °C) for selected parts (see Table 2).

3. Applications

- eMetering
- Alarm systems
- Lighting
- White goods

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SO20, TSSOP20, TSSOP28, and DIP28 packages			
LPC1110FD20	SO20	SO20: plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
LPC1111FDH20/002	TSSOP20	TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
LPC1112FD20/102	SO20	SO20: plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
LPC1112FDH20/102	TSSOP20	TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
LPC1112FDH28/102	TSSOP28	TSSOP28: plastic thin shrink small outline package; 28 leads; body width 4.4 mm	SOT361-1
LPC1114FDH28/102	TSSOP28	TSSOP28: plastic thin shrink small outline package; 28 leads; body width 4.4 mm	SOT361-1
LPC1114FN28/102	DIP28	DIP28: plastic dual in-line package; 28 leads (600 mil)	SOT117-1
HVQFN24/33, LQFP48, and TFBGA48 packages			
LPC1111FHN33/101	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1111FHN33/102	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1111FHN33/201	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1111FHN33/202	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1111FHN33/103	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1111JHN33/103	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1111FHN33/203	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1111JHN33/203	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1112FHN33/101	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a
LPC1112FHN33/102	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 × 7 × 0.85 mm	n/a

Table 3. Pin description overview

Part	Pin description table	Pinning diagram
LPC1114FHN33/203	Table 11	Figure 7
LPC1114JHN33/203	Table 11	Figure 7
LPC1114FHN33/301	Table 9	Figure 6
LPC1114FHN33/302	Table 9	Figure 6
LPC1114JHN33/303	Table 11	Figure 7
LPC1114FHN33/303	Table 11	Figure 7
LPC1114FHN33/333	Table 11	Figure 7
LPC1114JHN33/333	Table 11	Figure 7
LPC1114FHI33/302	Table 9	Figure 6
LPC1114FHI33/303	Table 11	Figure 7
LPC1114JHI33/303	Table 11	Figure 7
LPC1113FBD48/301	Table 8	Figure 3
LPC1113FBD48/302	Table 8	Figure 3
LPC1113FBD48/303	Table 10	Figure 4
LPC1113JBD48/303	Table 10	Figure 4
LPC1114FBD48/301	Table 8	Figure 3
LPC1114FBD48/302	Table 8	Figure 3
LPC1114FBD48/303	Table 10	Figure 4
LPC1114JBD48/303	Table 10	Figure 4
LPC1114FBD48/323	Table 10	Figure 4
LPC1114JBD48/323	Table 10	Figure 4
LPC1114FBD48/333	Table 10	Figure 4
LPC1114JBD48/333	Table 10	Figure 4
LPC1115FBD48/303	Table 10	Figure 4
LPC1115JBD48/303	Table 10	Figure 4
LPC1115FET48/303	Table 10	Figure 5
LPC1115JET48/303	Table 10	Figure 5

Table 6. LPC1100L series: LPC1112 (HVQFN24 package) *…continued*

Symbol	HVQFN pin	Start logic input	Type	Reset state [1]	Description
PIO0_5/SDA	9[4]	yes	I/O	I; IA	**PIO0_5 —** General purpose digital input/output pin (open-drain).
			I/O	-	**SDA —** I^2C-bus, open-drain data input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	10[3]	yes	I/O	I; PU	**PIO0_6 —** General purpose digital input/output pin.
			I/O	-	**SCK0 —** Serial clock for SPI0.
PIO0_7/$\overline{\text{CTS}}$	11[3]	yes	I/O	I; PU	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
			I	-	**$\overline{\text{CTS}}$ —** Clear To Send input for UART.
PIO0_8/MISO0/ CT16B0_MAT0	12[3]	yes	I/O	I; PU	**PIO0_8 —** General purpose digital input/output pin.
			I/O	-	**MISO0 —** Master In Slave Out for SPI0.
			O	-	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	13[3]	yes	I/O	I; PU	**PIO0_9 —** General purpose digital input/output pin.
			I/O	-	**MOSI0 —** Master Out Slave In for SPI0.
			O	-	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2	14[3]	yes	I	I; PU	**SWCLK —** Serial wire clock.
			I/O	-	**PIO0_10 —** General purpose digital input/output pin.
			I/O	-	**SCK0 —** Serial clock for SPI0.
			O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
R/PIO0_11/ AD0/CT32B0_MAT3	15[5]	yes	I	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO0_11 —** General purpose digital input/output pin.
			I	-	**AD0 —** A/D converter, input 0.
			O	-	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
R/PIO1_0/ AD1/CT32B1_CAP0	16[5]	yes	I	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO1_0 —** General purpose digital input/output pin.
			I	-	**AD1 —** A/D converter, input 1.
			I	-	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
R/PIO1_1/ AD2/CT32B1_MAT0	17[5]	no	O	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO1_1 —** General purpose digital input/output pin.
			I	-	**AD2 —** A/D converter, input 2.
			O	-	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
R/PIO1_2/ AD3/CT32B1_MAT1	18[5]	no	I	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO1_2 —** General purpose digital input/output pin.
			I	-	**AD3 —** A/D converter, input 3.
			O	-	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.

Table 9. LPC1100 and LPC1100L series: LPC1111/12/13/14 pin description table (HVQFN33 package) *…continued*

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO1_7/TXD/ CT32B0_MAT1	32[3]	no	I/O	I;PU	**PIO1_7 —** General purpose digital input/output pin.
			O	-	**TXD —** Transmitter output for UART.
			O	-	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO1_8/ CT16B1_CAP0	7[3]	no	I/O	I;PU	**PIO1_8 —** General purpose digital input/output pin.
			I	-	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
PIO1_9/ CT16B1_MAT0	12[3]	no	I/O	I;PU	**PIO1_9 —** General purpose digital input/output pin.
			O	-	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
PIO1_10/AD6/ CT16B1_MAT1	20[5]	no	I/O	I;PU	**PIO1_10 —** General purpose digital input/output pin.
			I	-	**AD6 —** A/D converter, input 6.
			O	-	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
PIO1_11/AD7	27[5]	no	I/O	I;PU	**PIO1_11 —** General purpose digital input/output pin.
			I	-	**AD7 —** A/D converter, input 7.
PIO2_0					**Port 2 —** Port 2 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 2 pins depends on the function selected through the IOCONFIG register block. Pins PIO2_1 to PIO2_11 are not available.
PIO2_0/$\overline{\text{DTR}}$	1[3]	no	I/O	I;PU	**PIO2_0 —** General purpose digital input/output pin.
			O	-	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for UART.
PIO3_0 to PIO3_5					**Port 3 —** Port 3 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 3 pins depends on the function selected through the IOCONFIG register block. Pins PIO3_0, PIO3_1, PIO3_3 and PIO3_6 to PIO3_11 are not available.
PIO3_2	28[3]	no	I/O	I;PU	**PIO3_2 —** General purpose digital input/output pin.
PIO3_4	13[3]	no	I/O	I;PU	**PIO3_4 —** General purpose digital input/output pin.
PIO3_5	14[3]	no	I/O	I;PU	**PIO3_5 —** General purpose digital input/output pin.
V_{DD}	6; 29	-	I	-	3.3 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	4[6]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	5[6]	-	O	-	Output from the oscillator amplifier.
V_{SS}	33	-	-	-	Thermal pad. Connect to ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to 2.6 V for LPC111x/101/201/301, pins pulled up to full V_{DD} level on LPC111x/002/102/202/302 (V_{DD} = 3.3 V)); IA = inactive, no pull-up/down enabled.

[2] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See Figure 52 for the reset pad configuration.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 51).

[4] I^2C-bus pads compliant with the I^2C-bus specification for I^2C standard mode and I^2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled, and the pin is not 5 V tolerant (see Figure 51).

Table 10. LPC1100XL series: LPC1113/14/15 pin description table (LQFP48 and TFBGA48 package) *…continued*

Symbol	LQFP48	TFBGA48	Start logic input	Type	Reset state [1]	Description
PIO0_8/MISO0/ CT16B0_MAT0	27[3]	F8[3]	yes	I/O	I; PU	**PIO0_8 —** General purpose digital input/output pin.
				I/O	-	**MISO0 —** Master In Slave Out for SPI0.
				O	-	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	28[3]	F7[3]	yes	I/O	I; PU	**PIO0_9 —** General purpose digital input/output pin.
				I/O	-	**MOSI0 —** Master Out Slave In for SPI0.
				O	-	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2	29[3]	E7[3]	yes	I	I; PU	**SWCLK —** Serial wire clock.
				I/O	-	**PIO0_10 —** General purpose digital input/output pin.
				I/O	-	**SCK0 —** Serial clock for SPI0.
				O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
R/PIO0_11/ AD0/CT32B0_MAT3	32[5]	D8[5]	yes	I	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
				I/O	-	**PIO0_11 —** General purpose digital input/output pin.
				I	-	**AD0 —** A/D converter, input 0.
				O	-	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
PIO1_0 to PIO1_11				I/O		**Port 1 —** Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block.
R/PIO1_0/ AD1/CT32B1_CAP0	33[5]	C7[5]	yes	I	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
				I/O	-	**PIO1_0 —** General purpose digital input/output pin.
				I	-	**AD1 —** A/D converter, input 1.
				I	-	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
R/PIO1_1/ AD2/CT32B1_MAT0	34[5]	C8[5]	no	O	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
				I/O	-	**PIO1_1 —** General purpose digital input/output pin.
				I	-	**AD2 —** A/D converter, input 2.
				O	-	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
R/PIO1_2/ AD3/CT32B1_MAT1	35[5]	B7[5]	no	I	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
				I/O	-	**PIO1_2 —** General purpose digital input/output pin.
				I	-	**AD3 —** A/D converter, input 3.
				O	-	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ AD4/CT32B1_MAT2	39[5]	B6[5]	no	I/O	I; PU	**SWDIO —** Serial wire debug input/output.
				I/O	-	**PIO1_3 —** General purpose digital input/output pin.
				I	-	**AD4 —** A/D converter, input 4.
				O	-	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.

Table 11. LPC1100XL series: LPC1111/12/13/14 pin description table (HVQFN33 package)

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO0_0 to PIO0_11					**Port 0 —** Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.
$\overline{\text{RESET}}$/PIO0_0	2[2]	yes	I	I;PU	**$\overline{\text{RESET}}$ —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO pin if an external $\overline{\text{RESET}}$ function is not needed and Deep power-down mode is not used.
			I/O	-	**PIO0_0 —** General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/ CT32B0_MAT2	3[3]	yes	I/O	I;PU	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
			O	-	**CLKOUT —** Clock out pin.
			O	-	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	8[3]	yes	I/O	I;PU	**PIO0_2 —** General purpose digital input/output pin.
			I/O	-	**SSEL0 —** Slave select for SPI0.
			I	-	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO0_3	9[3]	yes	I/O	I;PU	**PIO0_3 —** General purpose digital input/output pin.
PIO0_4/SCL	10[4]	yes	I/O	I;IA	**PIO0_4 —** General purpose digital input/output pin (open-drain).
			I/O	-	**SCL —** I^2C-bus, open-drain clock input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	11[4]	yes	I/O	I;IA	**PIO0_5 —** General purpose digital input/output pin (open-drain).
			I/O	-	**SDA —** I^2C-bus, open-drain data input/output. High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	15[3]	yes	I/O	I;PU	**PIO0_6 —** General purpose digital input/output pin.
			I/O	-	**SCK0 —** Serial clock for SPI0.
PIO0_7/$\overline{\text{CTS}}$	16[3]	yes	I/O	I;PU	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
			I	-	**$\overline{\text{CTS}}$ —** Clear To Send input for UART.
PIO0_8/MISO0/ CT16B0_MAT0	17[3]	yes	I/O	I;PU	**PIO0_8 —** General purpose digital input/output pin.
			I/O	-	**MISO0 —** Master In Slave Out for SPI0.
			O	-	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	18[3]	yes	I/O	I;PU	**PIO0_9 —** General purpose digital input/output pin.
			I/O	-	**MOSI0 —** Master Out Slave In for SPI0.
			O	-	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2	19[3]	yes	I	I;PU	**SWCLK —** Serial wire clock.
			I/O	-	**PIO0_10 —** General purpose digital input/output pin.
			I/O	-	**SCK0 —** Serial clock for SPI0.
			O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.

- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

7.10 I²C-bus serial I/O controller

The LPC1110/11/12/13/14/15 contain one I²C-bus controller.

Remark: Part LPC1112FDH20/102 does not contain the I²C-bus controller.

The I²C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock Line (SCL) and a Serial DAta line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.10.1 Features

- The I²C-interface is a standard I²C-bus compliant interface with open-drain pins. The I²C-bus interface also supports Fast-mode Plus with bit rates up to 1 Mbit/s.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I²C-bus can be used for test and diagnostic purposes.
- The I²C-bus controller supports multiple address recognition and a bus monitor mode.

7.11 10-bit ADC

The LPC1110/11/12/13/14/15 contain one ADC. It is a single 10-bit successive approximation ADC with eight channels.

7.11.1 Features

- 10-bit successive approximation ADC.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 V to V_{DD}.
- 10-bit conversion time $\geq$ 2.44 μs (up to 400 kSamples/s).
- Burst conversion mode for single or multiple inputs.

The start logic must be configured in the system configuration block and in the NVIC before being used.

7.17.2 Reset

Reset has four sources on the LPC1110/11/12/13/14/15: the $\overline{\text{RESET}}$ pin, the Watchdog reset, Power-On Reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

A LOW-going pulse as short as 50 ns resets the part.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

An external pull-up resistor is required on the $\overline{\text{RESET}}$ pin if Deep power-down mode is used.

7.17.3 Brownout detection

The LPC1110/11/12/13/14/15 includes up to four levels for monitoring the voltage on the V_{DD} pin. If this voltage falls below one of the selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC in order to cause a CPU interrupt; if not, software can monitor the signal by reading a dedicated status register. Four threshold levels can be selected to cause a forced reset of the chip.

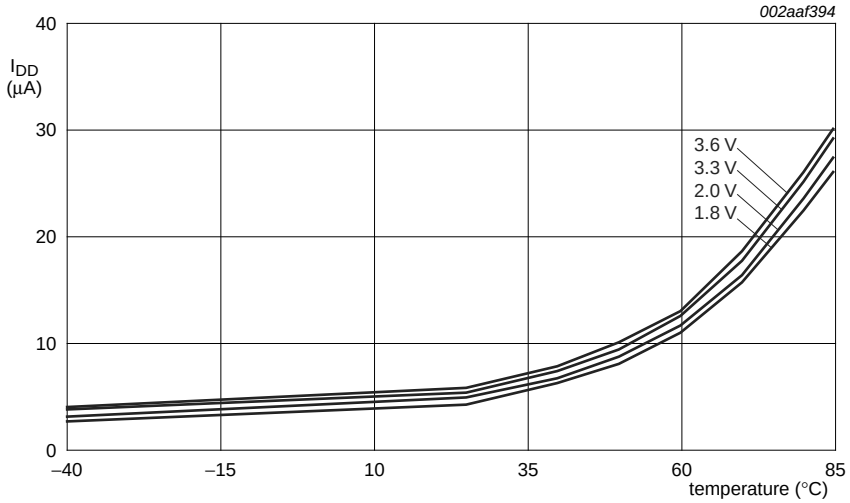
7.17.4 Code security (Code Read Protection - CRP)

This feature of the LPC1110/11/12/13/14/15 allows user to enable different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

In addition, ISP entry via the PIO0_1 pin can be disabled without enabling CRP. For details see the *LPC111x user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_1 pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via the UART.



Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 21. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD} (for LPC111x/101/201/301)

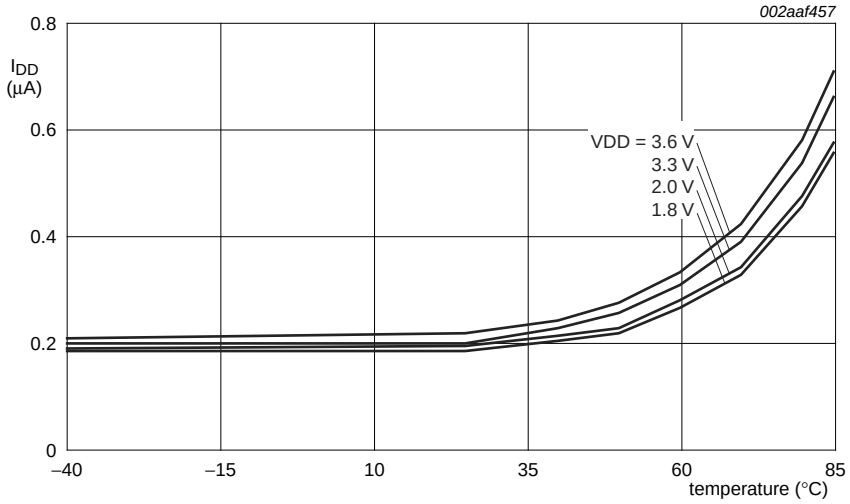


Fig 22. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD} (for LPC111x/101/201/301)

Table 26. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register; [2][3]	-	9.4	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register [2][3]	-	2300	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +105 °C) is ±40 %.

[3] See the LPC111x user manual.

11.5 I/O pins

Table 27. Dynamic characteristic: I/O pins[1]
T_{amb} = −40 °C to +105 °C; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	pin configured as output	3.0	-	5.0	ns
t_f	fall time	pin configured as output	2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

11.6 I²C-bus

Table 28. Dynamic characteristic: I²C-bus pins[1]
T_{amb} = −40 °C to +105 °C.[2]

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency	Standard-mode	0	100	kHz
		Fast-mode	0	400	kHz
		Fast-mode Plus	0	1	MHz
t_f	fall time [4][5][6][7]	of both SDA and SCL signals Standard-mode	-	300	ns
		Fast-mode	$20 + 0.1 \times C_b$	300	ns
		Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock	Standard-mode	4.7	-	µs
		Fast-mode	1.3	-	µs
		Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock	Standard-mode	4.0	-	µs
		Fast-mode	0.6	-	µs
		Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time [3][4][8]	Standard-mode	0	-	µs
		Fast-mode	0	-	µs
		Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time [9][10]	Standard-mode	250	-	ns
		Fast-mode	100	-	ns
		Fast-mode Plus	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

12. Application information

12.1 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 18:

- The ADC input trace must be short and as close as possible to the LPC1110/11/12/13/14/15 chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- Because the ADC and the digital core share the same power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

12.2 Use of ADC input trigger signals

For applications that use trigger signals to start conversions and require a precise sample frequency, ensure that the period of the trigger signal is an integral multiple of the period of the ADC clock.

12.3 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV (RMS) is needed.

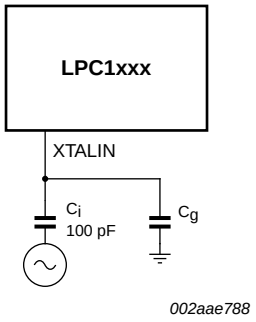


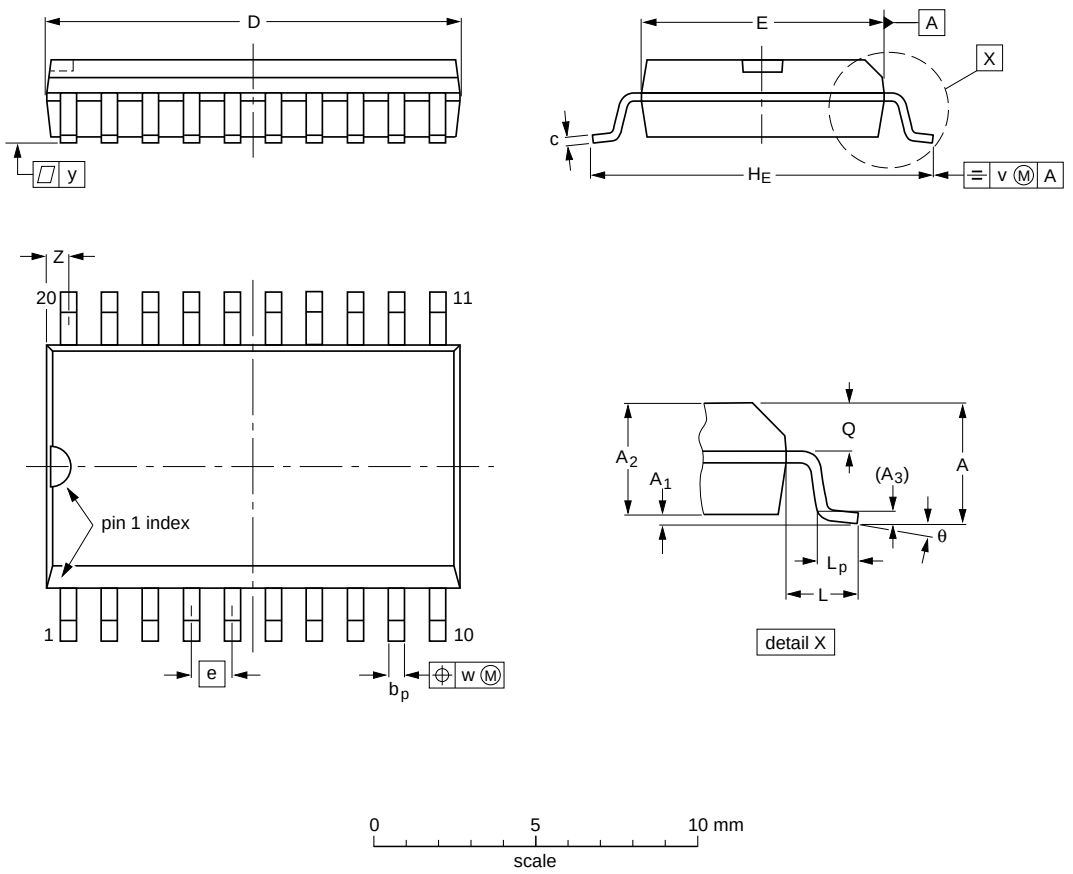
Fig 49. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 49), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 50 and in Table 30 and Table 31. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of

13. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

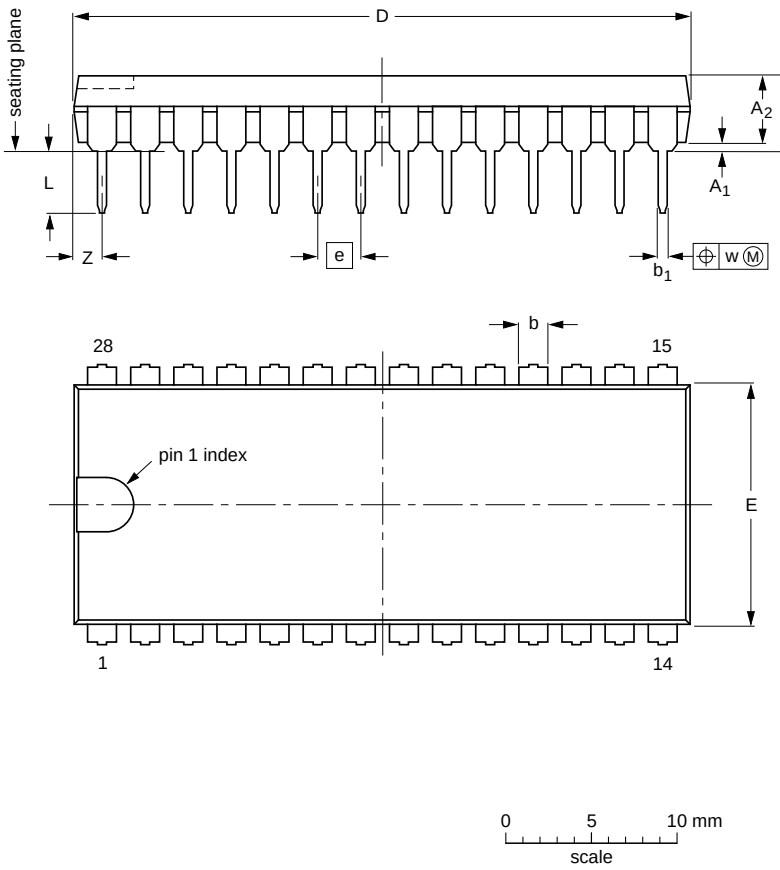
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 54. Package outline SOT163-1 (SO20)

DIP28: plastic dual in-line package; 28 leads (600 mil) **SOT117-1**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4	1.7 1.3	0.53 0.38	0.32 0.23	36 35	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.2	0.02	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.1	0.6	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

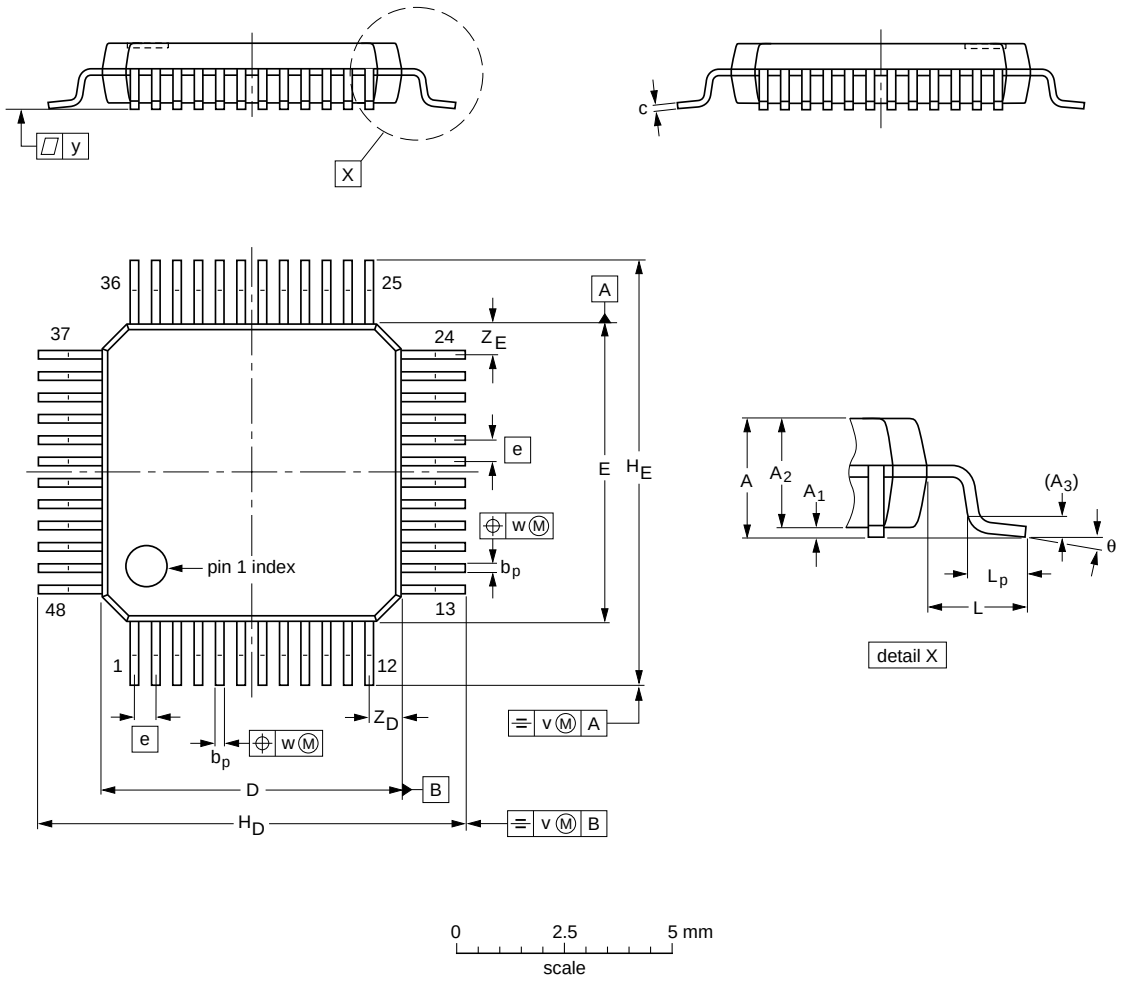
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT117-1	051G05	MO-015	SC-510-28			~~99-12-27~~ 03-02-13

Fig 57. Package outline SOT117-1 (DIP28)

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

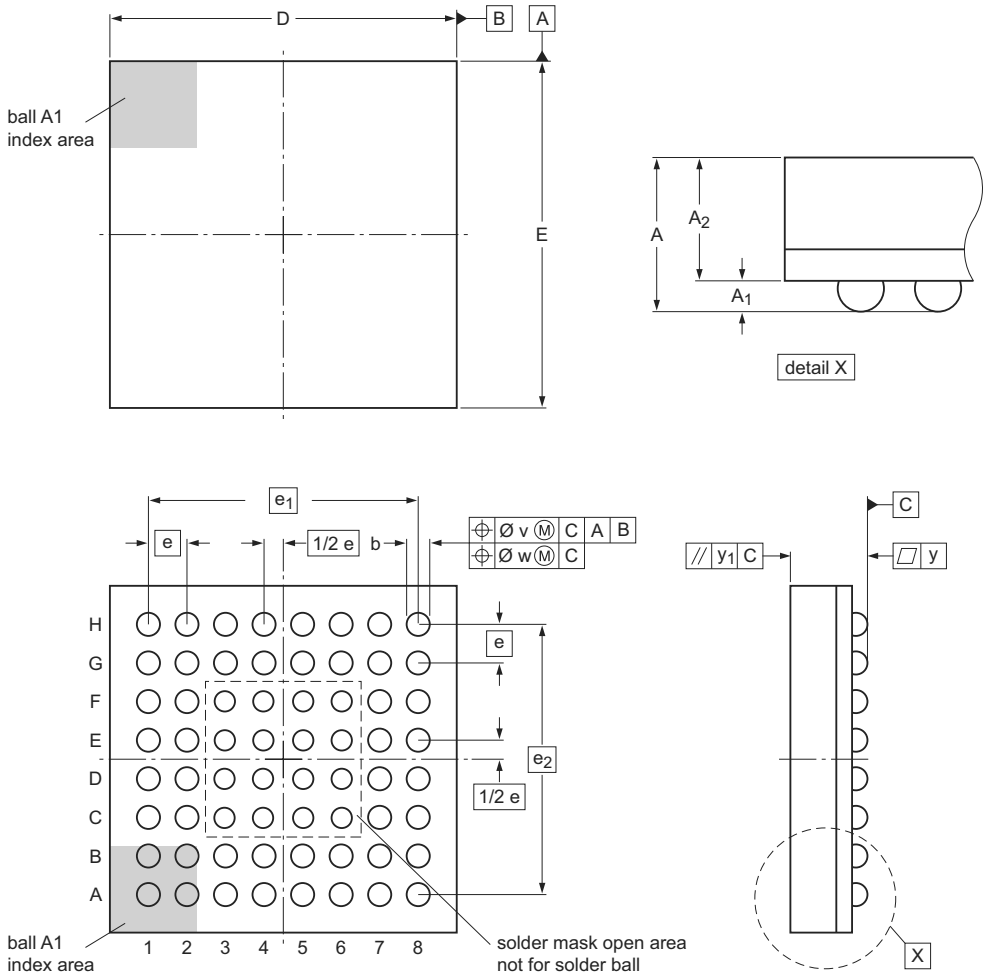
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 60. Package outline SOT313-2 (LQFP48)

TFBGA48: plastic thin fine-pitch ball grid array package; 48 balls; body 4.5 x 4.5 x 0.7 mm **SOT1155-2**



Dimensions

Unit	A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
max	1.10	0.30	0.80	0.35	4.6	4.6							
mm nom	0.95	0.25	0.70	0.30	4.5	4.5	0.5	3.5	3.5	0.15	0.05	0.08	0.1
min	0.85	0.20	0.65	0.25	4.4	4.4							

sot1155-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1155-2		- - -				~~13-06-17~~ 13-06-19

Fig 62. Package outline TFBGA48 (SOT1155-2)

Table 34. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	BOD level 0 for reset added in Table 15.			
LPC111X v.7.4	20120730	Product data sheet	-	LPC111X v.7.3
Modifications:	• Function SSEL1 added to pin PIO2_0 in Figure 6 “LPC1100XL series pin configuration HVQFN33” and Table 11 “LPC1100XL series: LPC1111/12/13/14 pin description table (HVQFN33 package)”. • BOD level 0 for reset and interrupt removed.			
LPC111X v.7.3	20120706	Product data sheet	-	LPC111X v.7.2
Modifications:	• Corrected pinout for part LPC1112FHN24/202. Pin XTALOUT replaced by V_{DD}. See Table 6 and Figure 10.			
LPC111X v.7.2	20120604	Product data sheet	-	LPC111X v.7.1
Modifications:	• For parameters I_{OL}, V_{OL}, I_{OH}, V_{OH}, changed conditions to 1.8 V ≤ V_{DD} < 2.5 V and 2.5 V ≤ V_{DD} ≤ 3.6 V in Table 13). • Capture-clear feature added to general-purpose counter/timers (see Section 7.12; LPC1100XL series only). • Figure 47 updated for parts with configurable open-drain mode. • Added Section 9.5 “CoreMark data” • Added LPC1100L series part (LPC1112FHN24/202). • WDOSc frequency range corrected.			
LPC111X v.7.1	20120401	Product data sheet	-	LPC111X v.7
Modifications:	• Added HVQFN33 (5x5) reflow soldering information.			
LPC111X v.7	20120301	Product data sheet	-	LPC1110_11_12_13_14 v.6
Modifications:	• LPC1100XL series parts added (LPC1111FHN33/103, LPC1111FHN33/203, LPC1112FHN33/103, LPC1112FHN33/203, LPC1112FHI33/203, LPC1113FBD48/303, LPC1113FHN33/203, LPC1113FHN33/303, LPC1114FBD48/303, LPC1114FHN33/203, LPC1114FHN33/303, LPC1114FHI33/303, LPC1114FBD48/323, LPC1114FBD48/333, LPC1114FHN33/333, LPC1115FBD48/303).			
LPC1110_11_12_13_14 v.6	20111102	Product data sheet	-	LPC1111_12_13_14 v.5
Modifications:	• Parts LPC1112FHI33/202 and LPC1114FHI33/302 added. • Parts LPC1112FDH28/102, LPC1114FDH28/102, LPC1114FN28/102, LPC1112FDH20/102, LPC1110FD20, LPC1111FDH20/002, LPC1112FD20/102 added.			
LPC1111_12_13_14 v.5	20110622	Product data sheet	-	LPC1111_12_13_14 v.4
Modifications:	• ADC sampling frequency corrected in Table 7 (Table note 7). • Pull-up level specified in Table 3 to Table 4 and Section 7.7.1. • Parameter $T_{cy(clk)}$ corrected on Table 17. • WWDT for parts LPC111x/102/202/302 added in Section 2 and Section 7.15. • Programmable open-drain mode for parts LPC111x/102/202/302 added in Section 2 and Section 7.12. • Condition for parameter T_{stg} in Table 5 updated. • Table note 4 of Table 5 updated. • Section 13 added. • Removed PLCC44 package information.			
LPC1111_12_13_14 v.4	20110210	Product data sheet	-	LPC1111_12_13_14 v.3

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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20. Contents

continued >>