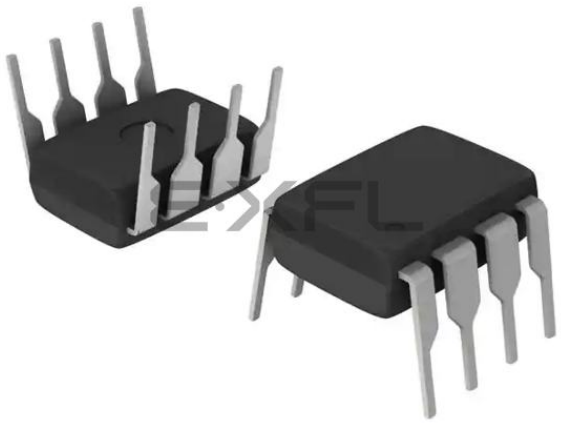

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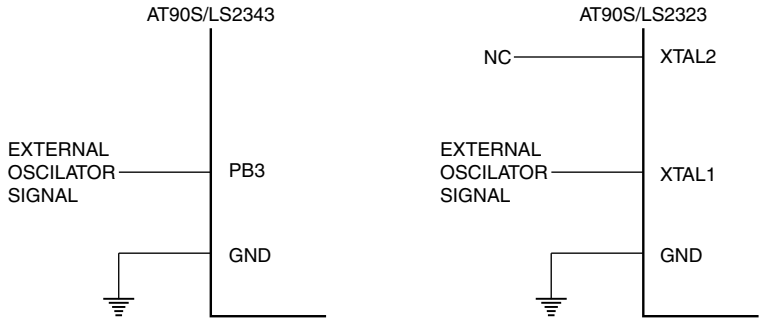
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | AVR |
| Core Size | 8-Bit |
| Speed | 4MHz |
| Connectivity | SPI |
| Peripherals | Brown-out Detect/Reset, POR, WDT |
| Number of I/O | 3 |
| Program Memory Size | 2KB (1K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | 128 x 8 |
| RAM Size | 128 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 6V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C |
| Mounting Type | Through Hole |
| Package / Case | 8-DIP (0.300", 7.62mm) |
| Supplier Device Package | 8-PDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/at90ls2323-4pi |

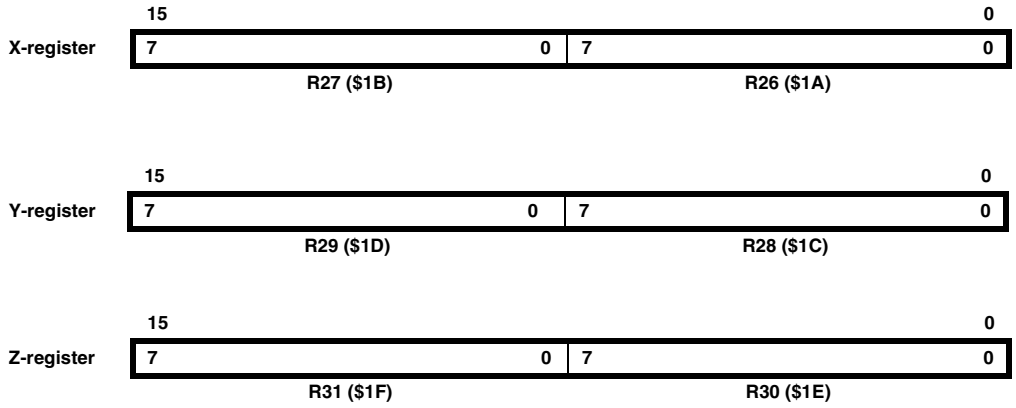
**Figure 4.** External Clock Drive Configuration



### X-register, Y-register and Z-register

The registers R26..R31 have some added functions to their general-purpose usage. These registers are the address pointers for indirect addressing of the Data Space. The three indirect address registers X, Y, and Z, are defined in Figure 8.

**Figure 8.** The X-, Y-, and Z-registers




In the different addressing modes, these address registers have functions as fixed displacement, automatic increment and decrement (see the descriptions for the different instructions).

## ALU – Arithmetic Logic Unit

The high-performance AVR ALU operates in direct connection with all the 32 general-purpose working registers. Within a single clock cycle, ALU operations between registers in the register file are executed. The ALU operations are divided into three main categories: arithmetic, logic and bit functions.

## In-System Programmable Flash Program Memory

The AT90S2323/2343 contains 2K bytes On-chip, In-System Programmable Flash memory for program storage. Since all instructions are 16- or 32-bit words, the Flash is organized as 1K x 16. The Flash memory has an endurance of at least 1000 write/erase cycles.

The AT90S2323/2343 Program Counter (PC) is 10 bits wide, hence addressing the 1024 program memory addresses. See page 42 for a detailed description on Flash data programming.

Constant tables must be allocated within the address 0 - 2K (see the LPM – Load Program Memory instruction description on page 60).

See page 12 for the different addressing modes.

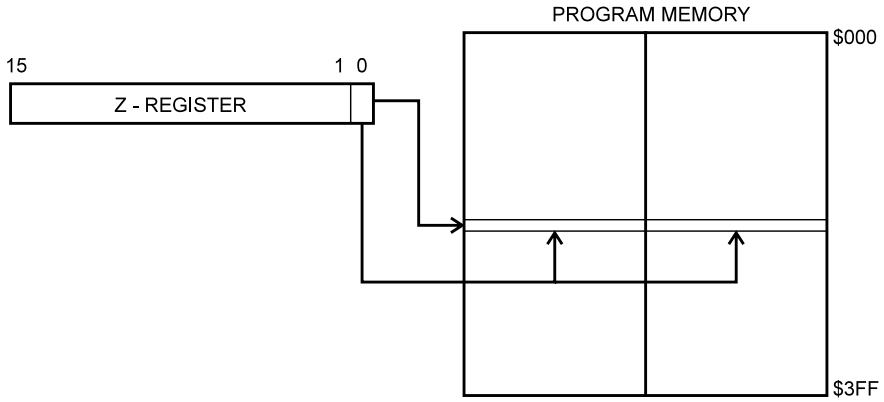
## EEPROM Data Memory

The AT90S2323/2343 contains 128 bytes of EEPROM data memory. It is organized as a separate data space, in which single bytes can be read and written. The EEPROM has an endurance of at least 100,000 write/erase cycles. The access between the EEPROM and the CPU is described on page 32, specifying the EEPROM address register, the EEPROM data register and the EEPROM control register.

For the SPI data downloading, see page 42 for a detailed description.

### Constant Addressing Using the LPM Instruction

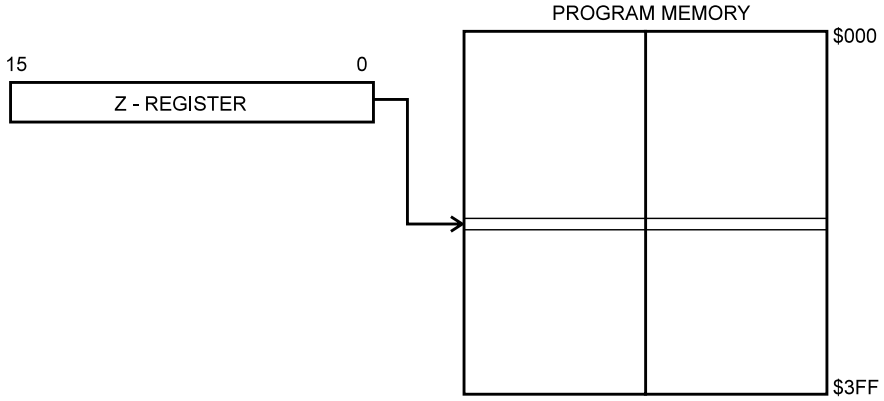
**Figure 18.** Code Memory Constant Addressing




Constant byte address is specified by the Z-register contents. The 15 MSBs select word address (0 - 1K), the LSB selects low byte if cleared (LSB = 0) or high byte if set (LSB = 1).

### Indirect Program Addressing, IJMP and ICALL

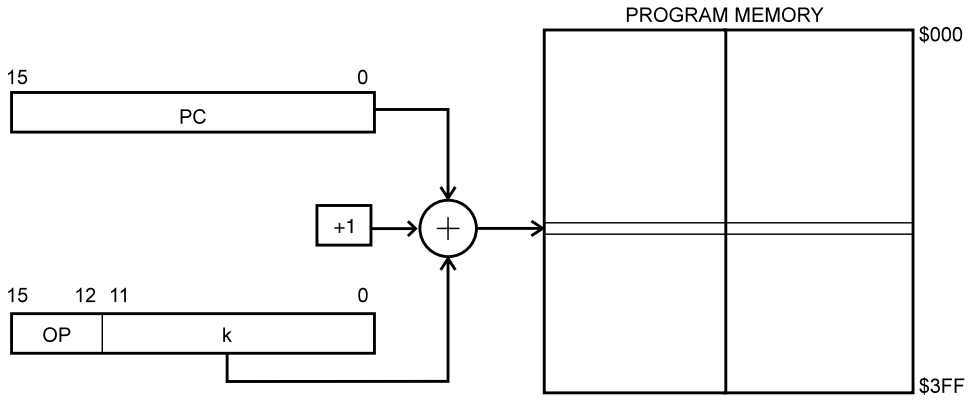
**Figure 19.** Indirect Program Memory Addressing




Program execution continues at address contained by the Z-register (i.e., the PC is loaded with the contents of the Z-register).

### Relative Program Addressing, RJMP and RCALL

**Figure 20.** Relative Program Memory Addressing




Program execution continues at address PC + k + 1. The relative address k is -2048 to 2047.

## Memory Access and Instruction Execution Timing

This section describes the general access timing concepts for instruction execution and internal memory access.

The AVR CPU is driven by the System Clock Ø, directly generated from the external clock signal applied to the CLOCK pin. No internal clock division is used.

Figure 21. shows the parallel instruction fetches and instruction executions enabled by the Harvard architecture and the fast-access register file concept. This is the basic pipelining concept to obtain up to 1 MIPS per MHz with the corresponding unique results for functions per cost, functions per clocks and functions per power unit.

**Figure 21.** The Parallel Instruction Fetches and Instruction Executions

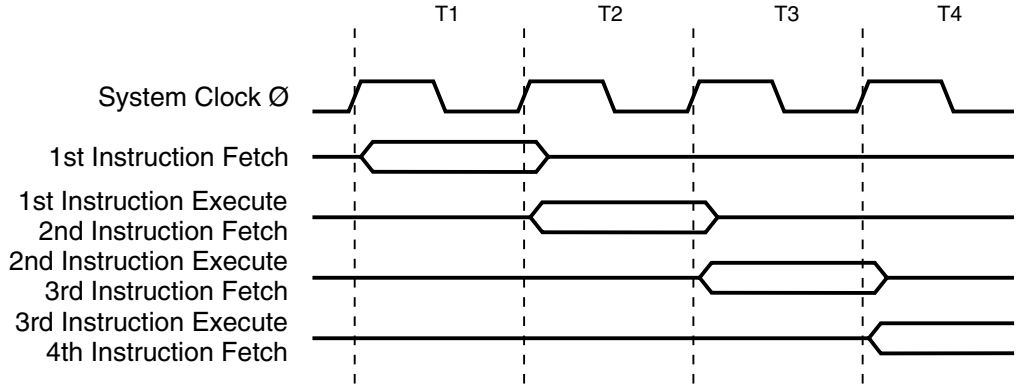
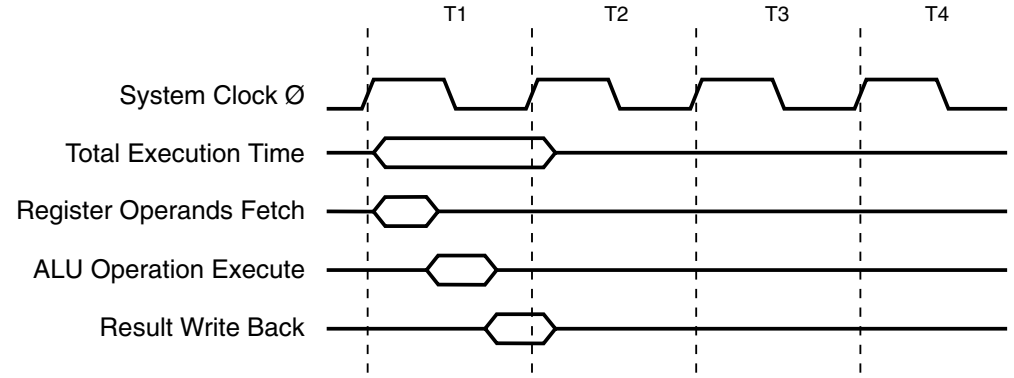



Figure 22. shows the internal timing concept for the register file. In a single clock cycle an ALU operation using two register operands is executed and the result is stored back to the destination register.

**Figure 22.** Single Cycle ALU Operation




The internal data SRAM access is performed in two System Clock cycles as described in Figure 23..

- **Bit 0 – C: Carry Flag**

The carry flag C indicates a carry in an arithmetical or logical operation. See the Instruction Set description for detailed information.

Note that the Status Register is not automatically stored when entering an interrupt routine and restored when returning from an interrupt routine. This must be handled by software.

**Stack Pointer – SPL**

An 8-bit register at I/O address $3D ($5D) forms the stack pointer of the AT90S2323/2343. Eight bits are used to address the 128 bytes of SRAM in locations $60 - $DF.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| $3D ($5D) | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 | SPL |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

The Stack Pointer points to the data SRAM stack area where the Subroutine and Interrupt stacks are located. This stack space in the data SRAM must be defined by the program before any subroutine calls are executed or interrupts are enabled. The Stack Pointer must be set to point above $60. The Stack Pointer is decremented by 1 when data is pushed onto the Stack with the PUSH instruction and it is decremented by 2 when an address is pushed onto the stack with subroutine calls and interrupts. The Stack Pointer is incremented by 1 when data is popped from the stack with the POP instruction and it is incremented by 2 when an address is popped from the stack with return from subroutine RET or return from interrupt RETI.

## Reset and Interrupt Handling

The AT90S2323/2343 provides two interrupt sources. These interrupts and the separate reset vector each have a separate program vector in the program memory space. Both interrupts are assigned individual enable bits that must be set (one) together with the I-bit in the Status Register in order to enable the interrupt.

The lowest addresses in the program memory space are automatically defined as the Reset and Interrupt vectors. The complete list of vectors is shown in Table 3. The list also determines the priority levels of the interrupts. The lower the address, the higher the priority level. RESET has the highest priority, and next is INT0 (the External Interrupt Request 0), etc.

**Table 3.** Reset and Interrupt Vectors

| Vector No. | Program Address | Source | Interrupt Definition |
|---|---|---|---|
| 1 | $000 | RESET | Hardware Pin, Power-on Reset and Watchdog Reset |
| 2 | $001 | INT0 | External Interrupt Request 0 |
| 3 | $002 | TIMER0, OVF0 | Timer/Counter0 Overflow |

The most typical program setup for the Reset and Interrupt vector addresses are:

```
Address     Labels      Code                    Comments
$000                    rjmp RESET              ; Reset Handler
$001                    rjmp EXT_INT0           ; IRQ0 Handler
$002                    rjmp TIM_OVF0           ; Timer0 Overflow
                                                ; Handler;
$003        MAIN:       ldi r16, low(RAMEND)    ; Main program start
                        out SPL, r16
                        <instr> xxx
...         ...         ...                     ...
```

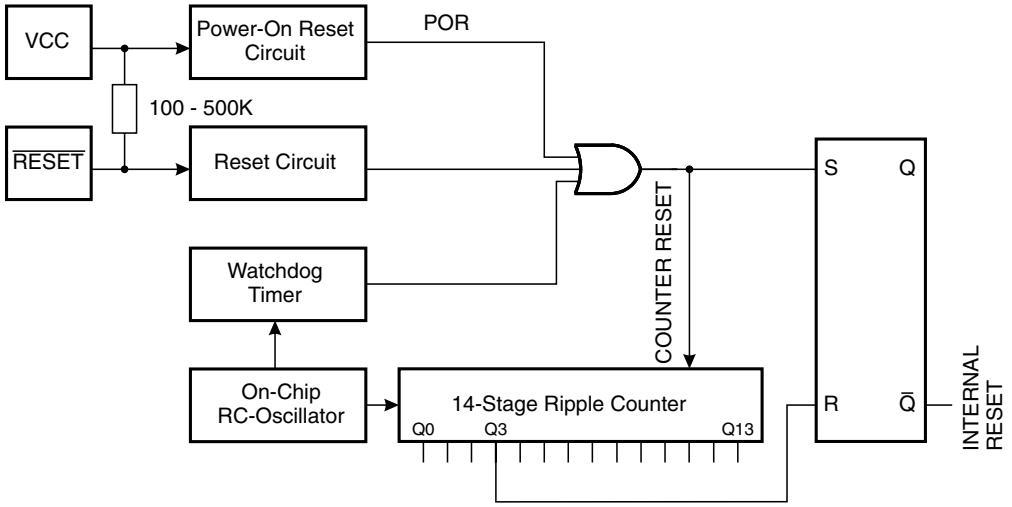
## Reset Sources

The AT90S2323/2343 provides three sources of reset:

- Power-on Reset. The MCU is reset when the supply voltage is below the Power-on Reset threshold ($V_{POT}$).
- External Reset. The MCU is reset when a low level is present on the $\overline{\text{RESET}}$ pin for more than 50 ns.
- Watchdog Reset. The MCU is reset when the Watchdog timer period expires and the Watchdog is enabled.

During reset, all I/O registers are set to their initial values and the program starts execution from address $000. The instruction placed in address $000 must be an RJMP (relative jump) instruction to the reset handling routine. If the program never enables an interrupt source, the interrupt vectors are not used and regular program code can be placed at these locations. The circuit diagram in Figure 24 shows the reset logic. Table 4 defines the timing and electrical parameters of the reset circuitry.

**Figure 24.** Reset Logic




The AT90S/LS2323 has a programmable start-up time. A fuse bit (FSTRT) in the Flash memory selects the shortest start-up time when programmed (“0”). The AT90S/LS2323 is shipped with this bit unprogrammed.

The AT90S/LS2343 has a fixed start-up time.

activate the interrupt are defined in Table 9. The value on the INT01 pin is sampled before detecting edges. If edge or toggle interrupt is selected, pulses that last longer than one clock period will generate an interrupt. Shorter pulses are not guaranteed to generate an interrupt. If low-level interrupt is selected, the low level must be held until the completion of the currently executing instruction to generate an interrupt.

**Table 9.** Interrupt 0 Sense Control

| ISC01 | ISC00 | Description |
|---|---|---|
| 0 | 0 | The low level of INT0 generates an interrupt request. |
| 0 | 1 | Reserved |
| 1 | 0 | The falling edge of INT0 generates an interrupt request. |
| 1 | 1 | The rising edge of INT0 generates an interrupt request. |

## Sleep Modes

To enter the sleep modes, the SE bit in MCUCR must be set (one) and a SLEEP instruction must be executed. If an enabled interrupt occurs while the MCU is in a sleep mode, the MCU awakes, executes the interrupt routine and resumes execution from the instruction following SLEEP. The contents of the register file, SRAM and I/O memory are unaltered. If a reset occurs during Sleep mode, the MCU wakes up and executes from the Reset vector.

### Idle Mode

When the SM bit is cleared (zero), the SLEEP instruction forces the MCU into the Idle mode, stopping the CPU but allowing Timer/Counters, Watchdog and the interrupt system to continue operating. This enables the MCU to wake up from external triggered interrupts as well as internal ones like Timer Overflow interrupt and Watchdog reset.

### Power-down Mode

When the SM bit is set (one), the SLEEP instruction forces the MCU into the Power-down mode. In this mode, the external oscillator is stopped while the external interrupts and the Watchdog (if enabled) continue operating. Only an external reset, a Watchdog reset (if enabled), or an external level interrupt on INT0 can wake up the MCU.

Note that if a level-triggered interrupt is used for wake-up from Power-down mode, the changed level must be held for some time to wake up the MCU. This makes the MCU less sensitive to noise. The changed level is sampled twice by the Watchdog oscillator clock and if the input has the required level during this time, the MCU will wake up. The period of the Watchdog oscillator is 1 µs (nominal) at 5.0V and 25°C. The frequency of the Watchdog oscillator is voltage-dependent as shown in section “Typical Characteristics” on page 49.

When waking up from Power-down mode, a delay from the wake-up condition occurs until the wake-up becomes effective. This allows the clock to restart and become stable after having been stopped. The wake-up period is equal to the clock reset period, as shown in Table 4 and Table 5 on page 21.

If the wake-up condition disappears before the MCU wakes up and starts to execute, e.g., a low-level on is not held long enough, the interrupt causing the wake-up will not be executed.

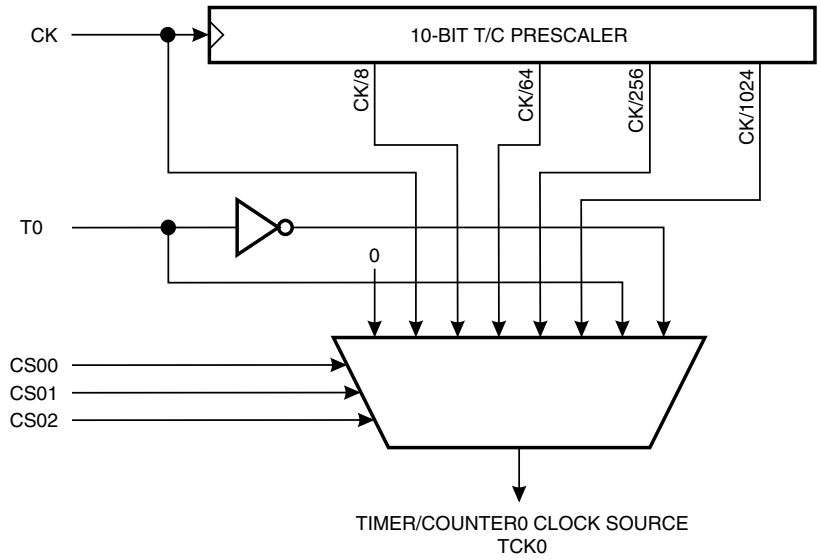
## Timer/Counter

The AT90S2323/2343 provides one general-purpose 8-bit Timer/Counter – Timer/Counter0. The Timer/Counter has prescaling selection from the 10-bit prescaling timer. The Timer/Counter can be used either as a timer with an internal clock time base or as a counter with an external pin connection that triggers the counting.

## Timer/Counter Prescaler

Figure 29 shows the Timer/Counter prescaler.

**Figure 29.** Timer/Counter0 Prescaler




The four different prescaled selections are: CK/8, CK/64, CK/256 and CK/1024, where CK is the oscillator clock. CK, external source and stop can also be selected as clock sources.

## 8-bit Timer/Counter0

Figure 30 shows the block diagram for Timer/Counter0.

The 8-bit Timer/Counter0 can select clock source from CK, prescaled CK or an external pin. In addition, it can be stopped as described in the specification for the Timer/Counter0 Control Register (TCCR0). The overflow status flag is found in the Timer/Counter Interrupt Flag Register (TIFR). Control signals are found in the Timer/Counter0 Control Register (TCCR0). The interrupt enable/disable settings for Timer/Counter0 are found in the Timer/Counter Interrupt Mask Register (TIMSK).

When Timer/Counter0 is externally clocked, the external signal is synchronized with the oscillator frequency of the CPU. To ensure proper sampling of the external clock, the minimum time between two external clock transitions must be at least one internal CPU clock period. The external clock signal is sampled on the rising edge of the internal CPU clock.

The 8-bit Timer/Counter0 features both a high-resolution and a high-accuracy usage with the lower prescaling opportunities. Similarly, the high prescaling opportunities make the Timer/Counter0 useful for lower speed functions or exact timing functions with infrequent actions.

## EEPROM Read/Write Access

The EEPROM access registers are accessible in the I/O space.

The write access time is in the range of 2.5 - 4 ms, depending on the $V_{CC}$ voltages. A self-timing function, however, lets the user software detect when the next byte can be written.

In order to prevent unintentional EEPROM writes, a specific write procedure must be followed. Refer to the description of the EEPROM Control Register for details on this.

When the EEPROM is written, the CPU is halted for two clock cycles before the next instruction is executed. When the EEPROM is read, the CPU is halted for four clock cycles before the next instruction is executed.

### EEPROM Address Register – EEAR

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| $1E ($3E) | – | EEAR6 | EEAR5 | EEAR4 | EEAR3 | EEAR2 | EEAR1 | EEAR0 | EEAR |
| Read/Write | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

- **Bit 7 – Res: Reserved Bit**

This bit is a reserved bit in the AT90S2323/2343 and will always read as zero.

- **Bit 6..0 – EEAR6..0: EEPROM Address**

The EEPROM Address Register (EEAR6..0) specifies the EEPROM address in the 128-byte EEPROM space. The EEPROM data bytes are addressed linearly between 0 and 127.

### EEPROM Data Register – EEDR

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| $1D ($3D) | MSB | | | | | | | LSB | EEDR |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

- **Bits 7..0 – EEDR7..0: EEPROM Data**

For the EEPROM write operation, the EEDR register contains the data to be written to the EEPROM in the address given by the EEAR register. For the EEPROM read operation, the EEDR contains the data read out from the EEPROM at the address given by EEAR.

# Memory Programming

## Program and Data Memory Lock Bits

The AT90S2323/2343 MCU provides two Lock bits that can be left unprogrammed (“1”) or can be programmed (“0”) to obtain the additional features listed in Table 14. The Lock bits can only be erased with the Chip Erase operation.

**Table 14.** Lock Bit Protection Modes

| Memory Lock Bits | | | |
|---|---|---|---|
| **Mode** | **LB1** | **LB2** | **Protection Type** |
| 1 | 1 | 1 | No memory lock features enabled. |
| 2 | 0 | 1 | Further programming of the Flash and EEPROM is disabled.(1) |
| 3 | 0 | 0 | Same as mode 2, and verify is also disabled. |

Note: 1. In the high-voltage Serial Programming mode, further programming of the Fuse bits are also disabled. Program the Fuse bits before programming the Lock bits.

## Fuse Bits in AT90S/LS2323

The AT90S/LS2323 has two Fuse bits, SPIEN and FSTRT.

- When the SPIEN Fuse is programmed (“0”), Serial Program and Data Downloading are enabled. Default value is programmed (“0”). This bit is not accessible in the low-voltage Serial Programming mode.
- When the FSTRT Fuse is programmed (“0”), the shortest start-up time is selected as indicated in Table 6 on page 21. Default value is programmed (“0”). Changing the FSTRT Fuse does not take effect until the next Power-on Reset. In AT90S/LS2343 the start-up time is fixed.

The status of the Fuse bits is not affected by Chip Erase.

## Fuse Bits in AT90S/LS2343

The AT90S/LS2343 has two Fuse bits, SPIEN and RCEN.

- When the SPIEN Fuse is programmed (“0”), Serial Program and Data Downloading are enabled. Default value is programmed (“0”). This bit is not accessible in the low-voltage Serial Programming mode.
- When the RCEN Fuse is programmed (“0”), the internal RC oscillator is selected as the MCU clock source. Default value is programmed ("0") in AT90LS2343-1. Default value is un-programmed ("1") in AT90LS2343-4 and AT90S2343-10. Changing the RCEN Fuse does not take effect until the next Power-on Reset. AT90S/LS2323 cannot select the internal RC oscillator as the MCU source.

The status of the Fuse bits is not affected by Chip Erase.

## Signature Bytes

All Atmel microcontrollers have a three-byte signature code that identifies the device. The three bytes reside in a separate address space.

For the AT90S/LS2323(Note:), they are:

1. $000: $1E (indicates manufactured by Atmel)
2. $001: $91 (indicates 2K bytes Flash memory)
3. $002: $02 (indicates AT90S/LS2323 when signature byte $001 is $91)

For AT90S/LS2343(Note:), they are:

1. $000: $1E (indicates manufactured by Atmel)
2. $001: $91 (indicates 2K bytes Flash memory)

## High-voltage Serial Programming Characteristics

**Figure 34.** High-voltage Serial Programming Timing

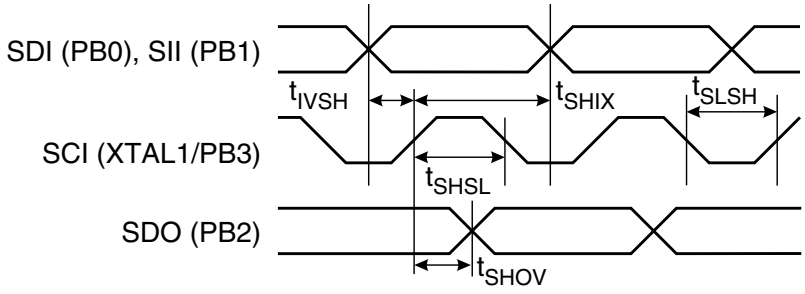


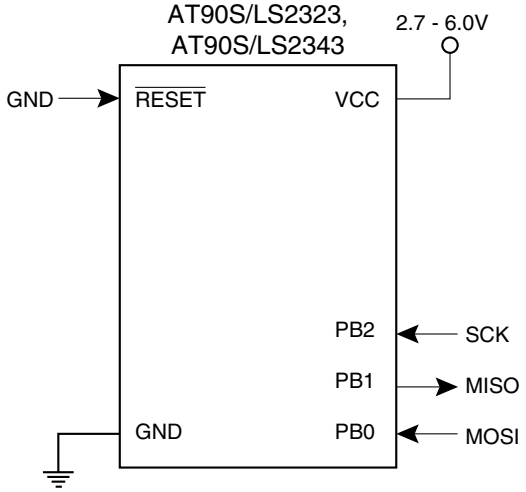

**Table 17.** High-voltage Serial Programming Characteristics, $T_A$ = 25°C ± 10%, $V_{CC}$ = 5.0V ± 10% (unless otherwise noted)

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $t_{SHSL}$ | SCI (XTAL1/PB3) Pulse Width High | 100.0 | | | ns |
| $t_{SLSH}$ | SCI (XTAL1/PB3) Pulse Width Low | 100.0 | | | ns |
| $t_{IVSH}$ | SDI (PB0), SII (PB1) Valid to SCI (XTAL1/PB3) High | 50.0 | | | ns |
| $t_{SHIX}$ | SDI (PB0), SII (PB1) Hold after SCI (XTAL1/PB3) High | 50.0 | | | ns |
| $t_{SHOV}$ | SCI (XTAL1/PB3) High to SDO (PB2) Valid | 10.0 | 16.0 | 32.0 | ns |
| $t_{WLWH\_CE}$ | Wait after Instr.3 for Chip Erase | 5.0 | 10.0 | 15.0 | ms |
| $t_{WLWH\_PFB}$ | Wait after Instr.3 for Write Fuse Bits | 1.0 | 1.5 | 1.8 | ms |

## Low-voltage Serial Downloading

Both the program and data memory arrays can be programmed using the serial SPI bus while $\overline{\text{RESET}}$ is pulled to GND. The serial interface consists of pins SCK, MOSI (input) and MISO (output) (see Figure 35). After $\overline{\text{RESET}}$ is set low, the Programming Enable instruction needs to be executed first before program/erase instructions can be executed.

**Figure 35.** Low-voltage Serial Programming and Verify



For the EEPROM, an auto-erase cycle is provided within the self-timed Write instruction and there is no need to first execute the Chip Erase instruction. The Chip Erase instruction turns the content of every memory location in both the program and EEPROM arrays into $FF.

The program and EEPROM memory arrays have separate address spaces: $0000 to $03FF for Flash program memory and $000 to $07F for EEPROM data memory.

Either an external clock is applied to the XTAL1/PB3 pin or the device must be clocked from the internal RC oscillator (AT90S/LS2343 only). The minimum low and high periods for the serial clock (SCK) input are defined as follows:

Low: > 2 MCU clock cycles

High: > 2 MCU clock cycles

**Low-voltage Serial Programming Algorithm**

When writing serial data to the AT90S2323/2343, data is clocked on the rising edge of SCK.

When reading data from the AT90S2323/2343, data is clocked on the falling edge of SCK. See Figure 36, Figure 37 and Table 20 for timing details.

To program and verify the AT90S2323/2343 in the low-voltage Serial Programming mode, the following sequence is recommended (see 4-byte instruction formats in Table 19):

1. Power-up sequence:

   Apply power between $V_{CC}$ and GND while RESET and SCK are set to “0”. (If the programmer cannot guarantee that SCK is held low during power-up, RESET must be given a positive pulse after SCK has been set to “0”.) If the device is programmed for external clocking, apply a 0 - 8 MHz clock to the XTAL1/PB3 pin. If the internal RC oscillator is selected as the clock source, no external clock source needs to be applied (AT90S/LS2343 only).
2. Wait for at least 20 ms and enable serial programming by sending the Programming Enable serial instruction to the MOSI (PB0) pin. Refer to the above section for minimum low and high periods for the serial clock input, SCK.
3. The serial programming instructions will not work if the communication is out of synchronization. When in sync, the second byte ($53) will echo back when issuing the third byte of the Programming Enable instruction. Whether the echo is correct or not, all four bytes of the instruction must be transmitted. If the $53 did not echo back, give SCK a positive pulse and issue a new Programming Enable instruction. If the $53 is not seen within 32 attempts, there is no functional device connected.
4. If a Chip Erase is performed (must be done to erase the Flash), wait $t_{WD\_ERASE}$ after the instruction, give $\overline{\text{RESET}}$ a positive pulse and start over from step 2. See Table 21 on page 46 for $t_{WD\_ERASE}$ value.
5. The Flash or EEPROM array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. An EEPROM memory location is first automatically erased before new data is written. Use Data Polling to detect when the next byte in the Flash or EEPROM can be written. If polling is not used, wait $t_{WD\_PROG}$ before transmitting the next instruction. See Table 22 on page 46 for $t_{WD\_PROG}$ value. In an erased device, no $FFs in the data file(s) need to be programmed.
6. Any memory location can be verified by using the Read instruction, which returns the content at the selected address at the serial output MISO (PB1) pin.

7. At the end of the programming session, $\overline{\text{RESET}}$ can be set high to commence normal operation.
8. Power-off sequence (if needed):

   Set CLOCK/XTAL1 to “0”.

   Set $\overline{\text{RESET}}$ to “1”.

   Turn $V_{CC}$ power off.

**Data Polling EEPROM**

When a byte is being programmed into the EEPROM, reading the address location being programmed will give the value P1 until the auto-erase is finished, and then the value P2 will be given. See Table 18 for P1 and P2 values.

At the time the device is ready for a new EEPROM byte, the programmed value will read correctly. This is used to determine when the next byte can be written. This will not work for the values P1 and P2, so when programming these values, the user will have to wait for at least the prescribed time $t_{WD\_PROG}$ before programming the next byte. See Table 22 for $t_{WD\_PROG}$ value. As a chip-erased device contains $FF in all locations, programming of addresses that are meant to contain $FF can be skipped. This does not apply if the EEPROM is reprogrammed without first chip-erasing the device.

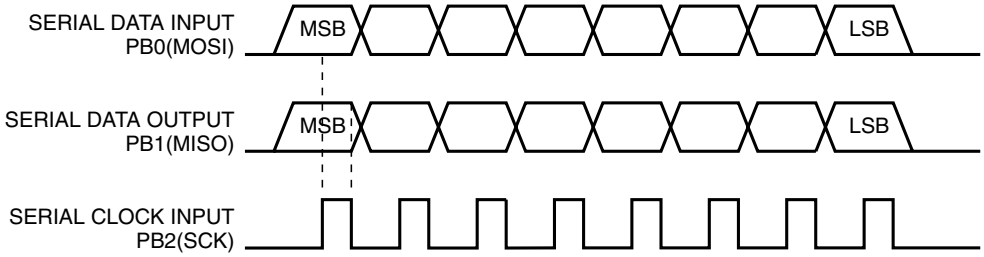
**Table 18.** Read Back Value during EEPROM Polling

| Part | P1 | P2 |
|---|---|---|
| AT90S2323 | $00 | $FF |
| AT90S2343 | $00 | $FF |

**Data Polling Flash**

When a byte is being programmed into the Flash, reading the address location being programmed will give the value $FF. At the time the device is ready for a new byte, the programmed value will read correctly. This is used to determine when the next byte can be written. This will not work for the value $FF, so when programming this value, the user will have to wait for at least $t_{WD\_PROG}$ before programming the next byte. As a chip-erased device contains $FF in all locations, programming of addresses that are meant to contain $FF can be skipped.

**Figure 36.** Low-voltage Serial Downloading Waveforms



## Low-voltage Serial Programming Characteristics

**Figure 37.** Low-voltage Serial Programming Timing

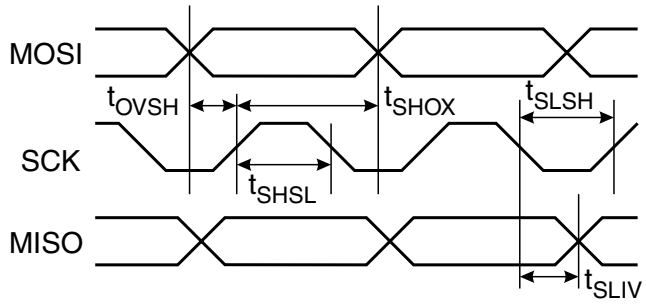



**Table 20.** Low-voltage Serial Programming Characteristics, $T_A$ = -40°C to 85°C, $V_{CC}$ = 2.7 - 6.0V (unless otherwise noted)

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $1/t_{CLCL}$ | Oscillator Frequency ($V_{CC}$ = 2.7 - 4.0V) | 0 | | 4.0 | MHz |
| $t_{CLCL}$ | Oscillator Period ($V_{CC}$ = 2.7 - 4.0V) | 250.0 | | | ns |
| $1/t_{CLCL}$ | Oscillator Frequency ($V_{CC}$ = 4.0 - 6.0V) | 0 | | 8.0 | MHz |
| $t_{CLCL}$ | Oscillator Period ($V_{CC}$ = 4.0 - 6.0V) | 125.0 | | | ns |
| $t_{SHSL}$ | SCK Pulse Width High | 2.0 $t_{CLCL}$ | | | ns |
| $t_{SLSH}$ | SCK Pulse Width Low | 2.0 $t_{CLCL}$ | | | ns |
| $t_{OVSH}$ | MOSI Setup to SCK High | $t_{CLCL}$ | | | ns |
| $t_{SHOX}$ | MOSI Hold after SCK High | 2.0 $t_{CLCL}$ | | | ns |
| $t_{SLIV}$ | SCK Low to MISO Valid | 10.0 | 16.0 | 32.0 | ns |

**Table 21.** Minimum Wait Delay after the Chip Erase Instruction

| Symbol | 3.2V | 3.6V | 4.0V | 5.0V |
|---|---|---|---|---|
| $t_{WD\_ERASE}$ | 18 ms | 14 ms | 12 ms | 8 ms |

**Table 22.** Minimum Wait Delay after Writing a Flash or EEPROM Location

| Symbol | 3.2V | 3.6V | 4.0V | 5.0V |
|---|---|---|---|---|
| $t_{WD\_PROG}$ | 9 ms | 7 ms | 6 ms | 4 ms |

# Electrical Characteristics

## Absolute Maximum Ratings*

| | |
|---|---|
| Operating Temperature | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on Any Pin except $\overline{\text{RESET}}$ with respect to Ground | -1.0V to $V_{CC}$ + 0.5V |
| Voltage on $\overline{\text{RESET}}$ with Respect to Ground | -1.0V to +13.0V |
| Maximum Operating Voltage | 6.6V |
| DC Current per I/O Pin | 40.0 mA |
| DC Current $V_{CC}$ and GND Pins | 200.0 mA |

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC Characteristics

$T_A$ = -40°C to 85°C, $V_{CC}$ = 2.7V to 6.0V (unless otherwise noted)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | (Except XTAL) | -0.5 | | 0.3 $V_{CC}$(1) | V |
| $V_{IL1}$ | Input Low Voltage | XTAL | -0.5 | | 0.1(1) | V |
| $V_{IH}$ | Input High Voltage | (Except XTAL, $\overline{\text{RESET}}$) | 0.6 $V_{CC}$(2) | | $V_{CC}$ + 0.5 | V |
| $V_{IH1}$ | Input High Voltage | XTAL | 0.7 $V_{CC}$(2) | | $V_{CC}$ + 0.5 | V |
| $V_{IH2}$ | Input High Voltage | RESET | 0.85 $V_{CC}$(2) | | $V_{CC}$ + 0.5 | V |
| $V_{OL}$ | Output Low Voltage Ports B | $I_{OL}$ = 20 mA, $V_{CC}$ = 5V<br>$I_{OL}$ = 10 mA, $V_{CC}$ = 3V | | | 0.5<br>0.4 | V<br>V |
| $V_{OH}$ | Output High Voltage Ports B | $I_{OH}$ = -3 mA, $V_{CC}$ = 5V<br>$I_{OH}$ = -1.5 mA, $V_{CC}$ = 3V | 4.2<br>2.4 | | | V<br>V |
| $I_{IL}$ | Input Leakage Current I/O Pin | $V_{CC}$ = 6V, Pin Low (absolute value) | | | 8.0 | µA |
| $I_{IH}$ | Input Leakage Current I/O Pin | $V_{CC}$ = 6V, Pin High (absolute value) | | | 8.0 | µA |
| RRST | Reset Pull-up | | 100.0 | | 500.0 | kΩ |
| $R_{I/O}$ | I/O Pin Pull-up | | 30.0 | | 150.0 | kΩ |
| $I_{CC}$ | Power Supply Current AT90S2343 | Active 4 MHz, $V_{CC}$ = 3V | | | 3.0 | mA |
| | | Idle 4 MHz, $V_{CC}$ = 3V | | | 1.1 | mA |
| | | Power-down 4 MHz(3), $V_{CC}$ = 3V WDT Enabled | | | 25.0 | µA |
| | | Power-down 4 MHz(3), $V_{CC}$ = 3V WDT Disabled | | | 20.0 | µA |
| | Power Supply Current AT90S2323 | Active 4 MHz, $V_{CC}$ = 3V | | | 4.0 | mA |
| | | Idle 4 MHz, $V_{CC}$ = 3V | | 1.0 | 1.2 | mA |
| | | Power-down(3), $V_{CC}$ = 3V WDT Enabled | | 9.0 | 15.0 | µA |
| | | Power-down(3), $V_{CC}$ = 3V WDT Disabled | | <1.0 | 2.0 | µA |

Notes: 1. "Max" means the highest value where the pin is guaranteed to be read as low.
2. "Min" means the lowest value where the pin is guaranteed to be read as high.
3. Minimum $V_{CC}$ for Power-down is 2V.

**Figure 54.** I/O Pin Input Threshold Voltage vs. $V_{CC}$

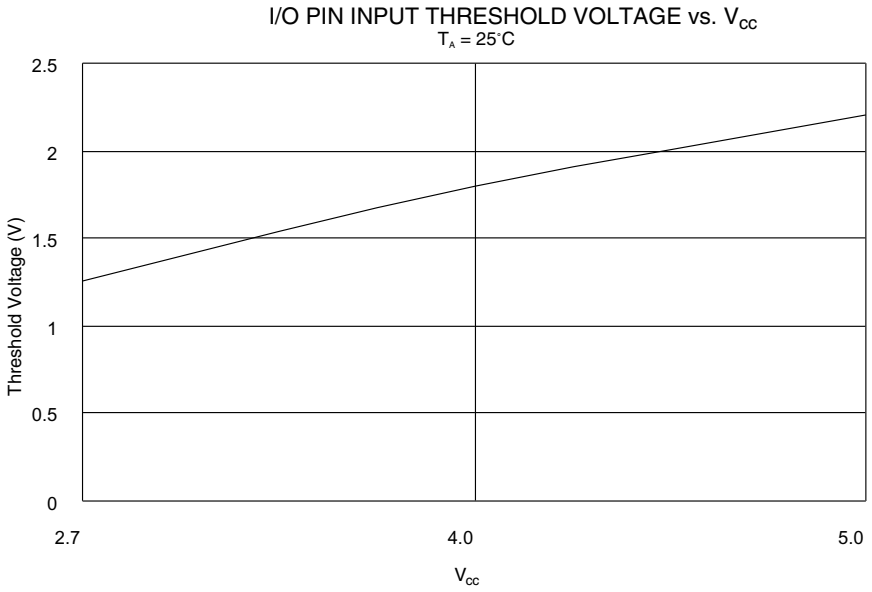
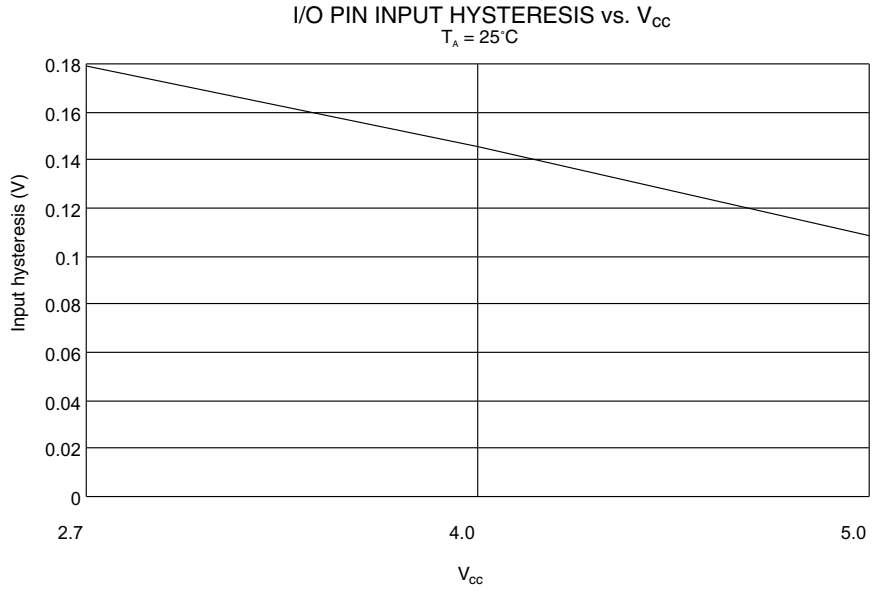



**Figure 55.** I/O Pin Input Hysteresis vs. $V_{CC}$



## AT90S2323/2343 Register Summary

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|---|---|---|---|---|---|---|---|---|---|---|
| $3F ($5F) | SREG | I | T | H | S | V | N | Z | C | page 18 |
| $3E ($5E) | Reserved | | | | | | | | | |
| $3D ($5D) | SPL | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 | page 19 |
| $3C ($5C) | Reserved | | | | | | | | | |
| $3B ($5B) | GIMSK | - | INT0 | - | - | - | - | - | - | page 24 |
| $3A ($5A) | GIFR | - | INTF0 | | | | | | | page 25 |
| $39 ($59) | TIMSK | - | - | - | - | - | - | TOIE0 | - | page 25 |
| $38 ($58) | TIFR | - | - | - | - | - | - | TOV0 | - | page 25 |
| $37 ($57) | Reserved | | | | | | | | | |
| $36 ($56) | Reserved | | | | | | | | | |
| $35 ($55) | MCUCR | - | - | SE | SM | - | - | ISC01 | ISC00 | page 26 |
| $34 ($54) | MCUSR | - | - | - | - | - | - | EXTRF | PORF | page 23 |
| $33 ($53) | TCCR0 | - | - | - | - | - | CS02 | CS01 | CS00 | page 29 |
| $32 ($52) | TCNT0 | Timer/Counter0 (8 Bits) | | | | | | | | page 30 |
| $31 ($51) | Reserved | | | | | | | | | |
| $30 ($50) | Reserved | | | | | | | | | |
| $2F ($4F) | Reserved | | | | | | | | | |
| $2E ($4E) | Reserved | | | | | | | | | |
| $2D ($4D) | Reserved | | | | | | | | | |
| $2C ($4C) | Reserved | | | | | | | | | |
| $2B ($4B) | Reserved | | | | | | | | | |
| $2A ($4A) | Reserved | | | | | | | | | |
| $29 ($49) | Reserved | | | | | | | | | |
| $28 ($48) | Reserved | | | | | | | | | |
| $27 ($47) | Reserved | | | | | | | | | |
| $26 ($46) | Reserved | | | | | | | | | |
| $25 ($45) | Reserved | | | | | | | | | |
| $24 ($44) | Reserved | | | | | | | | | |
| $23 ($43) | Reserved | | | | | | | | | |
| $22 ($42) | Reserved | | | | | | | | | |
| $21 ($41) | WDTCR | - | - | - | WDTOE | WDE | WDP2 | WDP1 | WDP0 | page 31 |
| $20 ($40) | Reserved | | | | | | | | | |
| $1F ($3F) | Reserved | | | | | | | | | |
| $1E ($3E) | EEAR | - | EEPROM Address Register | | | | | | | page 32 |
| $1D ($3D) | EEDR | EEPROM Data Register | | | | | | | | page 32 |
| $1C ($3C) | EECR | - | - | - | - | - | EEMWE | EEWE | EERE | page 33 |
| $1B ($3B) | Reserved | | | | | | | | | |
| $1A ($3A) | Reserved | | | | | | | | | |
| $19 ($39) | Reserved | | | | | | | | | |
| $18 ($38) | PORTB | - | - | - | PORTB4 | PORTB3 | PORTB2 | PORTB1 | PORTB0 | page 35 |
| $17 ($37) | DDRB | - | - | - | DDB4 | DDB3 | DDB2 | DDB1 | DDB0 | page 35 |
| $16 ($36) | PINB | - | - | - | PINB4 | PINB3 | PINB2 | PINB1 | PINB0 | page 36 |
| $15 ($35) | Reserved | | | | | | | | | |
| … | Reserved | | | | | | | | | |
| $00 ($20) | Reserved | | | | | | | | | |

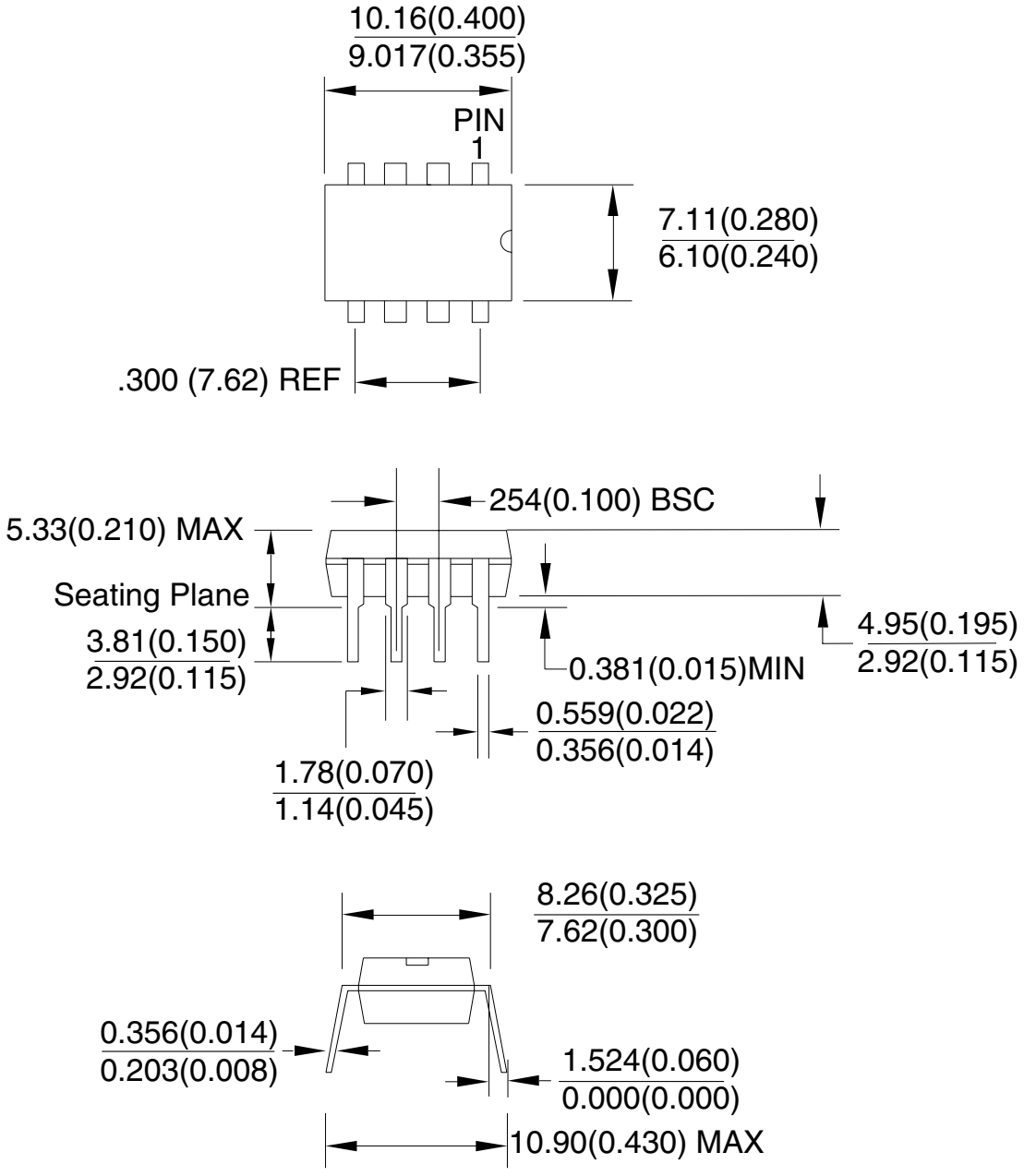
Note: 1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

2. Some of the status flags are cleared by writing a logical “1” to them. Note that the CBI and SBI instructions will operate on all bits in the I/O register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers $00 to $1F only.

## Packaging Information

### 8P3

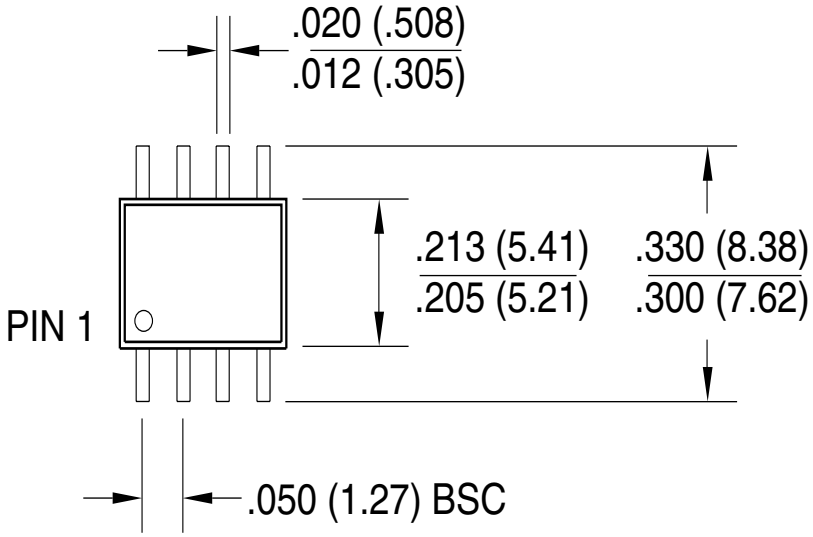
8P3, 8-lead, Plastic Dual Inline
Package (PDIP), 0.300" Wide.
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-001 BA

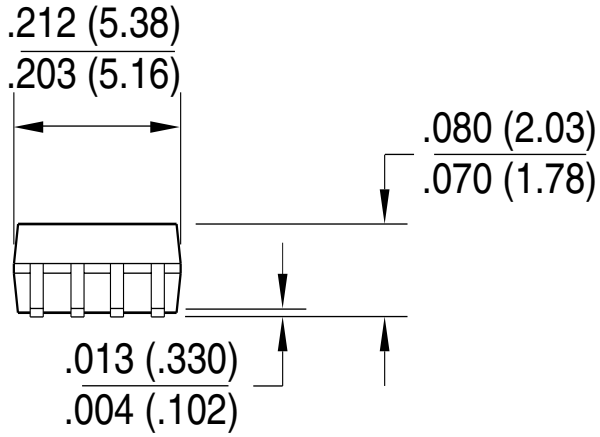


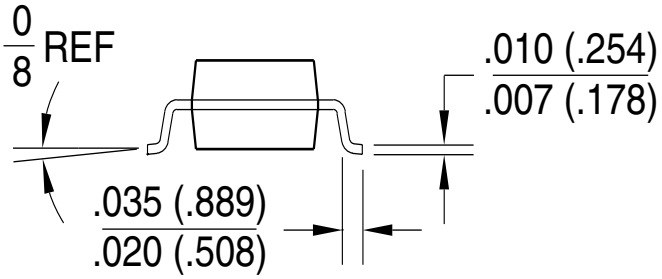

*Controlling dimension: Inches

REV. A 04/11/2001

**8S2**


.020 (.508)
.012 (.305)
.213 (5.41)
.205 (5.21)
.330 (8.38)
.300 (7.62)
PIN 1
.050 (1.27) BSC


.212 (5.38)
.203 (5.16)
.080 (2.03)
.070 (1.78)
.013 (.330)
.004 (.102)


0
8
REF
.010 (.254)
.007 (.178)
.035 (.889)
.020 (.508)

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