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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	121
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 15x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/ppc5605bclq64

Figure 2 shows the MPC5607B in the 176 LQFP package.

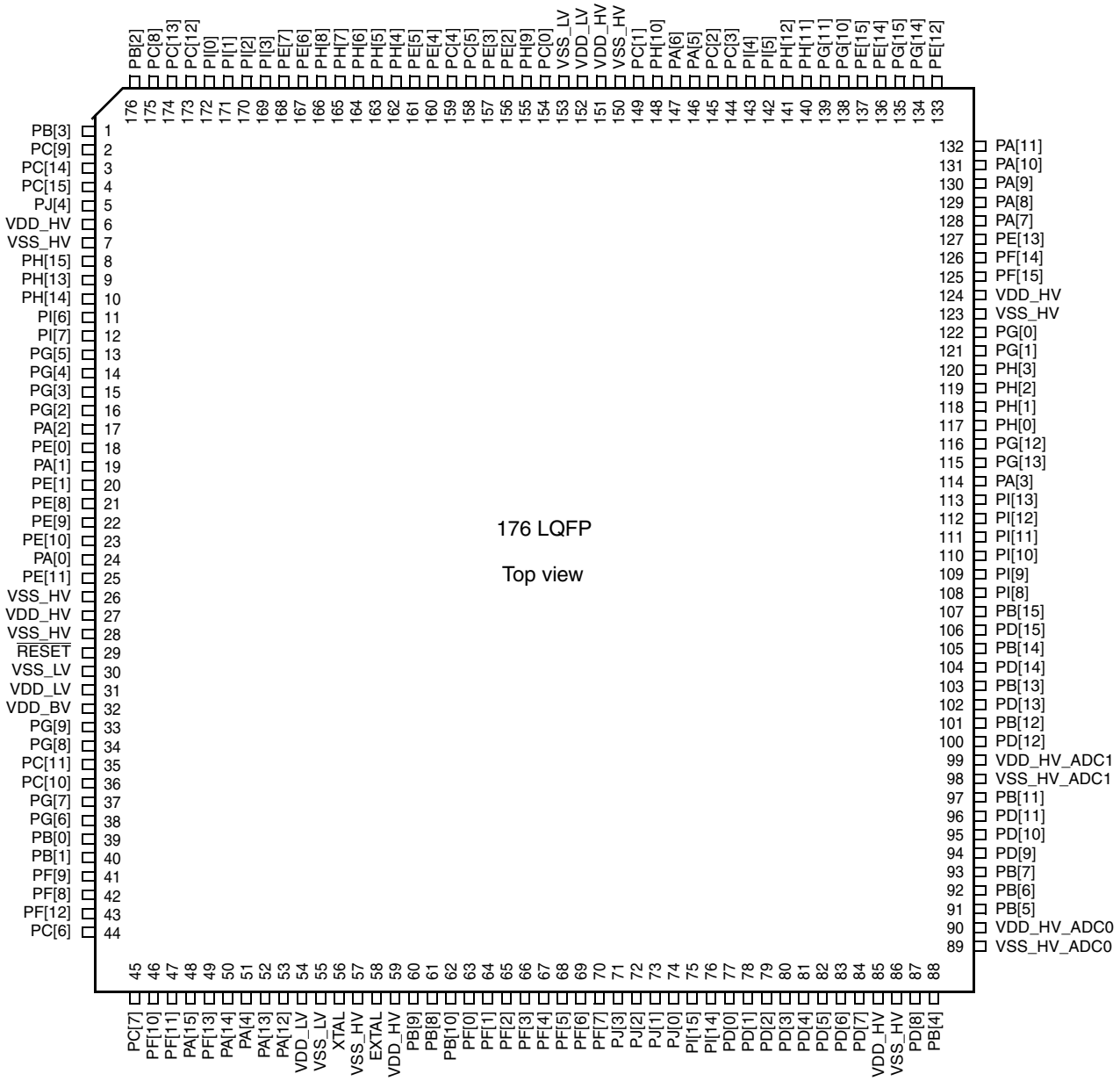


Figure 2. 176 LQFP pin configuration

Figure 4 shows the MPC5607B in the 100 LQFP package.

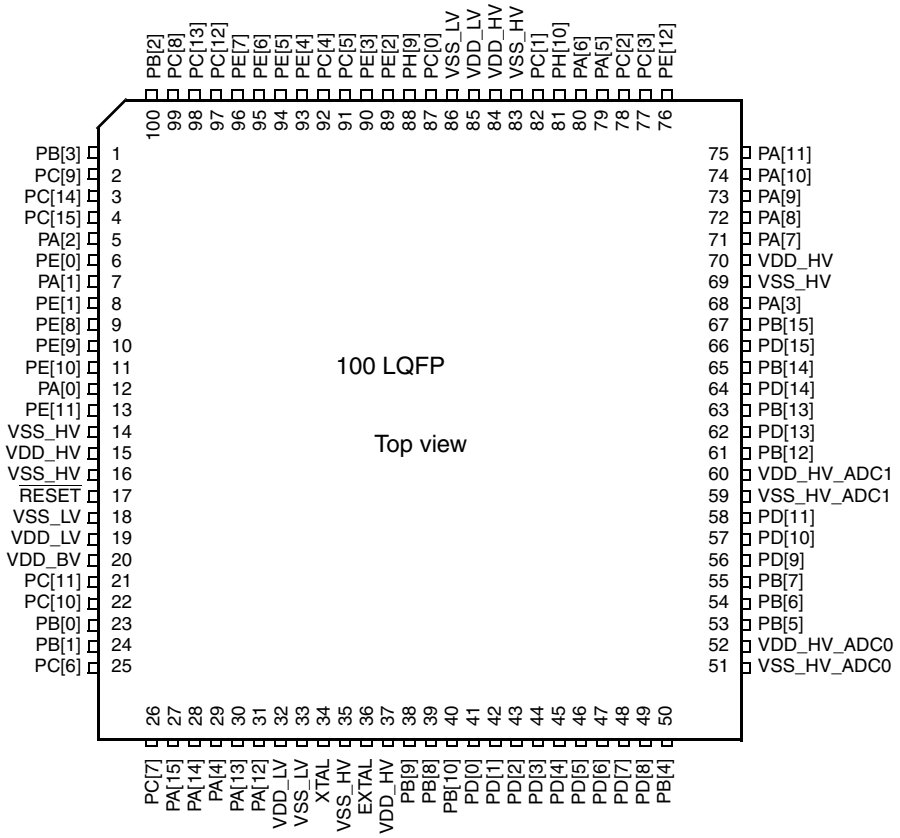


Figure 4. 100 LQFP pin configuration

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								100 LQFP	144 LQFP	176 LQFP	208 MAP BGA[4]
PB[5]	PCR[21]	AF0 AF1 AF2 AF3 — — —	— — — — ADC0_P[1] ADC1_P[1] GPIO[21]	— — — — ADC_0 ADC_1 SIUL	— — — — I I I	I	Tristate	53	75	91	R16
PB[6]	PCR[22]	AF0 AF1 AF2 AF3 — — —	— — — — ADC0_P[2] ADC1_P[2] GPIO[22]	— — — — ADC_0 ADC_1 SIUL	— — — — I I I	I	Tristate	54	76	92	P15
PB[7]	PCR[23]	AF0 AF1 AF2 AF3 — — —	— — — — ADC0_P[3] ADC1_P[3] GPIO[23]	— — — — ADC_0 ADC_1 SIUL	— — — — I I I	I	Tristate	55	77	93	P16
PB[8]	PCR[24]	AF0 AF1 AF2 AF3 — — — —	GPIO[24] — — — OSC32K_XTAL[8] WKPU[25][5] ADC0_S[0] ADC1_S[4]	SIUL — — — OSC32K WKPU ADC_0 ADC_1	I — — — — I[9] I I	I	—	39	53	61	R9
PB[9]	PCR[25]	AF0 AF1 AF2 AF3 — — — —	GPIO[25] — — — OSC32K_EXTAL[8] WKPU[26][5] ADC0_S[1] ADC1_S[5]	SIUL — — — OSC32K WKPU ADC_0 ADC_1	I — — — — I[9] I I	I	—	38	52	60	T9
PB[10]	PCR[26]	AF0 AF1 AF2 AF3 — — —	GPIO[26] — — — WKPU[8][5] ADC0_S[2] ADC1_S[6]	SIUL — — — WKPU ADC_0 ADC_1	I/O — — — I I I	J	Tristate	40	54	62	P9

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								100 LQFP	144 LQFP	176 LQFP	208 MAP BGA[4]
PG[0]	PCR[96]	AF0 AF1 AF2 AF3	GPIO[96] CAN5TX E1UC[23] —	SIUL FlexCAN_5 eMIOS_1 —	I/O O I/O —	M	Tristate	—	98	122	E14
PG[1]	PCR[97]	AF0 AF1 AF2 AF3 — —	GPIO[97] — E1UC[24] — EIRQ[14] CAN5RX	SIUL — eMIOS_1 — SIUL FlexCAN_5	I/O — I/O — I I	S	Tristate	—	97	121	E13
PG[2]	PCR[98]	AF0 AF1 AF2 AF3	GPIO[98] E1UC[11] SOUT_3 —	SIUL eMIOS_1 DSPI_3 —	I/O I/O O —	M	Tristate	—	8	16	E4
PG[3]	PCR[99]	AF0 AF1 AF2 AF3 —	GPIO[99] E1UC[12] CS0_3 — WKPU[17][5]	SIUL eMIOS_1 DSPI_3 — WKPU	I/O I/O I/O — I	S	Tristate	—	7	15	E3
PG[4]	PCR[100]	AF0 AF1 AF2 AF3	GPIO[100] E1UC[13] SCK_3 —	SIUL eMIOS_1 DSPI_3 —	I/O I/O I/O —	M	Tristate	—	6	14	E1
PG[5]	PCR[101]	AF0 AF1 AF2 AF3 — —	GPIO[101] E1UC[14] — — WKPU[18][5] SIN_3	SIUL eMIOS_1 — — WKPU DSPI_3	I/O I/O — — I I	S	Tristate	—	5	13	E2
PG[6]	PCR[102]	AF0 AF1 AF2 AF3	GPIO[102] E1UC[15] LIN6TX —	SIUL eMIOS_1 LINFlex_6 —	I/O I/O O —	M	Tristate	—	30	38	M2
PG[7]	PCR[103]	AF0 AF1 AF2 AF3 — —	GPIO[103] E1UC[16] E1UC[30] — WKPU[20][5] LIN6RX	SIUL eMIOS_1 eMIOS_1 — WKPU LINFlex_6	I/O I/O I/O — I I	S	Tristate	—	29	37	M1

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								100 LQFP	144 LQFP	176 LQFP	208 MAP BGA[4]
PG[8]	PCR[104]	AF0 AF1 AF2 AF3 —	GPIO[104] E1UC[17] LIN7TX CS0_2 EIRQ[15]	SIUL eMIOS_1 LINFlex_7 DSPI_2 SIUL	I/O I/O O I/O I	S	Tristate	—	26	34	L2
PG[9]	PCR[105]	AF0 AF1 AF2 AF3 — —	GPIO[105] E1UC[18] — SCK_2 WKPU[21][5] LIN7RX	SIUL eMIOS_1 — DSPI_2 WKPU LINFlex_7	I/O I/O — I/O I I	S	Tristate	—	25	33	L1
PG[10]	PCR[106]	AF0 AF1 AF2 AF3 —	GPIO[106] E0UC[24] E1UC[31] — SIN_4	SIUL eMIOS_0 eMIOS_1 — DSPI_4	I/O I/O I/O — I	S	Tristate	—	114	138	D13
PG[11]	PCR[107]	AF0 AF1 AF2 AF3	GPIO[107] E0UC[25] CS0_4 —	SIUL eMIOS_0 DSPI_4 —	I/O I/O I/O —	M	Tristate	—	115	139	B12
PG[12]	PCR[108]	AF0 AF1 AF2 AF3	GPIO[108] E0UC[26] SOUT_4 —	SIUL eMIOS_0 DSPI_4 —	I/O I/O O —	M	Tristate	—	92	116	K14
PG[13]	PCR[109]	AF0 AF1 AF2 AF3	GPIO[109] E0UC[27] SCK_4 —	SIUL eMIOS_0 DSPI_4 —	I/O I/O I/O —	M	Tristate	—	91	115	K16
PG[14]	PCR[110]	AF0 AF1 AF2 AF3	GPIO[110] E1UC[0] LIN8TX —	SIUL eMIOS_1 LINFlex_8 —	I/O I/O O —	S	Tristate	—	110	134	B14
PG[15]	PCR[111]	AF0 AF1 AF2 AF3 —	GPIO[111] E1UC[1] — — LIN8RX	SIUL eMIOS_1 — — LINFlex_8	I/O I/O — — I	M	Tristate	—	111	135	B13
Port H											
PH[0]	PCR[112]	AF0 AF1 AF2 AF3 —	GPIO[112] E1UC[2] — — SIN_1	SIUL eMIOS_1 — — DSPI_1	I/O I/O — — I	M	Tristate	—	93	117	F13

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								100 LQFP	144 LQFP	176 LQFP	208 MAP BGA[4]
PH[11]	PCR[123]	AF0 AF1 AF2 AF3	GPIO[123] SOUT_3 CS0_4 E1UC[5]	SIUL DSPI_3 DSPI_4 eMIOS_1	I/O O I/O I/O	M	Tristate	—	—	140	A14
PH[12]	PCR[124]	AF0 AF1 AF2 AF3	GPIO[124] SCK_3 CS1_4 E1UC[25]	SIUL DSPI_3 DSPI_4 eMIOS_1	I/O I/O O I/O	M	Tristate	—	—	141	D12
PH[13]	PCR[125]	AF0 AF1 AF2 AF3	GPIO[125] SOUT_4 CS0_3 E1UC[26]	SIUL DSPI_4 DSPI_3 eMIOS_1	I/O O I/O I/O	M	Tristate	—	—	9	B3
PH[14]	PCR[126]	AF0 AF1 AF2 AF3	GPIO[126] SCK_4 CS1_3 E1UC[27]	SIUL DSPI_4 DSPI_3 eMIOS_1	I/O I/O O I/O	M	Tristate	—	—	10	D1
PH[15]	PCR[127]	AF0 AF1 AF2 AF3	GPIO[127] SOUT_5 — E1UC[17]	SIUL DSPI_5 — eMIOS_1	I/O O — I/O	M	Tristate	—	—	8	A3
Port I											
PI[0]	PCR[128]	AF0 AF1 AF2 AF3	GPIO[128] E0UC[28] LIN8TX —	SIUL eMIOS_0 LINFlex_8 —	I/O I/O O —	S	Tristate	—	—	172	A9
PI[1]	PCR[129]	AF0 AF1 AF2 AF3 — —	GPIO[129] E0UC[29] — — WKPU[24][5] LIN8RX	SIUL eMIOS_0 — — WKPU LINFlex_8	I/O I/O — — I I	S	Tristate	—	—	171	A10
PI[2]	PCR[130]	AF0 AF1 AF2 AF3	GPIO[130] E0UC[30] LIN9TX —	SIUL eMIOS_0 LINFlex_9 —	I/O I/O O —	S	Tristate	—	—	170	B10
PI[3]	PCR[131]	AF0 AF1 AF2 AF3 — —	GPIO[131] E0UC[31] — — WKPU[23][5] LIN9RX	SIUL eMIOS_0 — — WKPU LINFlex_9	I/O I/O — — I I	S	Tristate	—	—	169	C10

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								100 LQFP	144 LQFP	176 LQFP	208 MAP BGA[4]
PI[13]	PCR[141]	AF0 AF1 AF2 AF3 —	GPIO[141] CS1_3 — — ADC0_S[21]	SIUL DSPI_3 — — ADC_0	I/O O — — I	J	Tristate	—	—	113	G15
PI[14]	PCR[142]	AF0 AF1 AF2 AF3 — —	GPIO[142] — — — ADC0_S[22] SIN_4	SIUL — — — ADC_0 DSPI_4	I/O — — — I I	J	Tristate	—	—	76	R8
PI[15]	PCR[143]	AF0 AF1 AF2 AF3 —	GPIO[143] CS0_4 — — ADC0_S[23]	SIUL DSPI_4 — — ADC_0	I/O I/O — — I	J	Tristate	—	—	75	T8
Port J											
PJ[0]	PCR[144]	AF0 AF1 AF2 AF3 —	GPIO[144] CS1_4 — — ADC0_S[24]	SIUL DSPI_4 — — ADC_0	I/O O — — I	J	Tristate	—	—	74	N5
PJ[1]	PCR[145]	AF0 AF1 AF2 AF3 — —	GPIO[145] — — — ADC0_S[25] SIN_5	SIUL — — —— ADC_0 DSPI_5	I/O — — — I I	J	Tristate	—	—	73	P5
PJ[2]	PCR[146]	AF0 AF1 AF2 AF3 —	GPIO[146] CS0_5 — — ADC0_S[26]	SIUL DSPI_5 — — ADC_0	I/O I/O — — I	J	Tristate	—	—	72	P4
PJ[3]	PCR[147]	AF0 AF1 AF2 AF3 —	GPIO[147] CS1_5 — — ADC0_S[27]	SIUL DSPI_5 — — ADC_0	I/O O — — I	J	Tristate	—	—	71	P2
PJ[4]	PCR[148]	AF0 AF1 AF2 AF3	GPIO[148] SCK_5 E1UC[18] —	SIUL DSPI_5 eMIOS_1 —	I/O I/O I/O —	M	Tristate	—	—	5	A4

Table 11. Absolute maximum ratings (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pins with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_ADC}	SR	Voltage on VDD_HV_ADC0, VDD_HV_ADC1 (ADC reference) pins with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	V_{DD} – 0.3	V_{DD} + 0.3	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	—	V_{DD} + 0.3	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
I_{AVGSEG}	SR	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	70	mA
			V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	64	
$T_{STORAGE}$	SR	Storage temperature	—	–55	150	°C

NOTE

Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.

4.4 Recommended operating conditions

Table 12. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}[1]	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	3.0	3.6	V
V_{SS_LV}[2]	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_BV}[3]	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	3.0	3.6	V
			Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	

Table 23. I/O weight[1] (continued)

Supply segment			Pad	176 LQFP				144/100 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
176 LQFP	144 LQFP	100 LQFP		SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
2	1	—	PG[9]	9%	—	10%	—	9%	—	10%	—
		—	PG[8]	9%	—	11%	—	9%	—	11%	—
		1	PC[11]	9%	—	11%	—	9%	—	11%	—
			PC[10]	9%	13%	11%	12%	9%	13%	11%	12%
		—	PG[7]	9%	—	11%	—	9%	—	11%	—
		—	PG[6]	10%	14%	11%	12%	10%	14%	11%	12%
		1	PB[0]	10%	14%	12%	12%	10%	14%	12%	12%
			PB[1]	10%	—	12%	—	10%	—	12%	—
		—	PF[9]	10%	—	12%	—	10%	—	12%	—
		—	PF[8]	10%	14%	12%	13%	10%	14%	12%	13%
		—	PF[12]	10%	15%	12%	13%	10%	15%	12%	13%
		1	PC[6]	10%	—	12%	—	10%	—	12%	—
			PC[7]	10%	—	12%	—	10%	—	12%	—
		—	PF[10]	10%	14%	11%	12%	10%	14%	11%	12%
		—	PF[11]	9%	—	11%	—	9%	—	11%	—
		1	PA[15]	8%	12%	10%	10%	8%	12%	10%	10%
		—	PF[13]	8%	—	10%	—	8%	—	10%	—
		1	PA[14]	8%	11%	9%	10%	8%	11%	9%	10%
			PA[4]	7%	—	9%	—	7%	—	9%	—
			PA[13]	7%	10%	8%	9%	7%	10%	8%	9%
			PA[12]	7%	—	8%	—	7%	—	8%	—

Table 23. I/O weight[1] (continued)

Supply segment			Pad	176 LQFP				144/100 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
176 LQFP	144 LQFP	100 LQFP		SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
6	4	4	PC[0]	6%	9%	7%	8%	7%	10%	8%	8%
			PH[9]	7%	—	8%	—	7%	—	9%	—
			PE[2]	7%	10%	8%	9%	8%	11%	9%	10%
			PE[3]	7%	10%	9%	9%	8%	12%	10%	10%
			PC[5]	7%	11%	9%	9%	8%	12%	10%	11%
			PC[4]	8%	11%	9%	10%	9%	13%	10%	11%
			PE[4]	8%	11%	9%	10%	9%	13%	11%	12%
			PE[5]	8%	11%	10%	10%	9%	14%	11%	12%
		—	PH[4]	8%	12%	10%	10%	10%	14%	12%	12%
		—	PH[5]	8%	—	10%	—	10%	—	12%	—
		—	PH[6]	8%	12%	10%	11%	10%	15%	12%	13%
		—	PH[7]	9%	12%	10%	11%	11%	15%	13%	13%
		—	PH[8]	9%	12%	10%	11%	11%	16%	13%	14%
		4	PE[6]	9%	12%	10%	11%	11%	16%	13%	14%
			PE[7]	9%	12%	10%	11%	11%	16%	14%	14%
	—	—	PI[3]	9%	—	10%	—	—	—	—	—
	—	—	PI[2]	9%	—	10%	—	—	—	—	—
	—	—	PI[1]	9%	—	10%	—	—	—	—	—
	—	—	PI[0]	9%	—	10%	—	—	—	—	—
	4	4	PC[12]	8%	12%	10%	11%	12%	18%	15%	16%
			PC[13]	8%	—	10%	—	13%	—	15%	—
			PC[8]	8%	—	10%	—	13%	—	15%	—
			PB[2]	8%	11%	9%	10%	13%	18%	15%	16%

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 SRC: “Slew Rate Control” bit in SIU_PCRx

Table 26. Low voltage detector electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{PORUP}	SR	P	Supply for functional POR module	T_A = 25 °C, after trimming	1.0	—	5.5	V
V_{PORH}	CC	P	Power-on reset threshold		1.5	—	2.6	
$V_{LVDHV3H}$	CC	T	LVDHV3 low voltage detector high threshold		—	—	2.95	
$V_{LVDHV3L}$	CC	P	LVDHV3 low voltage detector low threshold		2.7	—	2.9	
$V_{LVDHV3BH}$	CC	P	LVDHV3B low voltage detector high threshold		—	—	2.95	
$V_{LVDHV3BL}$	CC	P	LVDHV3B low voltage detector low threshold		2.7	—	2.9	
$V_{LVDHV5H}$	CC	T	LVDHV5 low voltage detector high threshold		—	—	4.5	
$V_{LVDHV5L}$	CC	P	LVDHV5 low voltage detector low threshold		3.8	—	4.4	
$V_{LVDLVCORL}$	CC	P	LVDLVCOR low voltage detector low threshold		1.08	—	1.16	
$V_{LVDLVBKPL}$	CC	P	LVDLVBKP low voltage detector low threshold		1.08	—	1.16	

[1] V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

4.9 Power consumption

Table 27 provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

Table 27. Power consumption on VDD_BV and VDD_HV

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{DDMAX}[2]	CC	D	RUN mode maximum average current	—		—	115	140[3]	mA
I_{DDRUN}[4]	CC	T	RUN mode typical average current[5]	f_{CPU} = 8 MHz		—	12	—	mA
		T		f_{CPU} = 16 MHz		—	27	—	
		T		f_{CPU} = 32 MHz		—	43	—	
		P		f_{CPU} = 48 MHz		—	56	100	
		P		f_{CPU} = 64 MHz		—	70	125	
I_{DDHALT}	CC	C	HALT mode current[6]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	10	18	mA
		P			T_A = 125 °C	—	17	28	
I_{DDSTOP}	CC	P	STOP mode current[7]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	350	900[8]	µA
		D			T_A = 55 °C	—	750	—	
		D			T_A = 85 °C	—	2	7	mA
		D			T_A = 105 °C	—	4	10	
		P			T_A = 125 °C	—	7	14	

Table 27. Power consumption on VDD_BV and VDD_HV (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
$I_{DDSTDBY2}$	CC	P	STANDBY2 mode current[9]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	30	100	µA
		D			T_A = 55 °C	—	75	—	
		D			T_A = 85 °C	—	180	700	
		D			T_A = 105 °C	—	315	1000	
		P			T_A = 125 °C	—	560	1700	
$I_{DDSTDBY1}$	CC	T	STANDBY1 mode current[10]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	20	60	µA
		D			T_A = 55 °C	—	45	—	
		D			T_A = 85 °C	—	100	350	
		D			T_A = 105 °C	—	165	500	
		D			T_A = 125 °C	—	280	900	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 Running consumption does not include I/Os toggling which is highly dependent on the application. The given value is thought to be a worst case value with all peripherals running, and code fetched from code flash while modify operation ongoing on data flash. Notice that this value can be significantly reduced by application: switch off not used peripherals (default), reduce peripheral frequency through internal prescaler, fetch from RAM most used functions, use low power mode when possible.

3 Higher current may be sunk by device during power-up and standby exit. Please refer to in-rush average current in Table 25.

4 RUN current measured with typical application with accesses on both Flash and RAM.

5 Only for the “P” classification: Data and Code Flash in Normal Power. Code fetched from RAM: Serial IPs CAN and LIN in loop back mode, DSPI as Master, PLL as system clock (4 x Multiplier) peripherals on (eMIOS/CTU/ADC) and running at max frequency, periodic SW/WDG timer reset enabled.

6 Data Flash Power Down. Code Flash in Low Power. SIRC 128 kHz and FIRC 16 MHz on. 10 MHz XTAL clock. FlexCAN: instances: 0, 1, 2 ON (clocked but not reception or transmission), instances: 4, 5, 6 clocks gated. LINFlex: instances: 0, 1, 2 ON (clocked but not reception or transmission), instance: 3 to 9 clocks gated. eMIOS: instance: 0 ON (16 channels on PA[0]–PA[11] and PC[12]–PC[15]) with PWM 20 kHz, instance: 1 clock gated. DSPI: instance: 0 (clocked but no communication), instance: 1 to 5 clocks gated. RTC/API ON. PIT ON. STM ON. ADC1 OFF. ADC0 ON but no conversion except two analog watchdogs.

7 Only for the “P” classification: No clock, FIRC 16 MHz off, SIRC 128 kHz on, PLL off, HPvreg off, ULPVreg/LPVreg on. All possible peripherals off and clock gated. Flash in power down mode.

8 When going from RUN to STOP mode and the core consumption is > 6 mA, it is normal operation for the main regulator module to be kept on by the on-chip current monitoring circuit. This is most likely to occur with junction temperatures exceeding 125 °C and under these circumstances, it is possible for the current to initially exceed the maximum STOP specification by up to 2 mA. After entering stop, the application junction temperature will reduce to the ambient level and the main regulator will be automatically switched off when the load current is below 6 mA.

9 Only for the “P” classification: ULPreg on, HP/LPVreg off, 32 KB RAM on, device configured for minimum consumption, all possible modules switched off.

10 ULPreg on, HP/LPVreg off, 8 KB RAM on, device configured for minimum consumption, all possible modules switched off.

Table 34. ESD absolute maximum ratings[1,2]

Symbol	Ratings	Conditions	Class	Max value[3]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500	
				750 (corners)	

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

3 Data based on characterization results, not tested in production

4.11.3.2 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 35. Latch-up results

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

4.12 Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

The device provides an oscillator/resonator driver. Figure 11 describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

Table 36 provides the parameter description of 4 MHz to 16 MHz crystals used for the design simulations.

Table 37. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics (continued)

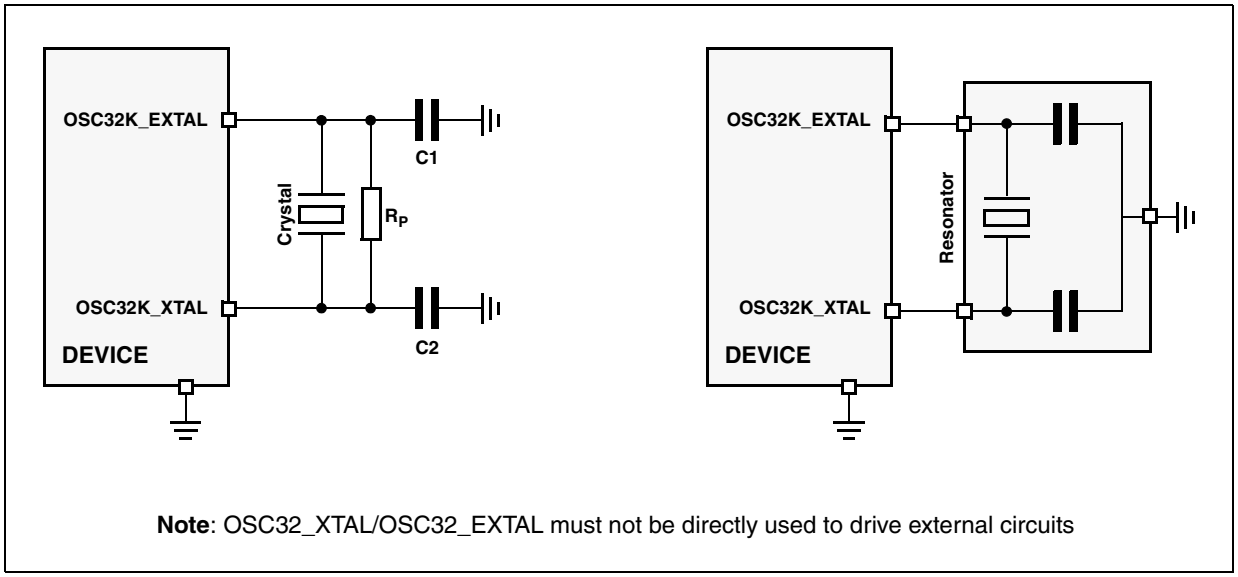
Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
$t_{FXOSCSU}$	CC	T	Fast external crystal oscillator start-up time	f_{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0	—	—	6	ms
				f_{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1	—	—	1.8	
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	Oscillator bypass mode	$0.65V_{DD}$	—	V_{DD} + 0.4	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	Oscillator bypass mode	–0.4	—	$0.35V_{DD}$	V

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 Stated values take into account only analog module consumption but not the digital contributor (clock tree and enabled peripherals).

4.13 Slow external crystal oscillator (32 kHz) electrical characteristics

The device provides a low power oscillator/resonator driver.



Note: OSC32_XTAL/OSC32_EXTAL must not be directly used to drive external circuits

Figure 13. Crystal oscillator and resonator connection scheme

Table 44. ADC_0 conversion characteristics (10-bit ADC_0) (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
R_{SW1}	CC	D	Internal resistance of analog source	—		—	—	3	kΩ
R_{SW2}	CC	D	Internal resistance of analog source	—		—	—	2	kΩ
R_{AD}	CC	D	Internal resistance of analog source	—		—	—	2	kΩ
I_{INJ}	SR	—	Input current Injection	Current injection on one ADC_0 input, different from the converted one	V_{DD} = 3.3 V ± 10%	–5	—	5	mA
					V_{DD} = 5.0 V ± 10%	–5	—	5	
| INL |	CC	T	Absolute integral nonlinearity	No overload		—	0.5	1.5	LSB
| DNL |	CC	T	Absolute differential nonlinearity	No overload		—	0.5	1.0	LSB
| E_O |	CC	T	Absolute offset error	—		—	0.5	—	LSB
| E_G |	CC	T	Absolute gain error	—		—	0.6	—	LSB
TUEP	CC	P	Total unadjusted error[7] for precise channels, input only pins	Without current injection		–2	0.6	2	LSB
		T		With current injection		–3	—	3	
TUEX	CC	T	Total unadjusted error[7] for extended channel	Without current injection		–3	1	3	LSB
		T		With current injection		–4		4	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 Analog and digital V_{SS} **must** be common (to be tied together externally).

3 V_{AINx} may exceed V_{SS_ADC0} and V_{DD_ADC0} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF.

4 Duty cycle is ensured by using system clock without prescaling. When ADCLKSEL = 0, the duty cycle is ensured by internal divider by 2.

5 During the sampling time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC0_S}. After the end of the sampling time t_{ADC0_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sampling clock t_{ADC0_S} depend on programming.

6 This parameter does not include the sampling time t_{ADC0_S}, but only the time for determining the digital result and the time to load the result's register with the conversion result.

7 Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

Table 47. DSPI characteristics[1] (continued)

No.	Symbol		C	Parameter		DSPI0/DSPI1/DSPI5/DSPI6			DSPI2/DSPI4			Unit
						Min	Typ	Max	Min	Typ	Max	
9	t_{SUI}	SR	D	Data setup time for inputs	Master mode	43	—	—	145	—	—	ns
					Slave mode	5	—	—	5	—	—	
10	t_{HI}	SR	D	Data hold time for inputs	Master mode	0	—	—	0	—	—	ns
					Slave mode	2[6]	—	—	2[6]	—	—	
11	t_{SUO}[7]	CC	D	Data valid after SCK edge	Master mode	—	—	32	—	—	50	ns
					Slave mode	—	—	52	—	—	160	
12	t_{HO}[7]	CC	D	Data hold time for outputs	Master mode	0	—	—	0	—	—	ns
					Slave mode	8	—	—	13	—	—	

1 Operating conditions: C_L = 10 to 50 pF, $Slew_{IN}$ = 3.5 to 15 ns

2 Maximum value is reached when CSn pad is configured as SLOW pad while SCK pad is configured as MEDIUM. A positive value means that SCK starts before CSn is asserted. DSPI2 has only SLOW SCK available.

3 Maximum value is reached when CSn pad is configured as MEDIUM pad while SCK pad is configured as SLOW. A positive value means that CSn is deasserted before SCK. DSPI0 and DSPI1 have only MEDIUM SCK available.

4 The t_{CSC} delay value is configurable through a register. When configuring t_{CSC} (using PCSSCK and CSSCK fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{CSC} to ensure positive t_{CSCext}.

5 The t_{ASC} delay value is configurable through a register. When configuring t_{ASC} (using PASC and ASC fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{ASC} to ensure positive t_{ASCext}.

6 This delay value corresponds to SMPL_PT = 00b which is bit field 9 and 8 of DSPI_MCR register.

7 SCK and SOUT are configured as MEDIUM pad.

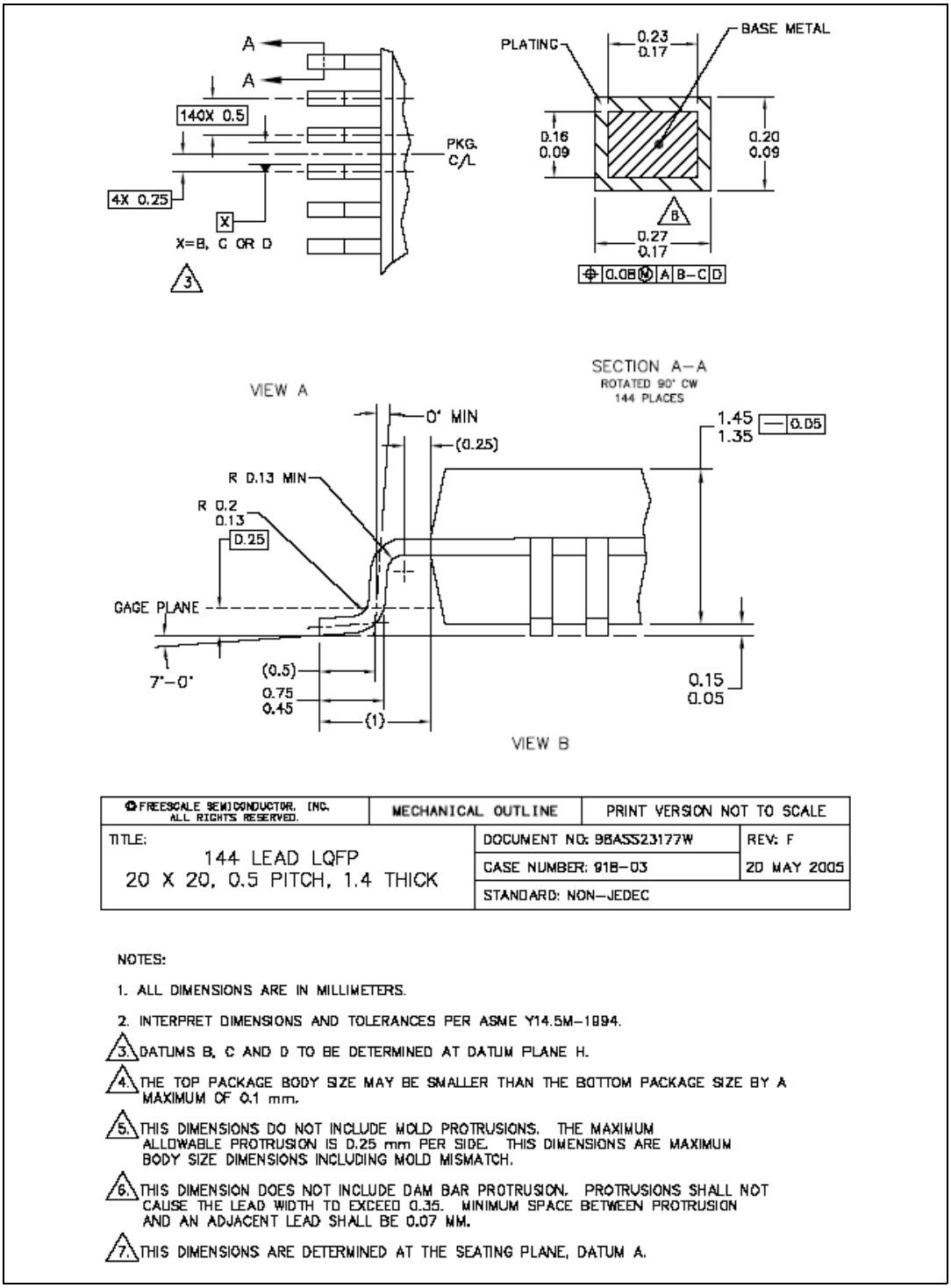
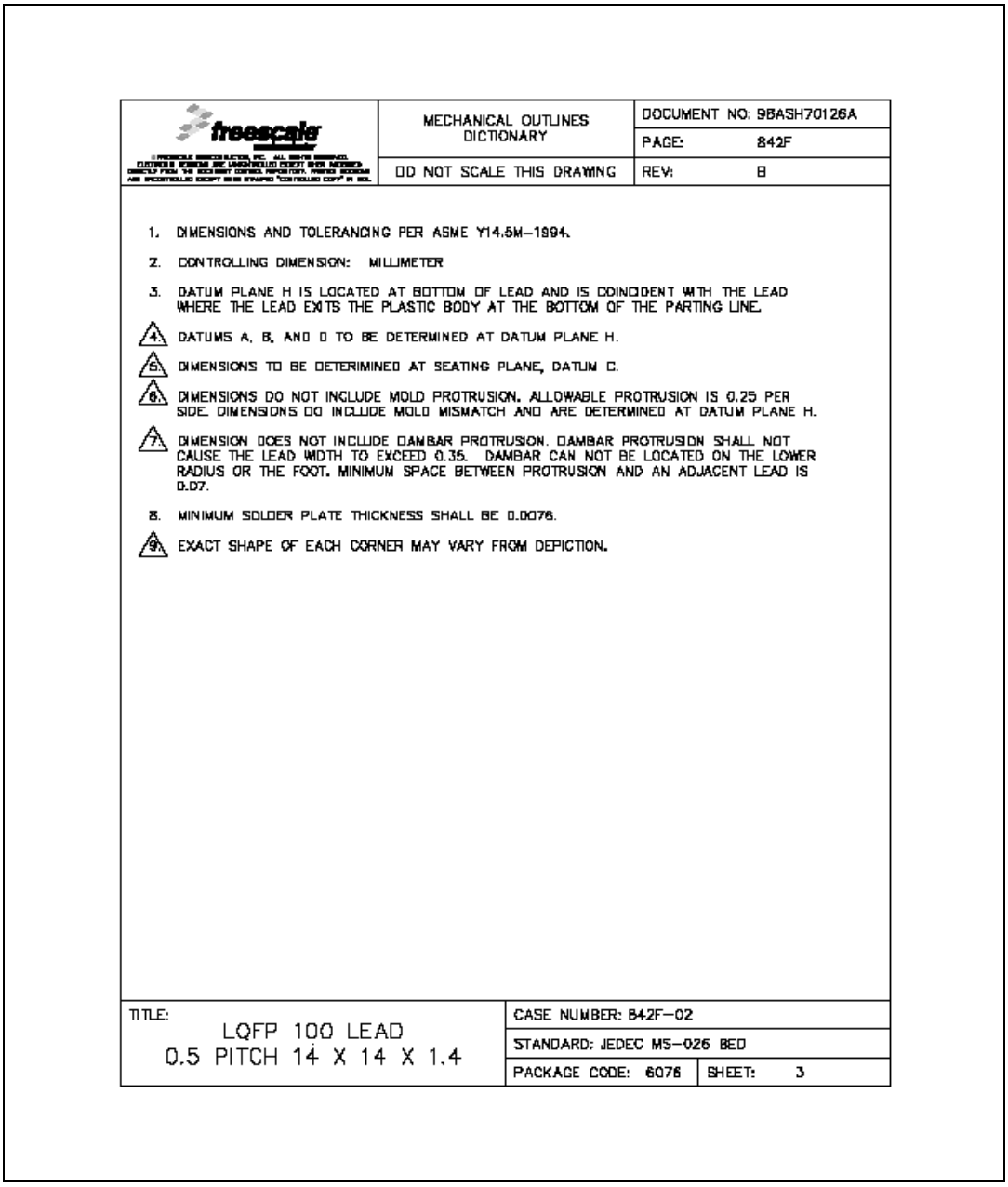


Figure 37. 144 LQFP package mechanical drawing (Part 2 of 2)



freescale	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASH70126A
		PAGE: 842F
	DO NOT SCALE THIS DRAWING	REV: B

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS TO BE DETERIMINED AT SEATING PLANE, DATUM C.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

TITLE: LQFP 100 LEAD 0.5 PITCH 14 X 14 X 1.4	CASE NUMBER: 842F–02	
	STANDARD: JEDEC MS–026 BED	
	PACKAGE CODE: 6076	SHEET: 3

Figure 40. 100 LQFP package mechanical drawing (Part 3 of 3)

5.1.4 208 MAPBGA

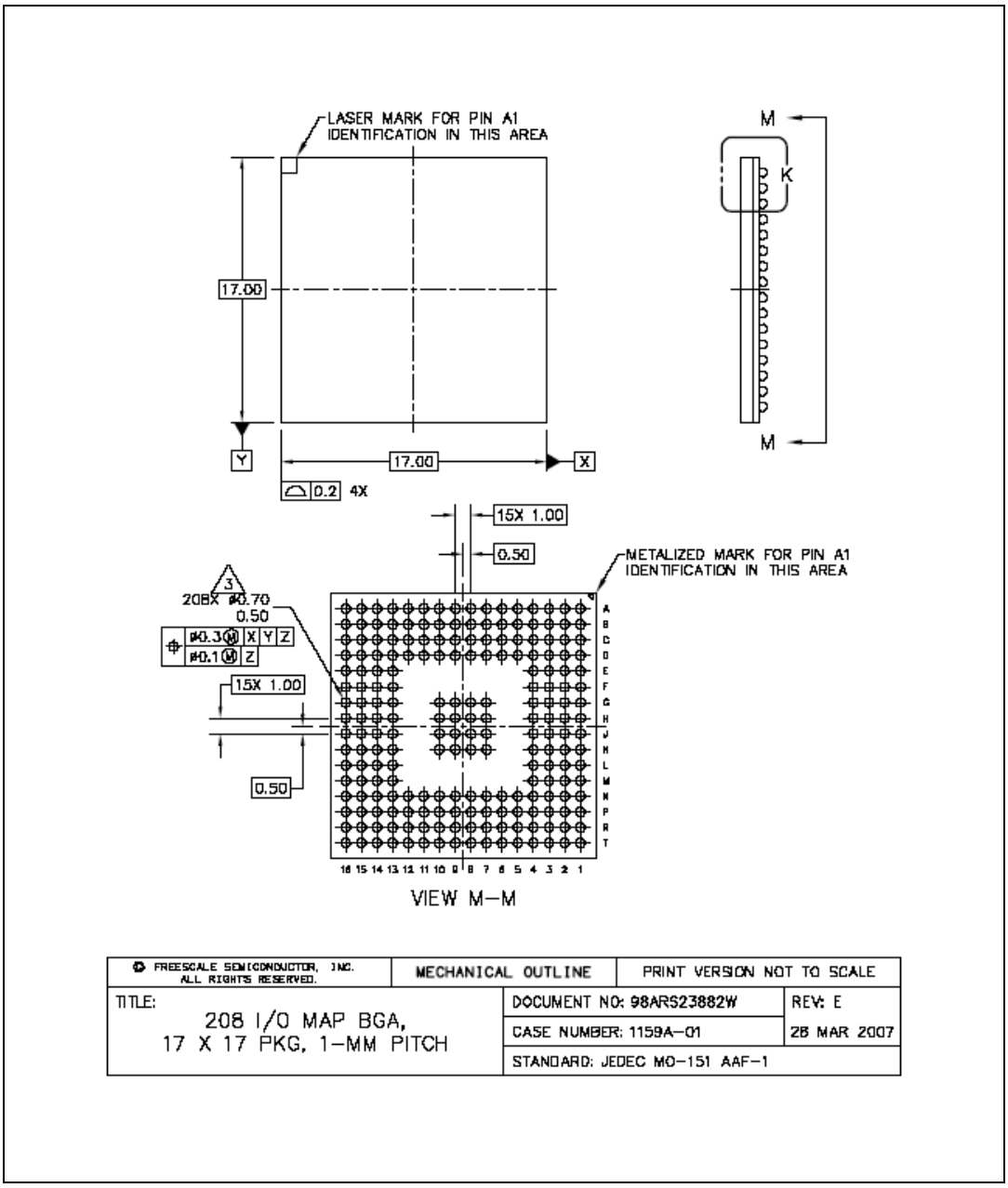


Figure 41. 208 MAPBGA package mechanical drawing (Part 1 of 2)

Appendix A Abbreviations

Table 50 lists abbreviations used but not defined elsewhere in this document.

Table 50. Abbreviations

Abbreviation	Meaning
CMOS	Complementary metal oxide semiconductor
CPHA	Clock phase
CPOL	Clock polarity
CS	Peripheral chip select
EVTO	Event out
MCKO	Message clock out
MDO	Message data out
MSEO	Message start/end out
MTFE	Modified timing format enable
SCK	Serial communications clock
SOUT	Serial data out
TBD	To be defined
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select