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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	149
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 29x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/ppc5605bclu48

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2 Block diagram

Figure 1 shows a top-level block diagram of the MPC5607B.

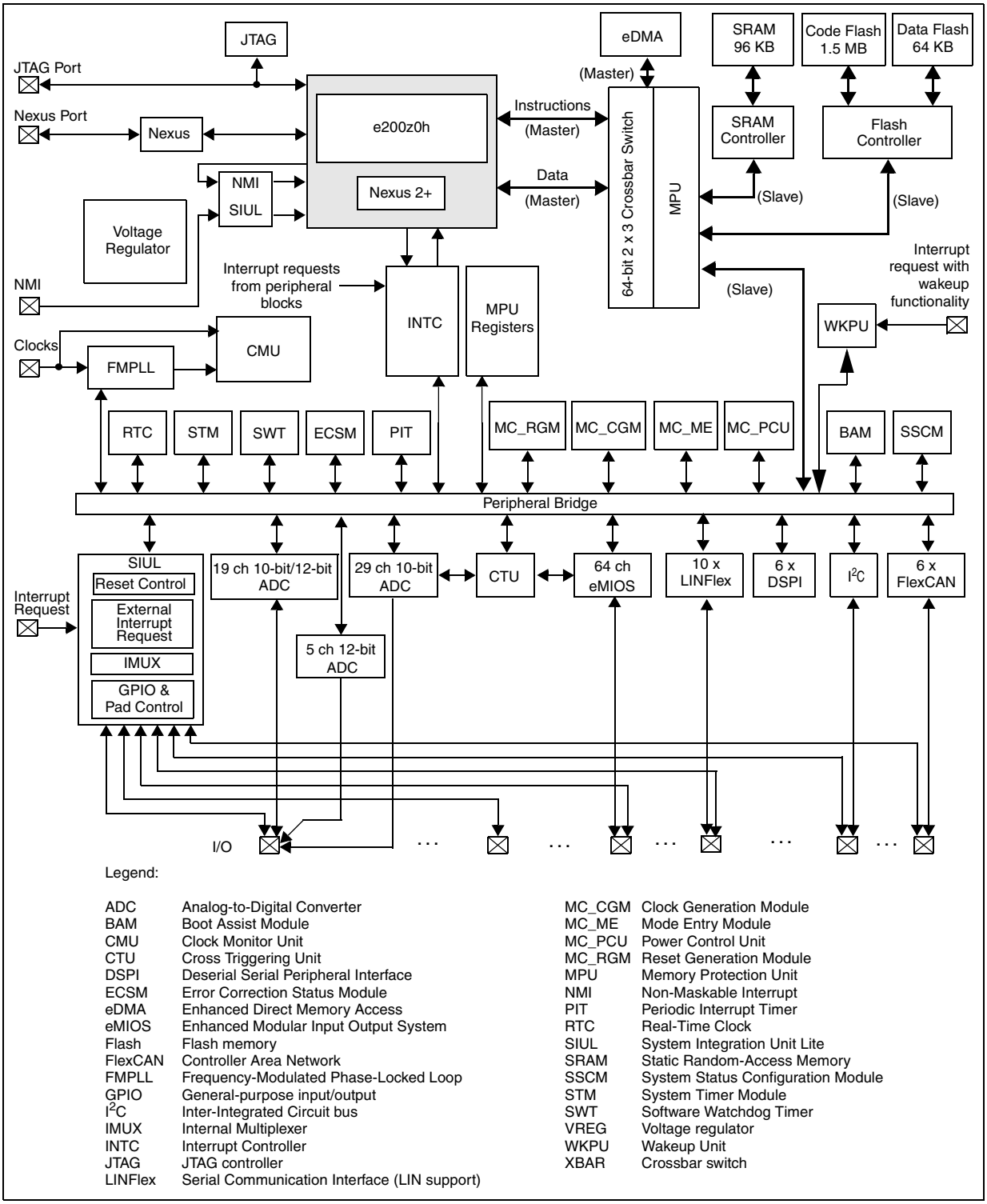

Figure 1. MPC5607B block diagram

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								100 LQFP	144 LQFP	176 LQFP	208 MAP BGA[4]
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 — — —	GPIO[43] — — MA[2] WKPU[5][5] CAN1RX CAN4RX	SIUL — — ADC_0 WKPU FlexCAN_1 FlexCAN_4	I/O — — O I I I	S	Tristate	21	27	35	M4
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 — —	GPIO[44] E0UC[12] — — EIRQ[19] SIN_2	SIUL eMIOS_0 — — SIUL DSPI_2	I/O I/O — — I I	M	Tristate	97	141	173	B4
PC[13]	PCR[45]	AF0 AF1 AF2 AF3	GPIO[45] E0UC[13] SOUT_2 —	SIUL eMIOS_0 DSPI_2 —	I/O I/O O —	S	Tristate	98	142	174	A2
PC[14]	PCR[46]	AF0 AF1 AF2 AF3 —	GPIO[46] E0UC[14] SCK_2 — EIRQ[8]	SIUL eMIOS_0 DSPI_2 — SIUL	I/O I/O I/O — I	S	Tristate	3	3	3	C1
PC[15]	PCR[47]	AF0 AF1 AF2 AF3 —	GPIO[47] E0UC[15] CS0_2 — EIRQ[20]	SIUL eMIOS_0 DSPI_2 — SIUL	I/O I/O I/O — I	M	Tristate	4	4	4	D3
Port D											
PD[0]	PCR[48]	AF0 AF1 AF2 AF3 — — —	GPIO[48] — — — WKPU[27][5] ADC0_P[4] ADC1_P[4]	SIUL — — — WKPU ADC_0 ADC_1	I — — — I I I	I	Tristate	41	63	77	P12
PD[1]	PCR[49]	AF0 AF1 AF2 AF3 — — —	GPIO[49] — — — WKPU[28][5] ADC0_P[5] ADC1_P[5]	SIUL — — — WKPU ADC_0 ADC_1	I — — — I I I	I	Tristate	42	64	78	T12

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								100 LQFP	144 LQFP	176 LQFP	208 MAP BGA[4]
PF[8]	PCR[88]	AF0 AF1 AF2 AF3	GPIO[88] CAN3TX CS4_0 CAN2TX	SIUL FlexCAN_3 DSPI_0 FlexCAN_2	I/O O O O	M	Tristate	—	34	42	P1
PF[9]	PCR[89]	AF0 AF1 AF2 AF3 — — —	GPIO[89] E1UC[1] CS5_0 — WKPU[22][5] CAN2RX CAN3RX	SIUL eMIOS_1 DSPI_0 — WKPU FlexCAN_2 FlexCAN_3	I/O I/O O — I I I	S	Tristate	—	33	41	N2
PF[10]	PCR[90]	AF0 AF1 AF2 AF3	GPIO[90] CS1_0 LIN4TX E1UC[2]	SIUL DSPI_0 LINFlex_4 eMIOS_1	I/O O O I/O	M	Tristate	—	38	46	R3
PF[11]	PCR[91]	AF0 AF1 AF2 AF3 — —	GPIO[91] CS2_0 E1UC[3] — WKPU[15][5] LIN4RX	SIUL DSPI_0 eMIOS_1 — WKPU LINFlex_4	I/O O I/O — I I	S	Tristate	—	39	47	R4
PF[12]	PCR[92]	AF0 AF1 AF2 AF3	GPIO[92] E1UC[25] LIN5TX —	SIUL eMIOS_1 LINFlex_5 —	I/O I/O O —	M	Tristate	—	35	43	R1
PF[13]	PCR[93]	AF0 AF1 AF2 AF3 — —	GPIO[93] E1UC[26] — — WKPU[16][5] LIN5RX	SIUL eMIOS_1 — — WKPU LINFlex_5	I/O I/O — — I I	S	Tristate	—	41	49	T6
PF[14]	PCR[94]	AF0 AF1 AF2 AF3	GPIO[94] CAN4TX E1UC[27] CAN1TX	SIUL FlexCAN_4 eMIOS_1 FlexCAN_1	I/O O I/O O	M	Tristate	—	102	126	D14
PF[15]	PCR[95]	AF0 AF1 AF2 AF3 — — —	GPIO[95] E1UC[4] — — EIRQ[13] CAN1RX CAN4RX	SIUL eMIOS_1 — — SIUL FlexCAN_1 FlexCAN_4	I/O I/O — — I I I	S	Tristate	—	101	125	E15
Port G											

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								100 LQFP	144 LQFP	176 LQFP	208 MAP BGA[4]
PG[0]	PCR[96]	AF0 AF1 AF2 AF3	GPIO[96] CAN5TX E1UC[23] —	SIUL FlexCAN_5 eMIOS_1 —	I/O O I/O —	M	Tristate	—	98	122	E14
PG[1]	PCR[97]	AF0 AF1 AF2 AF3 — —	GPIO[97] — E1UC[24] — EIRQ[14] CAN5RX	SIUL — eMIOS_1 — SIUL FlexCAN_5	I/O — I/O — I I	S	Tristate	—	97	121	E13
PG[2]	PCR[98]	AF0 AF1 AF2 AF3	GPIO[98] E1UC[11] SOUT_3 —	SIUL eMIOS_1 DSPI_3 —	I/O I/O O —	M	Tristate	—	8	16	E4
PG[3]	PCR[99]	AF0 AF1 AF2 AF3 —	GPIO[99] E1UC[12] CS0_3 — WKPU[17][5]	SIUL eMIOS_1 DSPI_3 — WKPU	I/O I/O I/O — I	S	Tristate	—	7	15	E3
PG[4]	PCR[100]	AF0 AF1 AF2 AF3	GPIO[100] E1UC[13] SCK_3 —	SIUL eMIOS_1 DSPI_3 —	I/O I/O I/O —	M	Tristate	—	6	14	E1
PG[5]	PCR[101]	AF0 AF1 AF2 AF3 — —	GPIO[101] E1UC[14] — — WKPU[18][5] SIN_3	SIUL eMIOS_1 — — WKPU DSPI_3	I/O I/O — — I I	S	Tristate	—	5	13	E2
PG[6]	PCR[102]	AF0 AF1 AF2 AF3	GPIO[102] E1UC[15] LIN6TX —	SIUL eMIOS_1 LINFlex_6 —	I/O I/O O —	M	Tristate	—	30	38	M2
PG[7]	PCR[103]	AF0 AF1 AF2 AF3 — —	GPIO[103] E1UC[16] E1UC[30] — WKPU[20][5] LIN6RX	SIUL eMIOS_1 eMIOS_1 — WKPU LINFlex_6	I/O I/O I/O — I I	S	Tristate	—	29	37	M1

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								100 LQFP	144 LQFP	176 LQFP	208 MAP BGA[4]
PI[4]	PCR[132]	AF0 AF1 AF2 AF3	GPIO[132] E1UC[28] SOUT_4 —	SIUL eMIOS_1 DSPI_4 —	I/O I/O O —	S	Tristate	—	—	143	A12
PI[5]	PCR[133]	AF0 AF1 AF2 AF3	GPIO[133] E1UC[29] SCK_4 —	SIUL eMIOS_1 DSPI_4 —	I/O I/O I/O —	S	Tristate	—	—	142	C12
PI[6]	PCR[134]	AF0 AF1 AF2 AF3	GPIO[134] E1UC[30] CS0_4 —	SIUL eMIOS_1 DSPI_4 —	I/O I/O I/O —	S	Tristate	—	—	11	D2
PI[7]	PCR[135]	AF0 AF1 AF2 AF3	GPIO[135] E1UC[31] CS1_4 —	SIUL eMIOS_1 DSPI_4 —	I/O I/O O —	S	Tristate	—	—	12	D3
PI[8]	PCR[136]	AF0 AF1 AF2 AF3 —	GPIO[136] — — — ADC0_S[16]	SIUL — — — ADC_0	I/O — — — I	J	Tristate	—	—	108	J13
PI[9]	PCR[137]	AF0 AF1 AF2 AF3 —	GPIO[137] — — — ADC0_S[17]	SIUL — — — ADC_0	I/O — — — I	J	Tristate	—	—	109	J14
PI[10]	PCR[138]	AF0 AF1 AF2 AF3 —	GPIO[138] — — — ADC0_S[18]	SIUL — — — ADC_0	I/O — — — I	J	Tristate	—	—	110	J15
PI[11]	PCR[139]	AF0 AF1 AF2 AF3 — —	GPIO[139] — — — ADC0_S[19] SIN_3	SIUL — — — ADC_0 DSPI_3	I/O — — — I I	J	Tristate	—	—	111	J16
PI[12]	PCR[140]	AF0 AF1 AF2 AF3 —	GPIO[140] CS0_3 — — ADC0_S[20]	SIUL DSPI_3 — — ADC_0	I/O I/O — — I	J	Tristate	—	—	112	G14

Table 12. Recommended operating conditions (3.3 V) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_ADC}[4]	SR	Voltage on VDD_HV_ADC0, VDD_HV_ADC1 (ADC reference) with respect to ground (V_{SS})	—	3.0[5]	3.6	V
			Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	—	V
			Relative to V_{DD}	—	V_{DD} + 0.1	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–5	5	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
TV_{DD}	SR	V_{DD} slope to ensure correct power up[6]	—	—	0.25	V/µs
$T_{A\ C\text{-}Grade\ Part}$	SR	Ambient temperature under bias	f_{CPU} < 64 MHz[7]	–40	85	°C
$T_{J\ C\text{-}Grade\ Part}$	SR	Junction temperature under bias	—	–40	110	
$T_{A\ V\text{-}Grade\ Part}$	SR	Ambient temperature under bias	f_{CPU} < 64 MHz[7]	–40	105	
$T_{J\ V\text{-}Grade\ Part}$	SR	Junction temperature under bias	—	–40	130	
$T_{A\ M\text{-}Grade\ Part}$	SR	Ambient temperature under bias	f_{CPU} < 64 MHz[7]	–40	125	
$T_{J\ M\text{-}Grade\ Part}$	SR	Junction temperature under bias	—	–40	150	

1 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.

2 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.

3 470 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics). Supply ramp slope on VDD_BV should always be faster or equal to slope of VDD_HV. Otherwise, device may enter regulator bypass mode if slope on VDD_BV is slower.

4 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.

5 Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed. When voltage drops below V_{LVDHVL}, device is reset.

6 Guaranteed by device validation

7 This frequency includes the 4% frequency modulation guardband.

Table 13. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}[1]	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	4.5	5.5	V
			Voltage drop[2]	3.0	5.5	
V_{SS_LV}[3]	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V

Table 13. Recommended operating conditions (5.0 V) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{DD_BV}[4]	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	4.5	5.5	V
			Voltage drop[2]	3.0	5.5	
			Relative to V_{DD}	3.0	V_{DD} + 0.1	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_ADC}[5]	SR	Voltage on VDD_HV_ADC0, VDD_HV_ADC1 (ADC reference) with respect to ground (V_{SS})	—	4.5	5.5	V
			Voltage drop[2]	3.0	5.5	
			Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	—	V
			Relative to V_{DD}	—	V_{DD} + 0.1	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–5	5	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
TV_{DD}	SR	V_{DD} slope to ensure correct power up[6]	—	—	0.25	V/µs
T_{A} C-Grade Part	SR	Ambient temperature under bias	f_{CPU} < 64 MHz[7]	–40	85	°C
T_{J} C-Grade Part	SR	Junction temperature under bias	—	–40	110	
T_{A} V-Grade Part	SR	Ambient temperature under bias	f_{CPU} < 64 MHz[7]	–40	105	
T_{J} V-Grade Part	SR	Junction temperature under bias	—	–40	130	
T_{A} M-Grade Part	SR	Ambient temperature under bias	f_{CPU} < 64 MHz[7]	–40	125	
T_{J} M-Grade Part	SR	Junction temperature under bias	—	–40	150	

1 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.

2 Full device operation is guaranteed by design when the voltage drops below 4.5 V down to 3.0 V. However, certain analog electrical characteristics will not be guaranteed to stay within the stated limits.

3 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.

4 470 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics). While the supply voltage ramps up, the slope on V_{DD_BV} should be less than $0.9V_{DD\_HV}$ in order to ensure the device does not enter regulator bypass mode.

5 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.

6 Guaranteed by device validation. Please refer to Section 4.5.1, “External ballast resistor recommendations for minimum V_{DD} slope to be guaranteed to ensure correct power up in case of external resistor usage.

7 This frequency includes the 4% frequency modulation guardband.

NOTE

RAM data retention is guaranteed with V_{DD_LV} not below 1.08 V.

Table 15. I/O input DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	—		$0.65V_{DD}$	—	V_{DD} + 0.4	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	—		–0.4	—	$0.35V_{DD}$	
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—		$0.1V_{DD}$	—	—	
I_{LKG}	CC	D	Digital input leakage	No injection on adjacent pin	T_A = –40 °C	—	2	200	nA
		D			T_A = 25 °C	—	2	200	
		D			T_A = 85 °C	—	5	300	
		D			T_A = 105 °C	—	12	500	
		P			T_A = 125 °C	—	70	1000	
W_{FI}[2]	SR	P	Wakeup input filtered pulse	—		—	—	40	ns
W_{NFI}[2]	SR	P	Wakeup input not filtered pulse	—		1000	—	—	ns

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 In the range from 40 to 1000 ns, pulses can be filtered or not filtered, according to operating temperature and voltage.

4.6.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- Table 16 provides weak pull figures. Both pull-up and pull-down resistances are supported.
- Table 17 provides output driver characteristics for I/O pads when in SLOW configuration.
- Table 18 provides output driver characteristics for I/O pads when in MEDIUM configuration.
- Table 19 provides output driver characteristics for I/O pads when in FAST configuration.

Table 16. I/O pull-up/pull-down DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
$\lvert I_{WPU}\rvert$	CC	P	Weak pull-up current absolute value	V_{IN} = V_{IL}, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1[2]	10	—	250	
		P		V_{IN} = V_{IL}, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	
$\lvert I_{WPD}\rvert$	CC	P	Weak pull-down current absolute value	V_{IN} = V_{IH}, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1	10	—	250	
		P		V_{IN} = V_{IH}, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 22. I/O consumption (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{RMSFST}	CC	D	Root mean square I/O current for FAST configuration	C_L = 25 pF, 40 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	22	mA
				C_L = 25 pF, 64 MHz		—	—	33	
				C_L = 100 pF, 40 MHz		—	—	56	
				C_L = 25 pF, 40 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	14	
				C_L = 25 pF, 64 MHz		—	—	20	
				C_L = 100 pF, 40 MHz		—	—	35	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	65	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to125 °C, unless otherwise specified

2 Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

Table 23 provides the weight of concurrent switching I/Os.

Due to the dynamic current limitations, the sum of the weight of concurrent switching I/Os on a single segment must not exceed 100% to ensure device functionality.

Table 23. I/O weight[1]

Supply segment			Pad	176 LQFP				144/100 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
176 LQFP	144 LQFP	100 LQFP		SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
6	4	4	PB[3]	5%	—	6%	—	13%	—	15%	—
			PC[9]	4%	—	5%	—	13%	—	15%	—
			PC[14]	4%	—	4%	—	13%	—	15%	—
			PC[15]	3%	4%	4%	4%	12%	18%	15%	16%
	—	—	PJ[4]	3%	4%	3%	3%	—	—	—	—

Table 23. I/O weight[1] (continued)

Supply segment			Pad	176 LQFP				144/100 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
176 LQFP	144 LQFP	100 LQFP		SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
2	1	—	PG[9]	9%	—	10%	—	9%	—	10%	—
		—	PG[8]	9%	—	11%	—	9%	—	11%	—
		1	PC[11]	9%	—	11%	—	9%	—	11%	—
			PC[10]	9%	13%	11%	12%	9%	13%	11%	12%
		—	PG[7]	9%	—	11%	—	9%	—	11%	—
		—	PG[6]	10%	14%	11%	12%	10%	14%	11%	12%
		1	PB[0]	10%	14%	12%	12%	10%	14%	12%	12%
			PB[1]	10%	—	12%	—	10%	—	12%	—
		—	PF[9]	10%	—	12%	—	10%	—	12%	—
		—	PF[8]	10%	14%	12%	13%	10%	14%	12%	13%
		—	PF[12]	10%	15%	12%	13%	10%	15%	12%	13%
		1	PC[6]	10%	—	12%	—	10%	—	12%	—
			PC[7]	10%	—	12%	—	10%	—	12%	—
		—	PF[10]	10%	14%	11%	12%	10%	14%	11%	12%
		—	PF[11]	9%	—	11%	—	9%	—	11%	—
		1	PA[15]	8%	12%	10%	10%	8%	12%	10%	10%
		—	PF[13]	8%	—	10%	—	8%	—	10%	—
		1	PA[14]	8%	11%	9%	10%	8%	11%	9%	10%
			PA[4]	7%	—	9%	—	7%	—	9%	—
			PA[13]	7%	10%	8%	9%	7%	10%	8%	9%
			PA[12]	7%	—	8%	—	7%	—	8%	—

4.8 Power management electrical characteristics

4.8.1 Voltage regulator electrical characteristics

The device implements an internal voltage regulator to generate the low voltage core supply V_{DD_LV} from the high voltage ballast supply V_{DD_BV}. The regulator itself is supplied by the common I/O supply V_{DD}. The following supplies are involved:

- HV: High voltage external power supply for voltage regulator module. This must be provided externally through V_{DD} power pin.
- BV: High voltage external power supply for internal ballast module. This must be provided externally through V_{DD_BV} power pin. Voltage values should be aligned with V_{DD}.
- LV: Low voltage internal power supply for core, FMPLL and Flash digital logic. This is generated by the internal voltage regulator but provided outside to connect stability capacitor. It is further split into four main domains to ensure noise isolation between critical LV modules within the device:
  - LV_COR: Low voltage supply for the core. It is also used to provide supply for FMPLL through double bonding.
  - LV_CFLA: Low voltage supply for code flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
  - LV_DFLA: Low voltage supply for data flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
  - LV_PLL: Low voltage supply for FMPLL. It is shorted to LV_COR through double bonding.

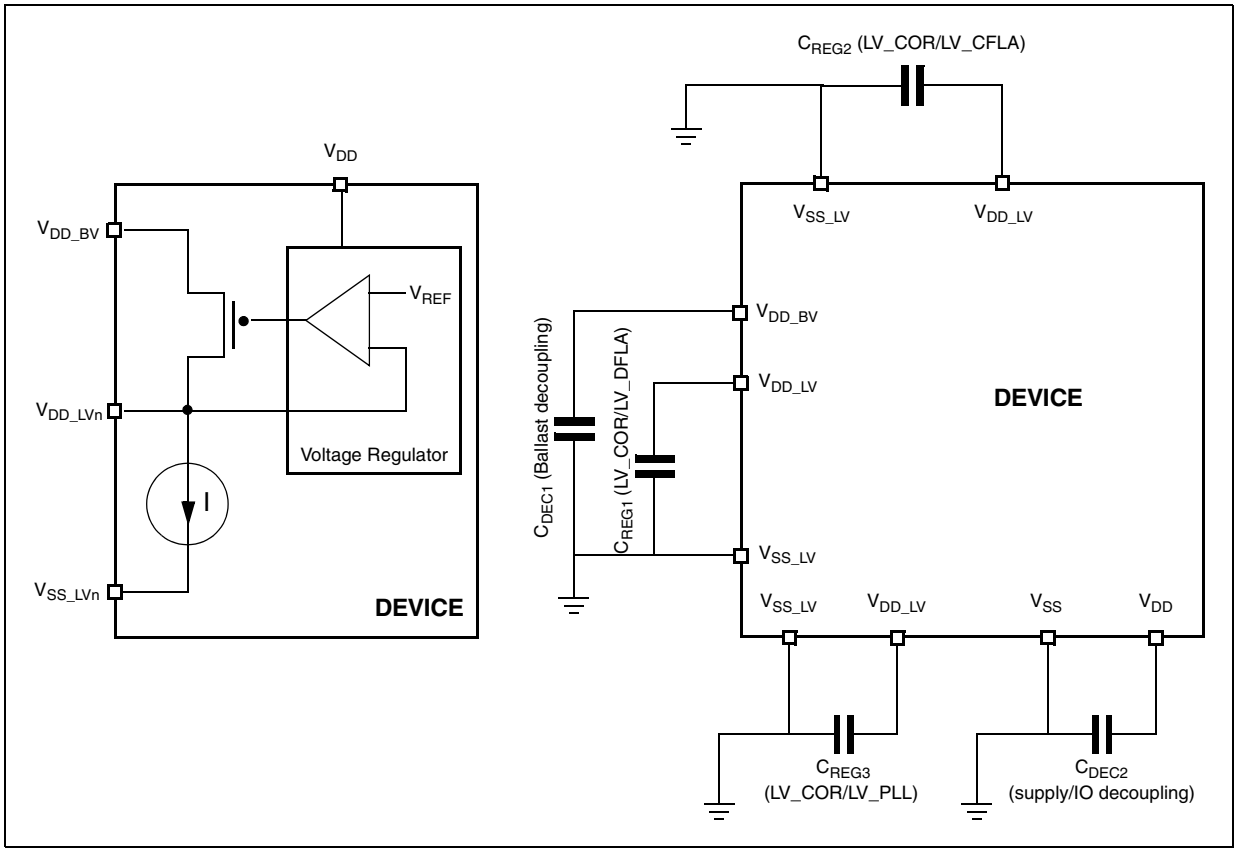

Figure 9. Voltage regulator capacitance connection

The internal voltage regulator requires external capacitance (C_{REGn}) to be connected to the device in order to provide a stable low voltage digital supply to the device. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 5 nH.

Table 31. Flash power supply DC electrical characteristics

Symbol		Parameter	Conditions[1]		Value			Unit
					Min	Typ	Max	
I_{CFREAD}	CC	Sum of the current consumption on V_{DD_HV} and V_{DD_BV} on read access	Flash module read f_{CPU} = 64 MHz	Code Flash	—	—	33	mA
I_{DFREAD}				Data Flash	—	—	33	
I_{CFMOD}	CC	Sum of the current consumption on V_{DD_HV} and V_{DD_BV} on matrix modification (program/erase)	Program/Erase on-going while reading Flash registers f_{CPU} = 64 MHz	Code Flash	—	—	52	mA
I_{DFMOD}				Data Flash	—	—	33	
I_{CFLPW}	CC	Sum of the current consumption on V_{DD_HV} and V_{DD_BV} during Flash low power mode	—	Code Flash	—	—	1.1	mA
I_{DFLPW}				Data Flash	—	—	900	µA
I_{CFPWD}	CC	Sum of the current consumption on V_{DD_HV} and V_{DD_BV} during Flash power down mode	—	Code Flash	—	—	150	µA
I_{DFPWD}				Data Flash	—	—	150	

[1] V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

4.10.3 Start-up/Switch-off timings

Table 32. Start-up time/Switch-off time

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
$t_{FLARSTEXIT}$	CC	T	Delay for Flash module to exit reset mode	—	—	—	125	µs
$t_{FLALPEXIT}$	CC	T	Delay for Flash module to exit low-power mode	—	—	—	0.5	
$t_{FLAPDEXIT}$	CC	T	Delay for Flash module to exit power-down mode	—	—	—	30	
$t_{FLALPENTRY}$	CC	T	Delay for Flash module to enter low-power mode	—	—	—	0.5	
$t_{FLAPDENTRY}$	CC	T	Delay for Flash module to enter power-down mode	—	—	—	1.5	

[1] V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

4.11 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

4.11.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and prequalification tests in relation with the EMC level requested for the application.

- Software recommendations – The software flowchart must include the management of runaway conditions such as:
  - Corrupted program counter

— Unexpected reset
— Critical data corruption (control registers...)

- Prequalification trials – Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.
  To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

4.11.2 Electromagnetic interference (EMI)

The product is monitored in terms of emission based on a typical application. This emission test conforms to the IEC61967-1 standard, which specifies the general conditions for EMI measurements.

Table 33. EMI radiated emission measurement[1,2]

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
—	SR	—	Scan range	—		0.150		1000	MHz
f_{CPU}	SR	—	Operating frequency	—		—	64	—	MHz
V_{DD_LV}	SR	—	LV operating voltages	—		—	1.28	—	V
S_{EMI}	CC	T	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP144 package Test conforming to IEC 61967-2, f_{OSC} = 8 MHz/f_{CPU} = 64 MHz	No PLL frequency modulation	—	—	18	dBµV
					± 2% PLL frequency modulation	—	—	14	dBµV

1 EMI testing and I/O port waveforms per IEC 61967-1, -2, -4

2 For information on conducted emission and susceptibility measurement (norm IEC 61967-4), please contact your local marketing representative.

4.11.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

4.11.3.1 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts×(n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

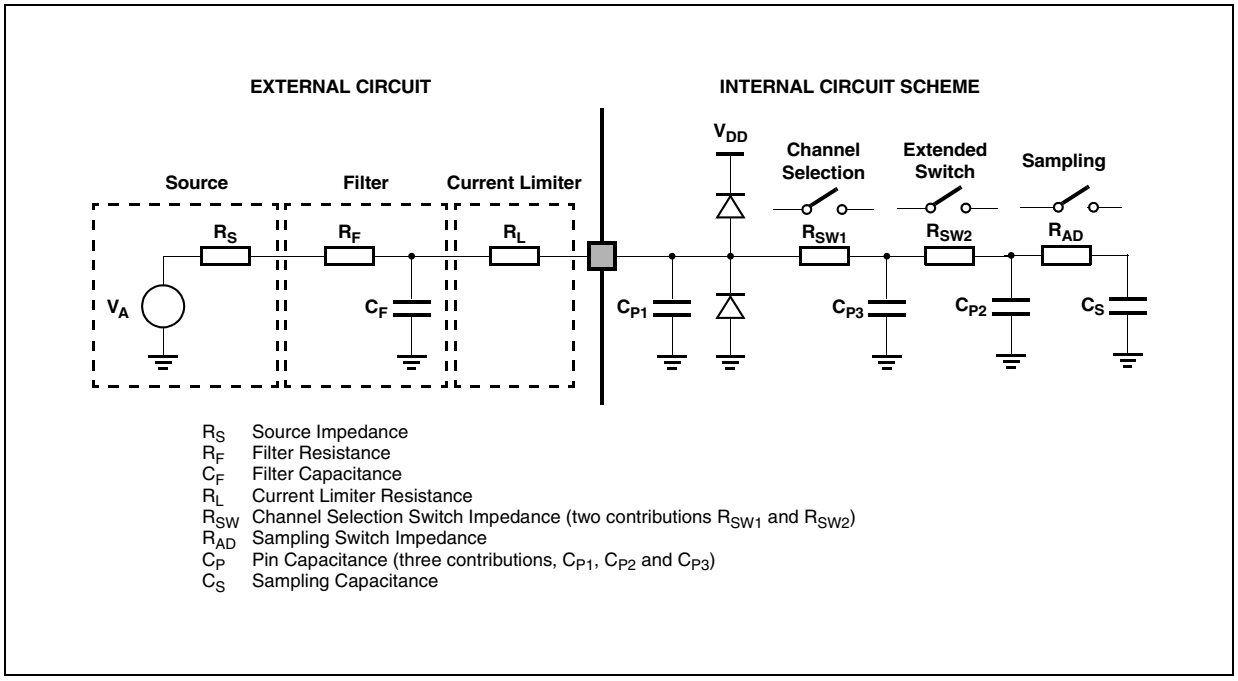

Figure 18. Input equivalent circuit (extended channels)

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 17): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

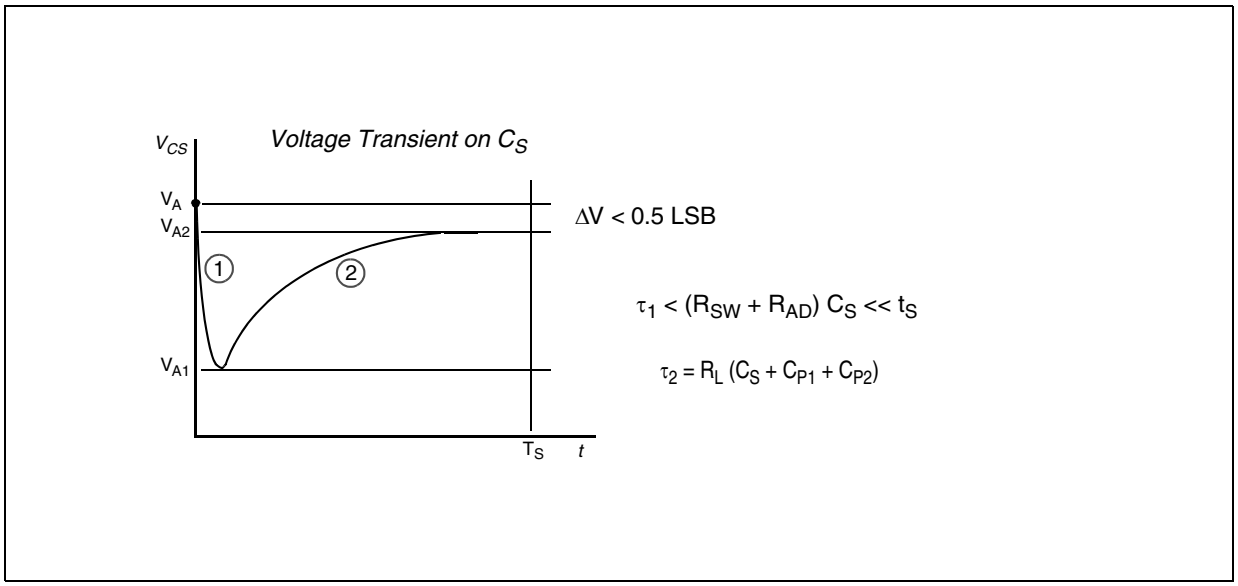

Figure 19. Transient behavior during sampling phase

In particular two different transient periods can be distinguished:

1. A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

4.18 On-chip peripherals

4.18.1 Current consumption

Table 46. On-chip peripherals current consumption[1]

Symbol		C	Parameter	Conditions		Typical value[2]	Unit
$I_{DD\_BV(CAN)}$	CC	T	CAN (FlexCAN) supply current on V_{DD_BV}	Bitrate: 500 Kbyte/s	Total (static + dynamic) consumption: • FlexCAN in loop-back mode • XTAL at 8 MHz used as CAN engine clock source • Message sending period is 580 µs	8 * f_{periph} + 85	µA
				Bitrate: 125 Kbyte/s		8 * f_{periph} + 27	
$I_{DD\_BV(eMIOS)}$	CC	T	eMIOS supply current on V_{DD_BV}	Static consumption: • eMIOS channel OFF • Global prescaler enabled		29 * f_{periph}	µA
				Dynamic consumption: • It does not change varying the frequency (0.003 mA)		3	
$I_{DD\_BV(SCI)}$	CC	T	SCI (LINFlex) supply current on V_{DD_BV}	Total (static + dynamic) consumption: • LIN mode • Baudrate: 20 Kbyte/s		5 * f_{periph} + 31	µA
$I_{DD\_BV(SPI)}$	CC	T	SPI (DSPI) supply current on V_{DD_BV}	Ballast static consumption (only clocked)		1	µA
				Ballast dynamic consumption (continuous communication): • Baudrate: 2 Mbit/s • Trasmission every 8 µs • Frame: 16 bits		16 * f_{periph}	
I_{DD_BV} (ADC_0/ADC_1)	CC	T	ADC_0/ADC_1 supply current on V_{DD_BV}	V_{DD} = 5.5 V	Ballast static consumption (no conversion)[3]	41 * f_{periph}	µA
					Ballast dynamic consumption (continuous conversion)[3]	46 * f_{periph}	
$I_{DD\_HV\_ADC0}$	CC	T	ADC_0 supply current on $V_{DD\_HV\_ADC0}$	V_{DD} = 5.5 V	Analog static consumption (no conversion)	200	µA
					Analog dynamic consumption (continuous conversion)	3	mA
$I_{DD\_HV\_ADC1}$	CC	T	ADC_1 supply current on $V_{DD\_HV\_ADC1}$	V_{DD} = 5.5 V	Analog static consumption (no conversion)	300 * f_{periph}	µA
					Analog dynamic consumption (continuous conversion)	4	mA
$I_{DD\_HV(FLASH)}$	CC	T	CFlash + DFlash supply current on V_{DD_HV}	V_{DD} = 5.5 V	—	12	mA
$I_{DD\_HV(PLL)}$	CC	T	PLL supply current on V_{DD_HV}	V_{DD} = 5.5 V	—	30 * f_{periph}	µA

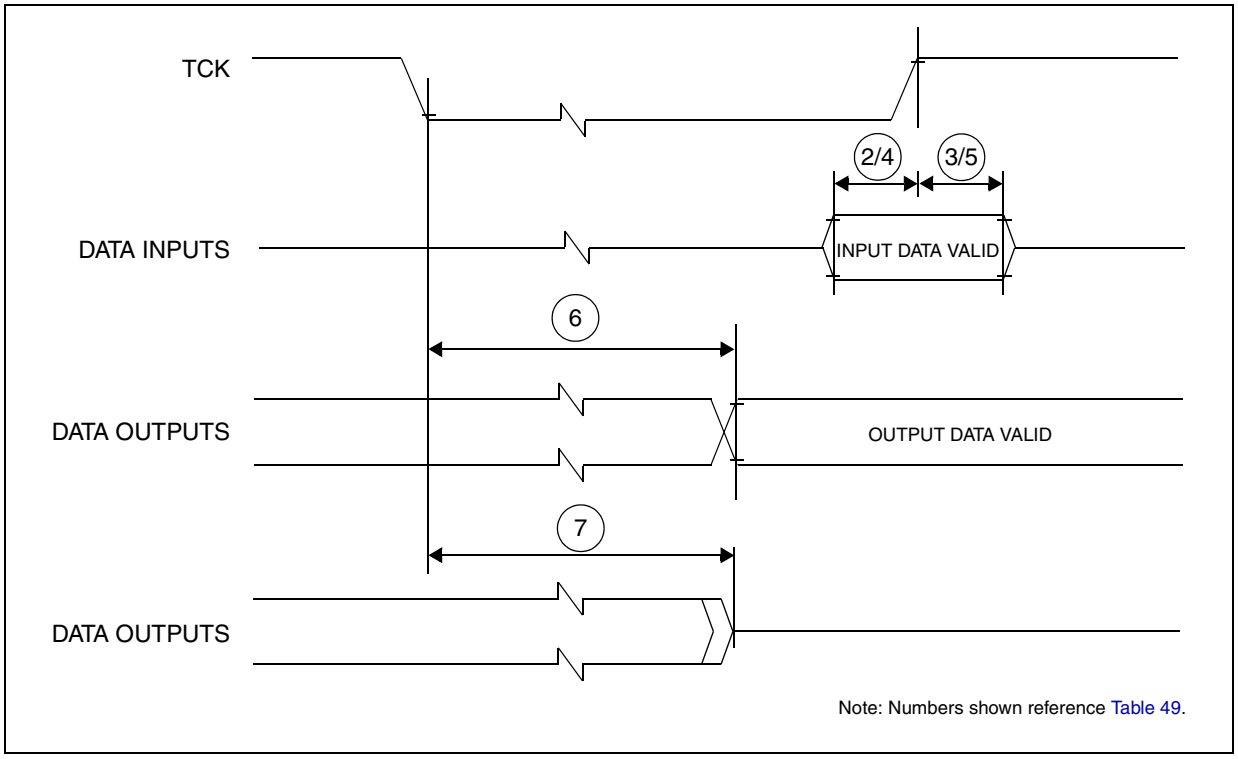

Figure 32. Timing diagram — JTAG boundary scan

7 Revision history

Table 51 summarizes revisions to this document.

Table 51. Revision history

Revision	Date	Substantive changes
1	12-Jan-2009	Initial release
2	09 Nov-2009	Updated Features Replaced 27 IRQs in place of 23 ADC features External Ballast resistor support conditions Updated device summary-added 208 BGA details Updated block diagram to include WKUP Updated block diagram to include 5 ch ADC 12 -bit Updated Block summary table Updated LQFP 144, 176 and 100 pinouts. Applied new naming convention for ADC signals as ADCx_P[x] and ADCx_S[x] Section 1, “General description Updated MPC5607B device comparison table Updated block diagram-aligned with 512k Updated block summary-aligned with 512k Section 2, “Package pinouts Updated 100,144,176,208 packages according to cut2.0 changes Added Section 3.5.1, “External ballast resistor recommendations Added NVUSRO [WATCHDOG_EN] field description Updated Absolute maximum ratings Updated LQFP thermal characteristics Updated I/O supply segments Updated Voltage regulator capacitance connection Updated Low voltage monitor electrical characteristics Updated Low voltage power domain electrical characteristics Updated DC electrical characteristics Updated Program/Erase specifications Updated Conversion characteristics (10 bit ADC) Updated FMPLL electrical characteristics Updated Fast RC oscillator electrical characteristics-aligned with MPC5604B Updated On-chip peripherals current consumption Updated ADC characteristics and error definitions diagram Updated ADC conversion characteristics (10 bit and 12 bit) Added ADC characteristics and error definitions diagram for 12 bit ADC
3	25 Jan-2010	Updated Features Updated block diagram to connect peripherals to pad I/O Updated block summary to include ADC 12-bit Updated 144, 176 and 100 pinouts to adjust format issues Table 26 Flash module life-retention value changed from 1-5 to 5 yrs Minor editing changes

Table 51. Revision history (continued)

Revision	Date	Substantive changes
4	24 Aug 2010	Editorial changes and improvements. Updated “Features“ section Table 1: updated footnote concerning 208 MAPBGA In the block diagram: • Added “5ch 12-bit ADC“ block. • Updated Legend. • Added “Interrupt request with wakeup functionality” as an input to the WKPU block. Figure 2: removed alternate functions Figure 3: removed alternate functions Figure 4: removed alternate functions Table 2: added contents concerning the following blocks: CMU, eDMA, ECSM, MC_ME, MC_PCU, NMI, SSCM, SWT and WKPU Added Section 3.2, Pin muxing Section 4, “Electrical characteristics: removed “Caution” note Section 4.2, “NVUSRO register: removed “NVUSRO[WATCHDOG_EN] field description“ section Table 11: V_{IN}: removed min value in “relative to V_{DD}” row Table 12 • $T_{A\ C\text{-}Grade\ Part}$, $T_{J\ C\text{-}Grade\ Part}$, $T_{A\ V\text{-}Grade\ Part}$, $T_{J\ V\text{-}Grade\ Part}$, $T_{A\ M\text{-}Grade\ Part}$, $T_{J\ M\text{-}Grade\ Part}$: added new rows • TV_{DD}: contents merged into one row • V_{DD_BV}: changed min value in “relative to V_{DD}” row Section 4.5, “Thermal characteristics • Section 4.5.1, “External ballast resistor recommendations: added new paragraph about power supply • Table 14: added $R_{\theta JB}$ and $R_{\theta JC}$ rows • Removed “208 MAPBGA thermal characteristics” table Table 15: rewrote parameter description of W_{FI} and W_{NFI} Section 4.6.5, “I/O pad current specification • Removed I_{DYNSEG} information • Updated “I/O supply segments” table Table 22: removed I_{DYNSEG} row Added Table 23 Table 25 • Updated all values • Removed $I_{VREGREF}$ and $I_{VREDLVD12}$ rows • Added the footnote “The duration of the in-rush current depends on the capacitance placed on LV pins. BV decaps must be sized accordingly. Refer to IMREG value for minimum amount of current to be provided in cc.” to the I_{DD_BV} specification. Table 26 • Updated V_{PORH} min/max value • Updated $V_{LVDLVCORL}$ min value Updated Table 27 Table 28 • $T_{dwprogram}$: added initial max value • Inserted T_{eslat} row Table 29: removed the “To be confirmed” footnote In the “Crystal oscillator and resonator connection scheme” figure, removed R_P Table 39 • Removed g_{mSXOSC} row • $I_{SXOSCBIAS}$: added min/typ/max value

Table 51. Revision history (continued)

Revision	Date	Substantive changes
6 (cont'd)	08 Jul 2011	Section "External ballast resistor recommendations": replaced "low voltage monitor" with "low voltage detector (LVD)" "I/O input DC electrical characteristics" table: updated I_{LKG} characteristics "MEDIUM configuration output buffer electrical characteristics" table: changed "I_{OH} = 100 µA" to "I_{OL} = 100 µA" in V_{OL} conditions I/O weight: updated table (includes replacing instances of bit "SRE" with "SRC") "Reset electrical characteristics" table: updated parameter classification for $\lvert I_{WPU} \rvert$ Updated voltage regulator electrical characteristics Section "Low voltage detector electrical characteristics": changed title (was "Voltage monitor electrical characteristics"); changed "as well as four low voltage detectors" to "as well as five low voltage detectors"; added event status flag names found in RGM chapter of device reference manual to POR module and LVD descriptions; replaced instances of "Low voltage monitor" with "Low voltage detector"; updated values for $V_{LVDLVBKPL}$ and $V_{LVDLVCORL}$ Updated section "Power consumption" Section "Program/erase characteristics": removed table "FLASH_BIU settings vs. frequency of operation" and associated introduction "Program and erase specifications" table: updated symbols PFCRn settings vs. frequency of operation: replaced "FLASH_BIU" with "PFCRn" in table title; updated field names and frequencies "Flash power supply DC electrical characteristics" table: deleted footnote 2 Crystal oscillator and resonator connection scheme: inserted footnote about possibly requiring a series resistor Fast external crystal oscillator (4 to 16 MHz) electrical characteristics: updated parameter classification for $V_{FXOSCOP}$ Slow external crystal oscillator (32 kHz) electrical characteristics: updated footnote 1 Section "ADC electrical characteristics": updated symbols for offset error and gain error Section "Input impedance and ADC accuracy": changed "V_A/V_{A2}" to "V_{A2}/V_A" in Equation 11 ADC input leakage current: updated I_{LKG} characteristics ADC_0 conversion characteristics table: replaced instances of "ADCx_conf_sample_input" with "INPSAMP"; replaced instances of "ADCx_conf_comp" with "INPCMP ADC_1 characteristic and error definitions: replaced "AVDD" with "V_{DD_ADC}" ADC_1 conversion characteristics table: replaced instances of "ADCx_conf_sample_input" with "INPSAMP"; replaced instances of "ADCx_conf_comp" with "INPCMP" Updated "On-chip peripherals current consumption" table