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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, SPI, UART, USB
Peripherals	DMA, I²S, LED, POR, PWM, WDT
Number of I/O	91
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-18
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4500-f144k1024-ab

	1	2	3	4	5	6	7	8	9	10	11	12	
A	VSS	VDDC	P0.2	P0.3	P0.5	P0.6	P3.6	P0.8	P4.1	P1.8	VDDP	VSS	A
B	VDDP	P3.1	P3.2	P0.10	P0.4	P3.5	P0.7	P4.0	P1.6	P1.7	P1.9	VDDC	B
C	P3.0	P3.13	P0.1	P0.0	P0.13	P0.15	P4.4	P4.6	P4.7	P1.4	P1.2	P1.3	C
D	USB_DM	P3.12	P3.11	P0.9	P0.12	P3.14	P3.15	P4.5	P1.0	P1.5	P1.11	P1.10	D
E	USB_DP	VBUS	P3.8	P3.7	P0.11	P0.14	P3.4	P4.2	P1.1	P1.14	P1.12	P1.13	E
F	RTC_XTAL2	RTC_XTAL1	HIB_IO_1	HIB_IO_0	P3.9	P3.10	P3.3	P4.3	P6.1	P6.4	P6.5	P6.6	F
G	VBAT	P15.3	P15.5	P15.4	P15.6	P15.7	TMS	TCK	P6.3	P6.0	$\overline{\text{PORST}}$	P1.15	G
H	P15.2	P14.15	P14.14	P14.13	P5.10	P5.8	P5.2	P5.1	P5.0	P6.2	XTAL1	XTAL2	H
J	P14.12	P14.7	P14.6	P14.3	P5.11	P2.15	P5.7	P5.5	P2.6	P5.3	P2.0	VSSO	J
K	P14.4	P14.5	P14.2	P15.15	P15.12	P5.9	P2.14	P5.6	P2.7	P5.4	P2.2	P2.1	K
L	VDDA	P14.1	P14.0	P15.14	P14.9	P15.9	P2.12	P2.10	P2.8	P2.4	P2.3	VDDP	L
M	VSSA	VAGND	VAREF	P15.13	P14.8	P15.8	P2.13	P2.11	P2.9	P2.5	VDDC	VSS	M
	1	2	3	4	5	6	7	8	9	10	11	12	

XMC4500- (top view)

Figure 6 XMC4500 PG-LFBGA-144 Pin Configuration (top view)

Table 9 Package Pin Mapping (cont'd)

Function	LQFP-144	LFBGA-144	LQFP-100	Pad Type	Notes
P5.3	81	J10	-	A2	
P5.4	80	K10	-	A2	
P5.5	79	J8	-	A2	
P5.6	78	K8	-	A2	
P5.7	77	J7	55	A1+	
P5.8	58	H6	-	A2	
P5.9	57	K6	-	A2	
P5.10	56	H5	-	A1+	
P5.11	55	J5	-	A1+	
P6.0	101	G10	-	A2	
P6.1	100	F9	-	A2	
P6.2	99	H10	-	A2	
P6.3	98	G9	-	A1+	
P6.4	97	F10	-	A2	
P6.5	96	F11	-	A2	
P6.6	95	F12	-	A2	
P14.0	42	L3	31	AN/DIG_IN	
P14.1	41	L2	30	AN/DIG_IN	
P14.2	40	K3	29	AN/DIG_IN	
P14.3	39	J4	28	AN/DIG_IN	
P14.4	38	K1	27	AN/DIG_IN	
P14.5	37	K2	26	AN/DIG_IN	
P14.6	36	J3	25	AN/DIG_IN	
P14.7	35	J2	24	AN/DIG_IN	
P14.8	52	M5	37	AN/DAC/DIG_IN	
P14.9	51	L5	36	AN/DAC/DIG_IN	
P14.12	34	J1	23	AN/DIG_IN	
P14.13	33	H4	22	AN/DIG_IN	
P14.14	32	H3	21	AN/DIG_IN	
P14.15	31	H2	20	AN/DIG_IN	
P15.2	30	H1	19	AN/DIG_IN	

Table 11 Port I/O Functions (cont'd)

Function	Outputs						Inputs									
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P6.6			DSD.MCLK3		DB.ETM_TRACEDATA0	$\overline{\text{EBU.BC3}}$			DSD.MCLK3A	ETH0.CLK_TXB						
P14.0									VADC.G0CH0							
P14.1									VADC.G0CH1							
P14.2									VADC.G0CH2	VADC.G1CH2						
P14.3									VADC.G0CH3	VADC.G1CH3			CAN.N0_RXDB			
P14.4									VADC.G0CH4		VADC.G2CH0					
P14.5									VADC.G0CH5		VADC.G2CH1		POSIF0.IN2B			
P14.6									VADC.G0CH6				POSIF0.IN1B		G0ORC6	
P14.7									VADC.G0CH7				POSIF0.IN0B		G0ORC7	
P14.8					DAC.OUT_0					VADC.G1CH0		VADC.G3CH2	ETH0.RXD0C			
P14.9					DAC.OUT_1					VADC.G1CH1		VADC.G3CH3	ETH0.RXD1C			
P14.12										VADC.G1CH4						
P14.13										VADC.G1CH5						
P14.14										VADC.G1CH6					G1ORC6	
P14.15										VADC.G1CH7					G1ORC7	
P15.2											VADC.G2CH2					
P15.3											VADC.G2CH3					
P15.4											VADC.G2CH4					
P15.5											VADC.G2CH5					
P15.6											VADC.G2CH6					
P15.7											VADC.G2CH7					
P15.8												VADC.G3CH0	ETH0.CLK_RMIIC			ETH0.CLKRXC
P15.9												VADC.G3CH1	ETH0.CRS_DVC			ETH0.RXDVC

Table 11 **Port I/O Functions** (cont'd)

Function	Outputs						Inputs									
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P15.12												VADC. G3CH4				
P15.13												VADC. G3CH5				
P15.14												VADC. G3CH6				
P15.15												VADC. G3CH7				
USB_DP																
USB_DM																
HIB_IO_0	HIBOUT	WWDT. SERVICE_OUT							WAKEUPA							
HIB_IO_1	HIBOUT	WWDT. SERVICE_OUT							WAKEUPB							
TCK							DB.TCK/ SWCLK									
TMS					DB.TMS/ SWDIO											
$\overline{\text{PORST}}$																
XTAL1									U0C0. DX0F	U0C1. DX0F	U1C0. DX0F	U1C1. DX0F	U2C0. DX0F	U2C1. DX0F		
XTAL2																
RTC_XTAL1											ERU0. 1B1					
RTC_XTAL2																

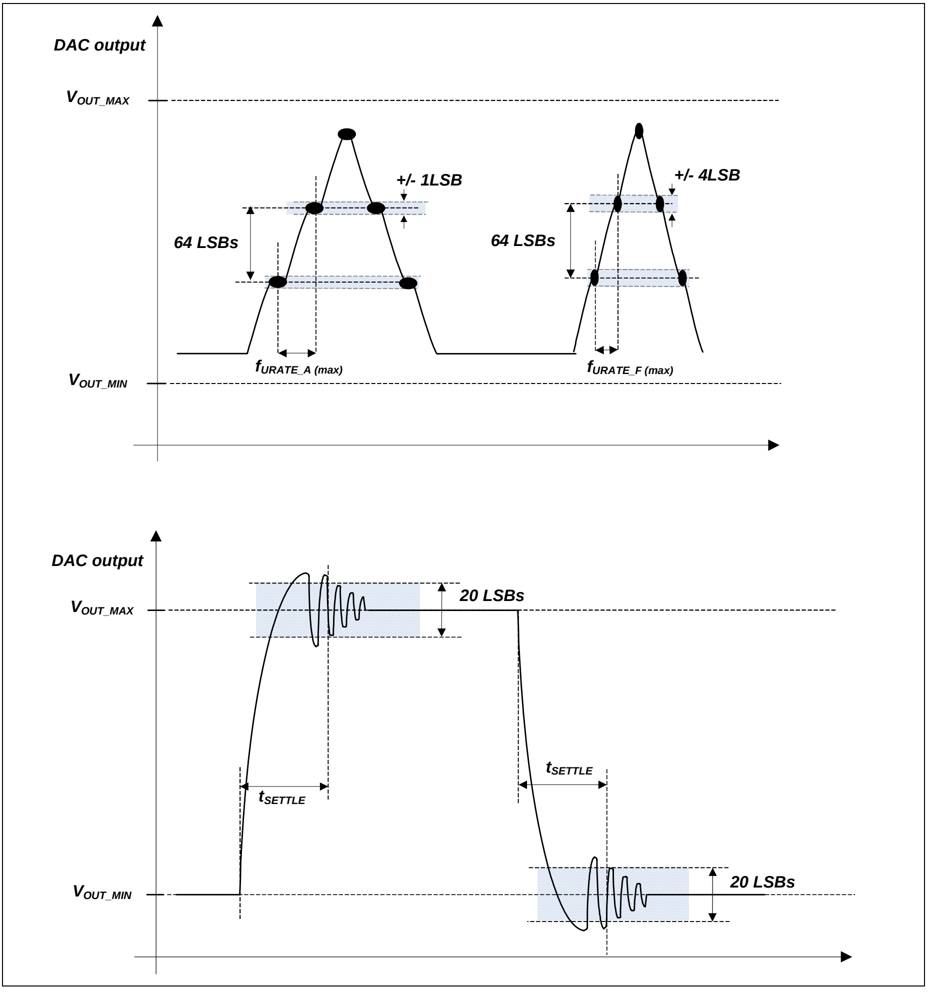


Figure 17 DAC Conversion Examples

Table 32 Power Supply Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sleep supply current[4)] Peripherals disabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPS} CC	–	110	–	mA	120 / 120 / 120
		–	100	–		120 / 60 / 60
		–	77	–		60 / 60 / 120
		–	59	–		24 / 24 / 24
		–	48	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	46	–		100 / 100 / 100
Deep Sleep supply current[5)] Flash in Sleep mode Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPD} CC	–	20	–	mA	24 / 24 / 24
		–	12	–		4 / 4 / 4
		–	10	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	6	–		100 / 100 / 100 [6)]
Hibernate supply current RTC on[7)]	I_{DDPH} CC	–	10	–	μA	V_{BAT} = 3.3 V
		–	7.5	–		V_{BAT} = 2.4 V
		–	6.2	–		V_{BAT} = 2.0 V
Hibernate supply current RTC off[8)]	I_{DDPH} CC	–	9.2	–	μA	V_{BAT} = 3.3 V
		–	6.7	–		V_{BAT} = 2.4 V
		–	5.6	–		V_{BAT} = 2.0 V
Worst case active supply current[9)]	I_{DDPA} CC	–	–	180 [10)]	mA	V_{DDP} = 3.6 V, T_J = 150 °C
V_{DDA} power supply current	I_{DDA} CC	–	–	– [11)]	mA	
I_{DDP} current at $\overline{\text{PORST}}$ Low	I_{DDP_PORST} CC	–	–	16	mA	V_{DDP} = 3.6 V, T_J = 150 °C
Power Dissipation	P_{DISS} CC	–	–	1	W	V_{DDP} = 3.6 V, T_J = 150 °C
Wake-up time from Sleep to Active mode	t_{SSA} CC	–	6	–	cycles	

Table 32 Power Supply Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Wake-up time from Deep Sleep to Active mode		–	–	–	ms	Defined by the wake-up of the Flash module, see **Section 3.2.9**
Wake-up time from Hibernate mode		–	–	–	ms	Wake-up via power-on reset event, see **Section 3.3.2**

1) CPU executing code from Flash, all peripherals idle.
2) CPU executing code from Flash.
3) CPU in sleep, all peripherals idle, Flash in Active mode.
4) CPU in sleep, Flash in Active mode.
5) CPU in sleep, peripherals disabled, after wake-up code execution from RAM.
6) To wake-up the Flash from its Sleep mode, $f_{CPU} \geq 1$ MHz is required.
7) OSC_ULP operating with external crystal on RTC_XTAL
8) OSC_ULP off, Hibernate domain operating with OSC_SI clock
9) Test Power Loop: f_{SYS} = 120 MHz, CPU executing benchmark code from Flash, all CCUs in 100kHz timer mode, all ADC groups in continuous conversion mode, USICs as SPI in internal loop-back mode, CAN in 500kHz internal loop-back mode, interrupt triggered DMA block transfers to parity protected RAMs and FCE, DTS measurements and FPU calculations.
The power consumption of each customer application will most probably be lower than this value, but must be evaluated separately.
10) I_{DDP} decreases typically by approximately 6 mA when f_{SYS} decreases by 10 MHz, at constant T_J
11) Sum of currents of all active converters (ADC and DAC)

3.3.4 Phase Locked Loop (PLL) Characteristics

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Main and USB PLL

Table 36 PLL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Accumulated Jitter	D_P CC	–	–	±5	ns	accumulated over 300 cycles f_{SYS} = 120 MHz
Duty Cycle[1]	D_{DC} CC	46	50	54	%	Low pulse to total period, assuming an ideal input clock source
PLL base frequency	$f_{PLLBASE}$ CC	30	–	140	MHz	
VCO input frequency	f_{REF} CC	4	–	16	MHz	
VCO frequency range	f_{VCO} CC	260	–	520	MHz	
PLL lock-in time	t_L CC	–	–	400	µs	

1) 50% for even K2 divider values, 50±(10/K2) for odd K2 divider values.

3.3.7 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply.

Table 40 SWD Interface Timing Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
SWDCLK clock period	t_{SC}	SR	25	–	–	ns	C_L = 30 pF
			40	–	–	ns	C_L = 50 pF
SWDCLK high time	t_1	SR	10	–	500000	ns	
SWDCLK low time	t_2	SR	10	–	500000	ns	
SWDIO input setup to SWDCLK rising edge	t_3	SR	6	–	–	ns	
SWDIO input hold after SWDCLK rising edge	t_4	SR	6	–	–	ns	
SWDIO output valid time after SWDCLK rising edge	t_5	CC	–	–	17	ns	C_L = 50 pF
			–	–	13	ns	C_L = 30 pF
SWDIO output hold time from SWDCLK rising edge	t_6	CC	3	–	–	ns	

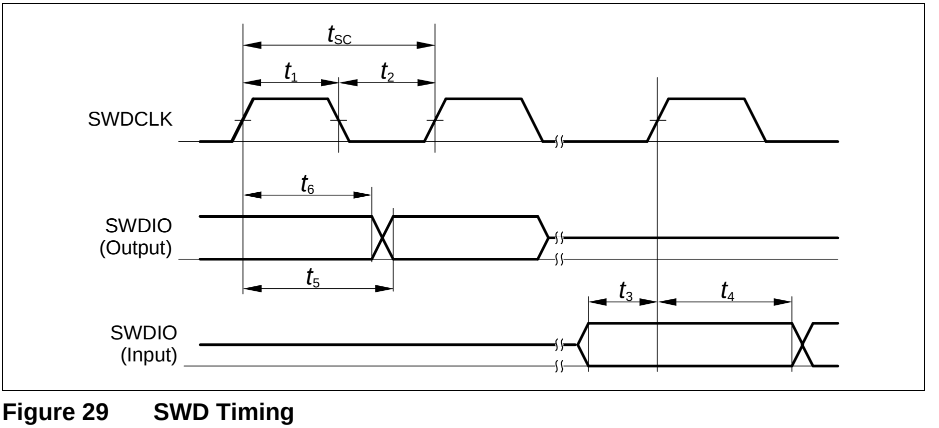


Figure 29 SWD Timing

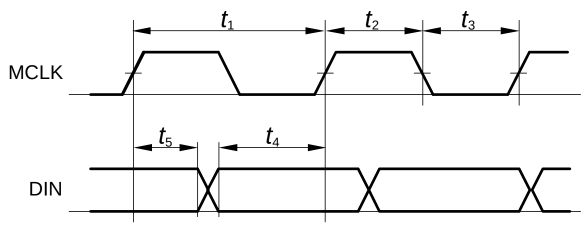


Figure 32 DSD Data Timing

3.3.9.2 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 43 USIC SSC Master Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
SCLKOUT master clock period	t_{CLK}	CC	33.3	–	–	ns	
Slave select output SELO active to first SCLKOUT transmit edge	t_1	CC	t_{PB} - 6.5[1)]	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2	CC	t_{PB} - 8.5[1)]	–	–	ns	
Data output DOUT[3:0] valid time	t_3	CC	-6	–	8	ns	
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	t_4	SR	23	–	–	ns	
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	t_5	SR	1	–	–	ns	

1) $t_{PB} = 1 / f_{PB}$

Table 46 USIC IIC Fast Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	20 + 0.1*C_b [2)]	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	20 + 0.1*C_b [2)]	-	300	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	100	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	1.3	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	0.6	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	0.6	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	0.6	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	0.6	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	1.3	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2) C_b refers to the total capacitance of one bus line in pF.

Multiplexed Write Timing

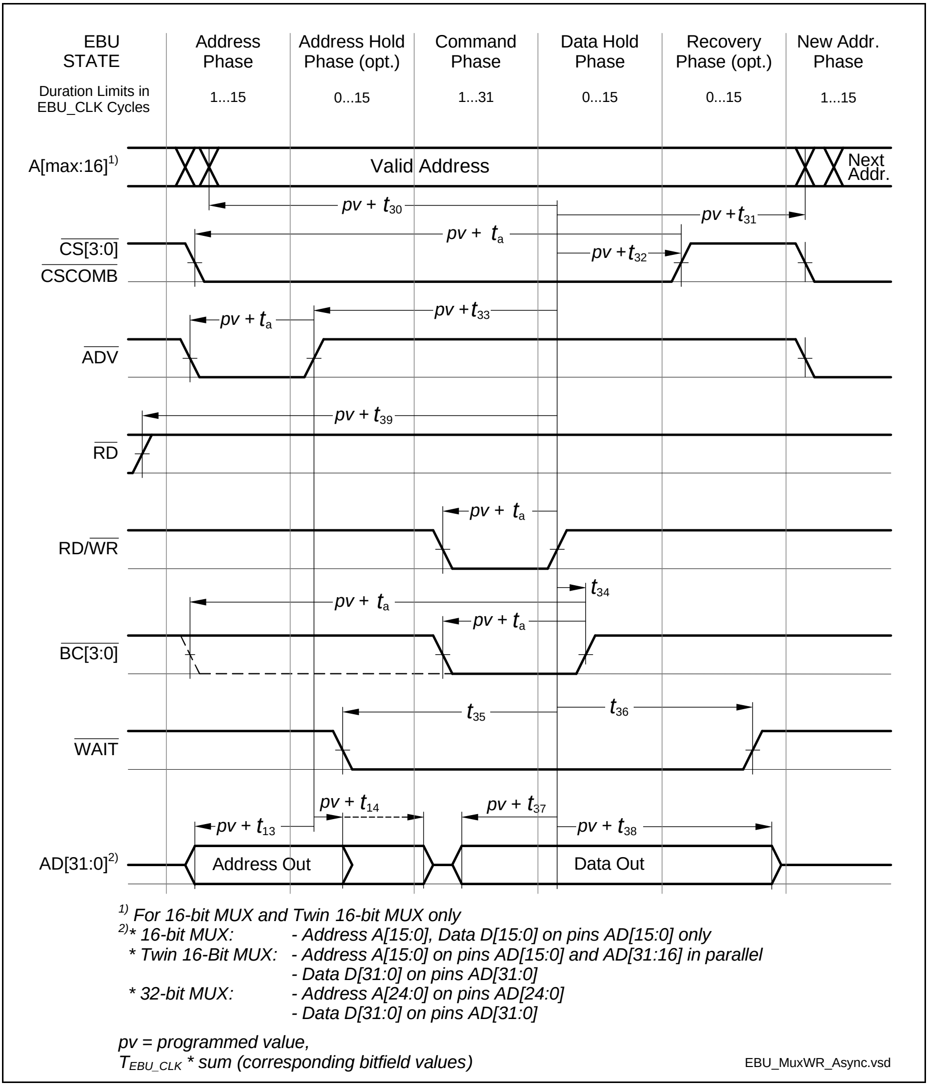
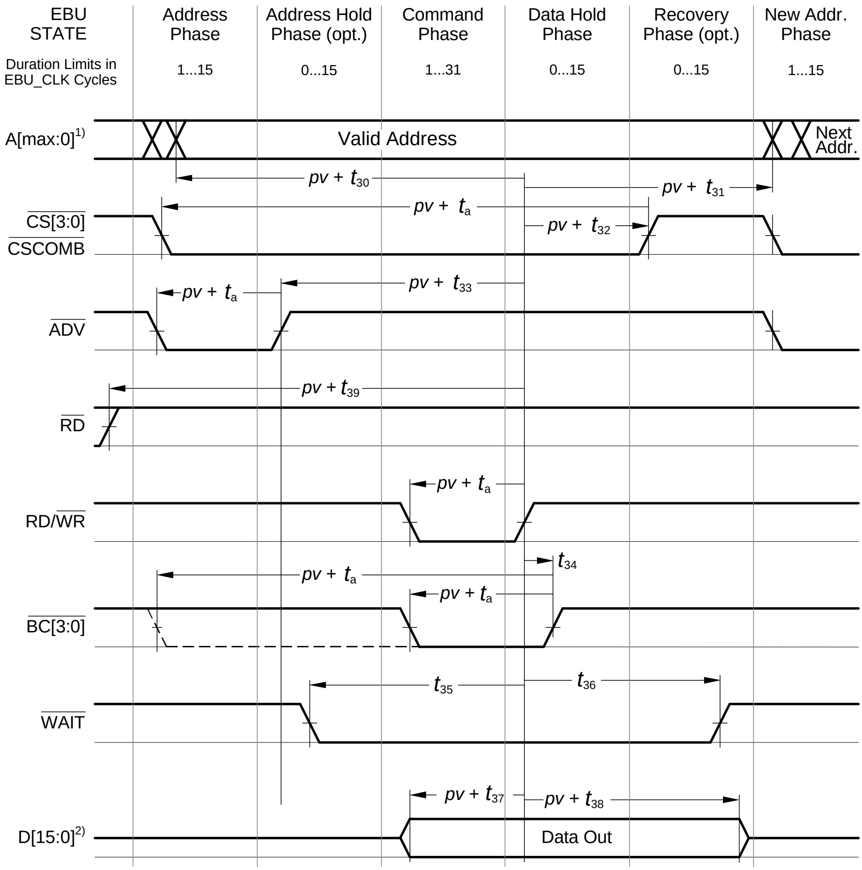


Figure 43 Multiplexed Write Access

Demultiplexed Write Timing



[1] *Address A[max:16] on pins A[max:16], Address A[15:0] on pins AD[31:16]*
[2] *Data D[15:0] on pins AD[15:0]*

pv = programmed value,
*T_{EBU_CLK} * sum (corresponding bitfield values)*

EBU_DeMuxWR_Async.vsd

Figure 44 Demultiplexed Write Access

3) If the clock feedback is not enabled, the input signals are latched using the internal clock in the same way as for asynchronous access. Thus, t_5, t_6, t_7 and t_8 from the asynchronous timing apply.

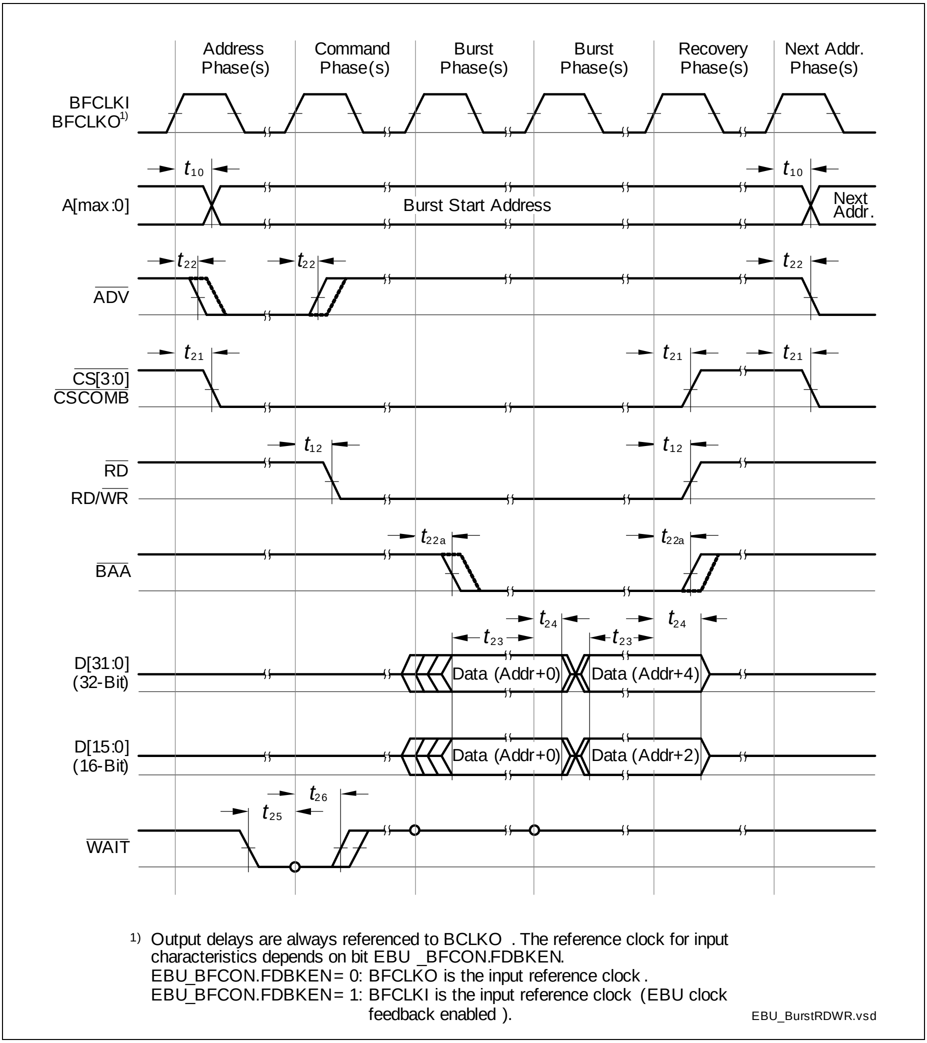


Figure 45 EBU Burst Mode Read / Write Access Timing

3.3.10.3 EBU Arbitration Signal Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 57 EBU Arbitration Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Output delay from BFCLKO rising edge	t_1	CC	–	–	16	ns	C_L = 50 pF
Data setup to BFCLKO falling edge	t_2	SR	11	–	–	ns	–
Data hold from BFCLKO falling edge	t_3	SR	2	–	–	ns	–

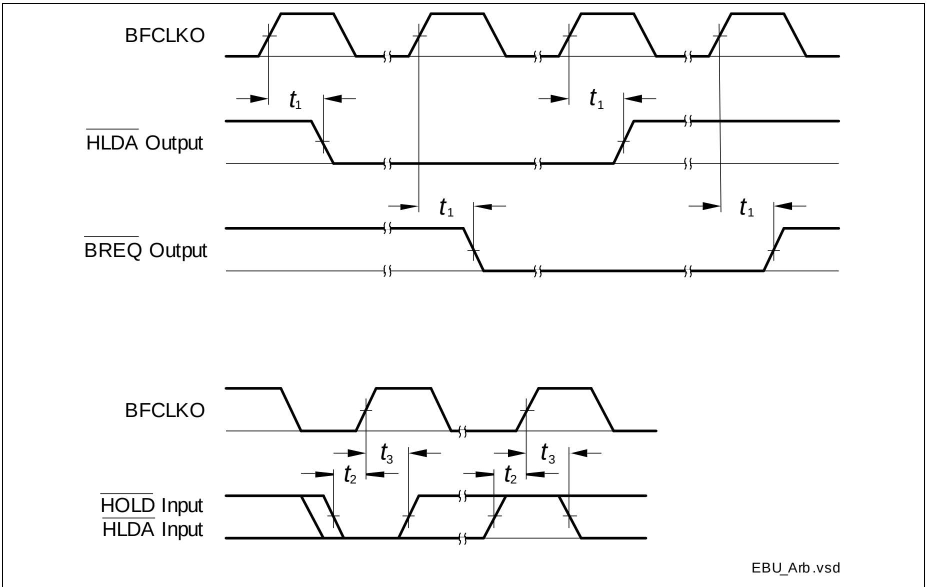


Figure 46 EBU Arbitration Signal Timing

3.3.11 USB Interface Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification and the OTG Specification Rev. 1.3. High-Speed Mode is not supported.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 60 USB Timing Parameters (operating conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Rise time	t_R	CC	4	–	20	ns	C_L = 50 pF
Fall time	t_F	CC	4	–	20	ns	C_L = 50 pF
Rise/Fall time matching	t_R/t_F	CC	90	–	111.11	%	C_L = 50 pF
Crossover voltage	V_{CRS}	CC	1.3	–	2.0	V	C_L = 50 pF

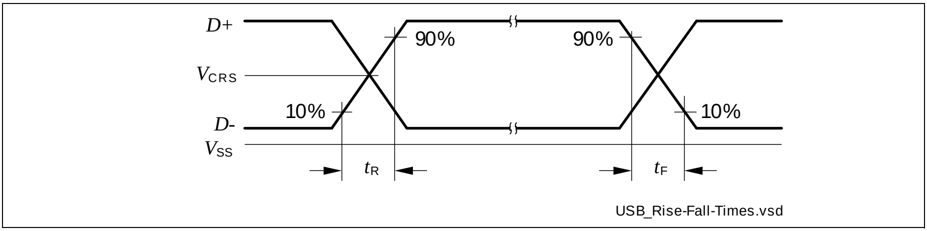


Figure 50 USB Signal Timing

3.3.12 Ethernet Interface (ETH) Characteristics

For proper operation of the Ethernet Interface it is required that $f_{SYS} \geq 100$ MHz.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.3.12.1 ETH Measurement Reference Points

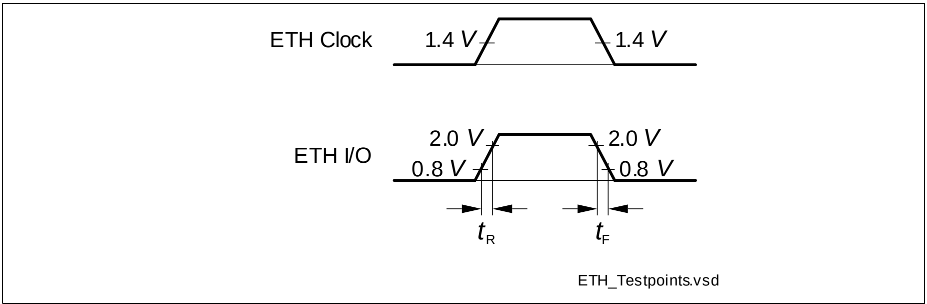


Figure 51 ETH Measurement Reference Points

3.3.12.2 ETH Management Signal Parameters (ETH_MDC, ETH_MDIO)

Table 61 ETH Management Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
ETH_MDC period	t_1	CC	400	–	–	ns	C_L = 25 pF
ETH_MDC high time	t_2	CC	160	–	–	ns	
ETH_MDC low time	t_3	CC	160	–	–	ns	
ETH_MDIO setup time (output)	t_4	CC	10	–	–	ns	
ETH_MDIO hold time (output)	t_5	CC	10	–	–	ns	
ETH_MDIO data valid (input)	t_6	SR	0	–	300	ns	

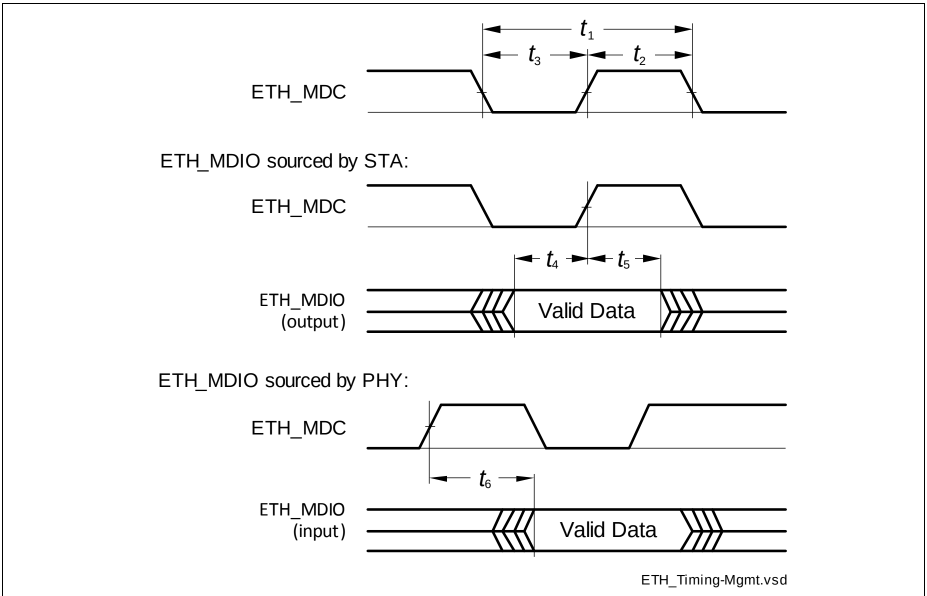


Figure 52 ETH Management Signal Timing

4.2 Package Outlines

Table 65 Differences PG-LQFP-14-18 to PG-LQFP-144-24

Change	PG-LQFP-144-18	PG-LQFP-144-24
Thermal Resistance Junction Ambient ($R_{\Theta JA}$)	22.4 K/W	21.0 K/W
Lead Width	$0.22^{\pm 0.05}$ mm	$0.2^{+0.07}_{-0.03}$ mm
Lead Thickness	$0.15^{+0.05}_{-0.06}$ mm	$0.127^{+0.073}_{-0.037}$ mm
Exposed Die Pad outer dimensions	6.5 mm × 6.5 mm	6.5 mm × 6.5 mm
Exposed Die Pad U-Groove inner dimensions	n.a.	5.7 mm × 5.7 mm

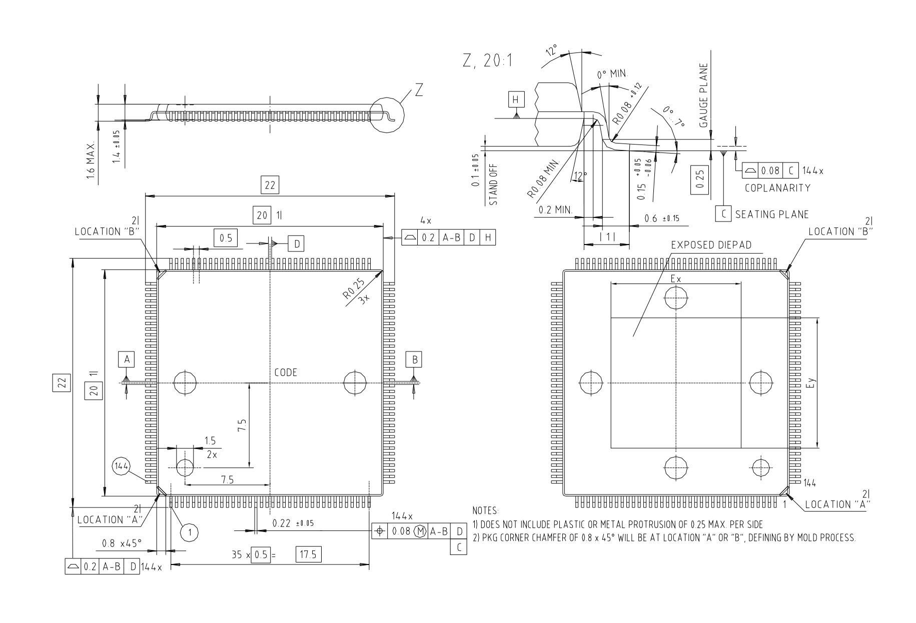
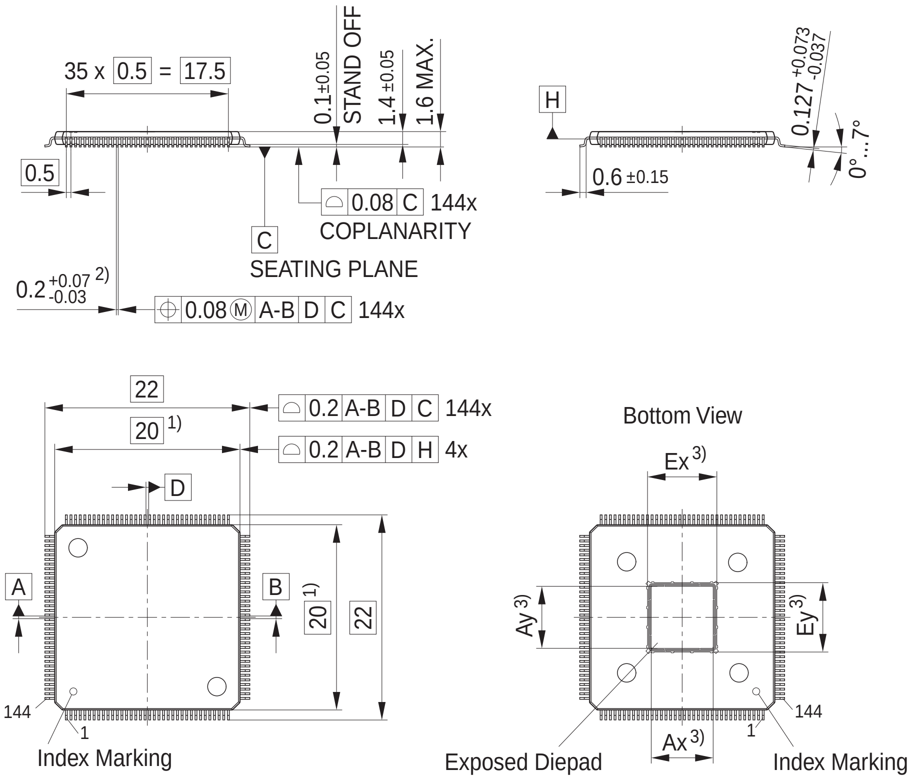


Figure 55 PG-LQFP-144-18 (Plastic Green Low Profile Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side
2) Does not include dambar protrusion
3) Refer table for exposed pad dimension

PG-LQFP-144-22-PO V04

Figure 56 **PG-LQFP-144-24** (Plastic Green Low Profile Quad Flat Package)