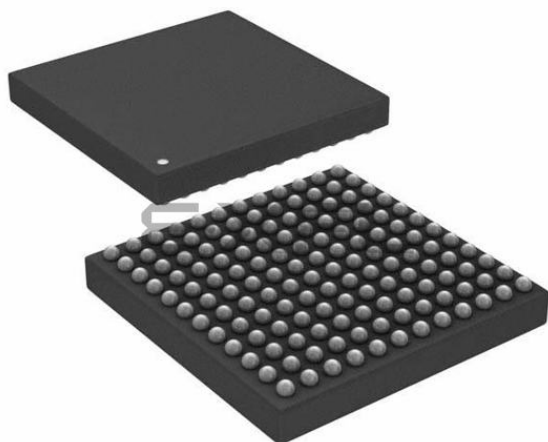




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, SPI, UART, USB
Peripherals	DMA, I ² S, LED, POR, PWM, WDT
Number of I/O	91
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	PG-LFBGA-144-10
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4500e144f1024acxqsa1

Input/Output Lines

- Programmable port driver control module (PORTS)
- Individual bit addressability
- Tri-stated in input mode
- Push/pull or open drain output mode
- Boundary scan test support over JTAG interface

On-Chip Debug Support

- Full support for debug features: 8 breakpoints, CoreSight, trace
- Various interfaces: ARM-JTAG, SWD, single wire trace

1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code "XMC4<DDD>-<Z><PPP><T><FFFF>" identifies:

- <DDD> the derivatives function set
- <Z> the package variant
 - E: LFBGA
 - F: LQFP
 - Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
 - F: -40°C to 85°C
 - X: -40°C to 105°C
 - K: -40°C to 125°C
- <FFFF> the Flash memory size.

For ordering codes for the XMC4500 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC4500 series, some descriptions may not apply to a specific product.

For simplicity the term **XMC4500** is used for all derivatives throughout this document.

Summary of Features

1.2 Device Types

These device types are available and can be ordered through Infineon's direct and/or distribution channels.

Table 1 Synopsis of XMC4500 Device Types

Derivative ¹⁾	Package	Flash Kbytes	SRAM Kbytes
XMC4500-E144x1024	PG-LFBGA-144	1024	160
XMC4500-F144x1024	PG-LQFP-144	1024	160
XMC4500-F100x1024	PG-LQFP-100	1024	160
XMC4500-F144x768	PG-LQFP-144	768	160
XMC4500-F100x768	PG-LQFP-100	768	160
XMC4502-F100x768	PG-LQFP-100	768	160
XMC4504-F144x512	PG-LQFP-144	512	128
XMC4504-F100x512	PG-LQFP-100	512	128

1) x is a placeholder for the supported temperature range.

1.3 Device Type Features

The following table lists the available features per device type.

Table 2 Features of XMC4500 Device Types

Derivative ¹⁾	LEDTS Intf.	SDMMC Intf.	EBU Intf. ²⁾	ETH Intf. ³⁾	USB Intf.	USIC Chan.	MultiCAN Nodes, MO
XMC4500-E144x1024	1	1	SDM	MR	1	3 x 2	N0, N1, N2 MO[0..63]
XMC4500-F144x1024	1	1	SDM	MR	1	3 x 2	N0, N1, N2 MO[0..63]
XMC4500-F100x1024	1	1	M16	R	1	3 x 2	N0, N1, N2 MO[0..63]
XMC4500-F144x768	1	1	SDM	MR	1	3 x 2	N0, N1, N2 MO[0..63]
XMC4500-F100x768	1	1	M16	R	1	3 x 2	N0, N1, N2 MO[0..63]
XMC4502-F100x768	1	1	M16	-	1	3 x 2	N0, N1, N2 MO[0..63]

Summary of Features
Table 4 Flash Memory Ranges (cont'd)

Total Flash Size	Cached Range	Uncached Range
768 Kbytes	0800 0000 _H – 080B FFFF _H	0C00 0000 _H – 0C0B FFFF _H
1,024 Kbytes	0800 0000 _H – 080F FFFF _H	0C00 0000 _H – 0C0F FFFF _H

Table 5 SRAM Memory Ranges

Total SRAM Size	Program SRAM	System Data SRAM	Communication Data SRAM
128 Kbytes	1000 0000 _H – 1000 FFFF _H	2000 0000 _H – 2000 FFFF _H	–
160 Kbytes	1000 0000 _H – 1000 FFFF _H	2000 0000 _H – 2000 FFFF _H	3000 0000 _H – 3000 7FFF _H

Table 6 ADC Channels¹⁾

Package	VADC G0	VADC G1	VADC G2	VADC G3
PG-LQFP-144 PG-LFBGA-144	CH0..CH7	CH0..CH7	CH0..CH7	CH0..CH7
PG-LQFP-100	CH0..CH7	CH0..CH7	CH0..CH3	CH0..CH3

1) Some pins in a package may be connected to more than one channel. For the detailed mapping see the Port I/O Function table.

1.5 Identification Registers

The identification registers allow software to identify the marking.

Table 7 XMC4500 Identification Registers

Register Name	Value	Marking
SCU_IDCHIP	0004 5002 _H	EES-AA, ES-AA
SCU_IDCHIP	0004 5003 _H	ES-AB, AB
SCU_IDCHIP	0004 5004 _H	AC
JTAG IDCODE	101D B083 _H	EES-AA, ES-AA
JTAG IDCODE	101D B083 _H	ES-AB, AB
JTAG IDCODE	401D B083 _H	AC

General Device Information

	1	2	3	4	5	6	7	8	9	10	11	12	
A	VSS	VDDC	P0.2	P0.3	P0.5	P0.6	P3.6	P0.8	P4.1	P1.8	VDDP	VSS	A
B	VDDP	P3.1	P3.2	P0.10	P0.4	P3.5	P0.7	P4.0	P1.6	P1.7	P1.9	VDDC	B
C	P3.0	P3.13	P0.1	P0.0	P0.13	P0.15	P4.4	P4.6	P4.7	P1.4	P1.2	P1.3	C
D	USB_D M	P3.12	P3.11	P0.9	P0.12	P3.14	P3.15	P4.5	P1.0	P1.5	P1.11	P1.10	D
E	USB_D P	VBUS	P3.8	P3.7	P0.11	P0.14	P3.4	P4.2	P1.1	P1.14	P1.12	P1.13	E
F	RTC_X TAL2	RTC_X TAL1	HIB_I O_1	HIB_I O_0	P3.9	P3.10	P3.3	P4.3	P6.1	P6.4	P6.5	P6.6	F
G	VBAT	P15.3	P15.5	P15.4	P15.6	P15.7	TMS	TCK	P6.3	P6.0	PORST	P1.15	G
H	P15.2	P14.15	P14.14	P14.13	P5.10	P5.8	P5.2	P5.1	P5.0	P6.2	XTAL1	XTAL2	H
J	P14.12	P14.7	P14.6	P14.3	P5.11	P2.15	P5.7	P5.5	P2.6	P5.3	P2.0	VSSO	J
K	P14.4	P14.5	P14.2	P15.15	P15.12	P5.9	P2.14	P5.6	P2.7	P5.4	P2.2	P2.1	K
L	VDDA	P14.1	P14.0	P15.14	P14.9	P15.9	P2.12	P2.10	P2.8	P2.4	P2.3	VDDP	L
M	VSSA	VAGND	VAREF	P15.13	P14.8	P15.8	P2.13	P2.11	P2.9	P2.5	VDDC	VSS	M
	1	2	3	4	5	6	7	8	9	10	11	12	

XMC4500- (top view)

Figure 6 XMC4500 PG-LFBGA-144 Pin Configuration (top view)

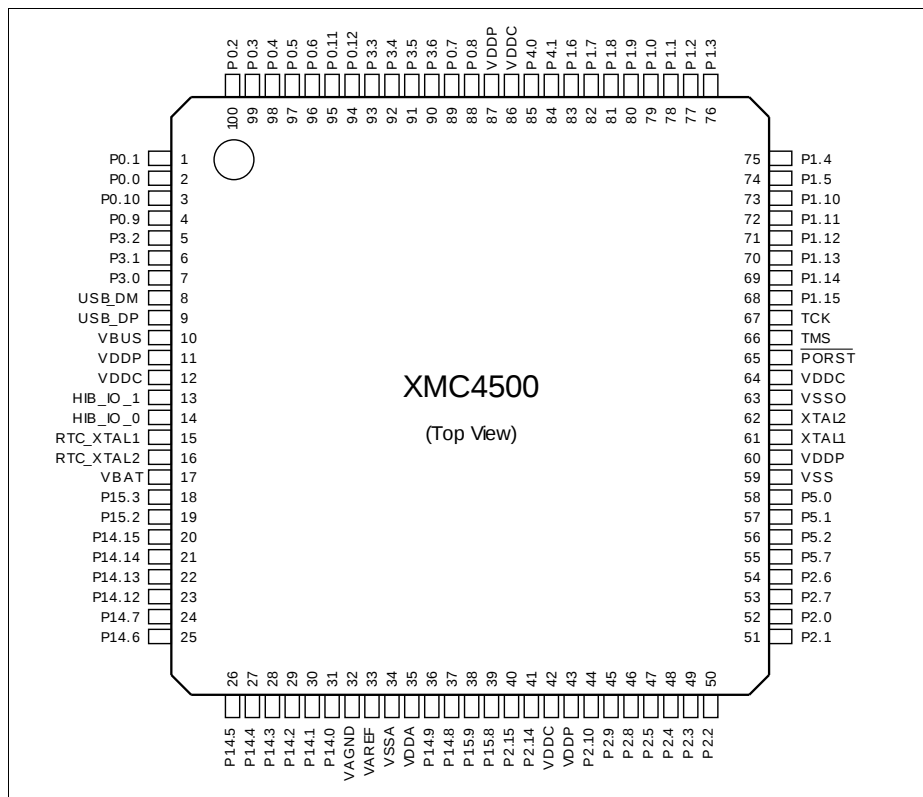


Figure 7 XMC4500 PG-LQFP-100 Pin Configuration (top view)

General Device Information
Table 9 Package Pin Mapping (cont'd)

Function	LQFP-144	LFBGA-144	LQFP-100	Pad Type	Notes
RTC_XTAL1	22	F2	15	clock_IN	
RTC_XTAL2	23	F1	16	clock_O	
VBAT	24	G1	17	Power	When VDDP is supplied VBAT has to be supplied as well.
VBUS	17	E2	10	special	
VAREF	46	M3	33	AN_Ref	
VAGND	45	M2	32	AN_Ref	
VDDA	48	L1	35	AN_Power	
VSSA	47	M1	34	AN_Power	
VDDC	19	-	12	Power	
VDDC	61	-	42	Power	
VDDC	90	-	64	Power	
VDDC	125	-	86	Power	
VDDC	-	A2	-	Power	
VDDC	-	B12	-	Power	
VDDC	-	M11	-	Power	
VDDP	18	-	11	Power	
VDDP	62	-	43	Power	
VDDP	86	-	60	Power	
VDDP	126	-	87	Power	
VDDP	-	A11	-	Power	
VDDP	-	B1	-	Power	
VDDP	-	L12	-	Power	
VSS	85	-	59	Power	
VSS	-	A1	-	Power	
VSS	-	A12	-	Power	
VSS	-	M12	-	Power	

Table 11 Port I/O Functions (cont'd)

Function	Outputs						Inputs								
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input
P15.12												VADC_G3CH4			
P15.13												VADC_G3CH5			
P15.14												VADC_G3CH6			
P15.15												VADC_G3CH7			
USB_DP															
USB_DM															
HIB_IO_0	HIBOUT	WWDT_SERVICE_OUT							WAKEUPA						
HIB_IO_1	HIBOUT	WWDT_SERVICE_OUT							WAKEUPB						
TCK							DB.TCK/ SWCLK								
TMS					DB.TMS/ SWDIO										
PORST															
XTAL1									U0C0. DX0F	U0C1. DX0F	U1C0. DX0F	U1C1. DX0F	U2C0. DX0F	U2C1. DX0F	
XTAL2															
RTC_XTAL1											ERU0. 1B1				
RTC_XTAL2															

2.3 Power Connection Scheme

Figure 9. shows a reference power connection scheme for the XMC4500.

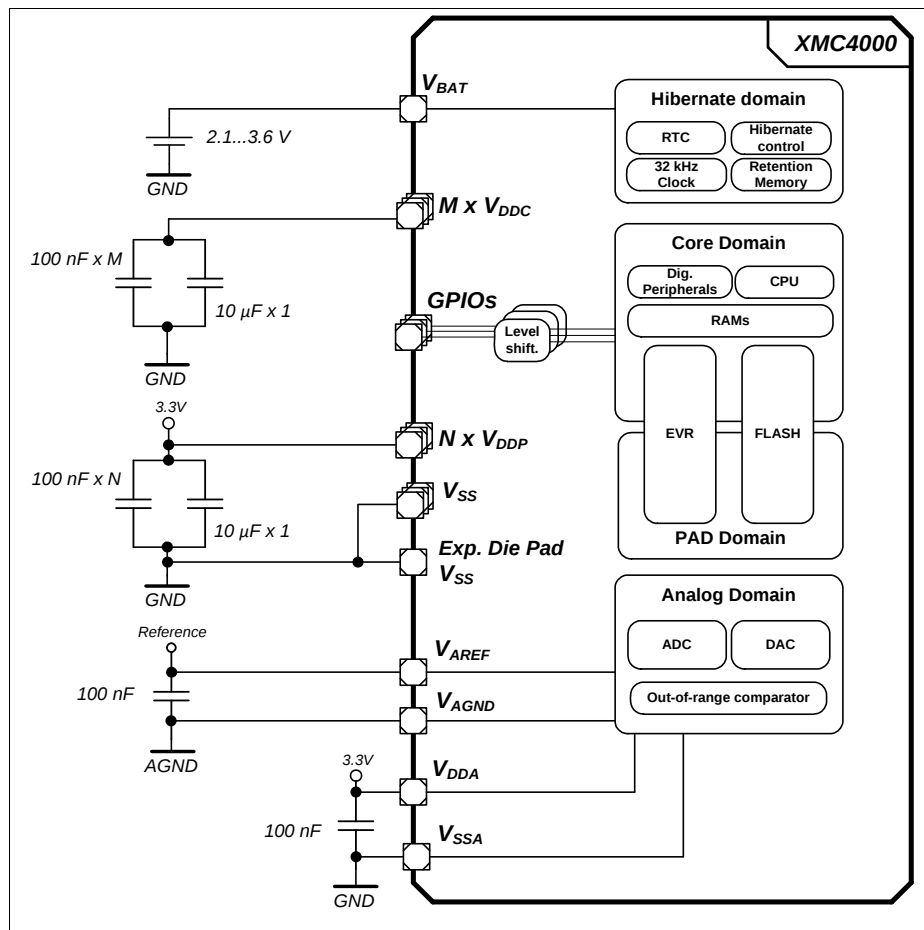


Figure 9 Power Connection Scheme

Every power supply pin needs to be connected. Different pins of the same supply need also to be externally connected. As example, all V_{DDP} pins must be connected externally to one V_{DDP} net. In this reference scheme one 100 nF capacitor is connected at each supply pin against V_{SS} . An additional 10 μF capacitor is connected to the V_{DDP} nets and an additional 10 μF capacitor to the V_{DDC} nets.

3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 12 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Storage temperature	T_{ST}	SR	-65	–	150	°C	–
Junction temperature	T_J	SR	-40	–	150	°C	–
Voltage at 3.3 V power supply pins with respect to V_{SS}	V_{DDP}	SR	–	–	4.3	V	–
Voltage on any Class A and dedicated input pin with respect to V_{SS}	V_{IN}	SR	-1.0	–	$V_{DDP} + 1.0$ or max. 4.3	V	whichever is lower
Voltage on any analog input pin with respect to V_{AGND}	V_{AIN} V_{AREF}	SR	-1.0	–	$V_{DDP} + 1.0$ or max. 4.3	V	whichever is lower
Input current on any pin during overload condition	I_{IN}	SR	-10	–	+10	mA	
Absolute maximum sum of all input circuit currents for one port group during overload condition ¹⁾	ΣI_{IN}	SR	-25	–	+25	mA	
Absolute maximum sum of all input circuit currents during overload condition	ΣI_{IN}	SR	-100	–	+100	mA	

1) The port groups are defined in [Table 16](#).

Figure 10 explains the input voltage ranges of V_{IN} and V_{AIN} and its dependency to the supply level of V_{DDP} . The input voltage must not exceed 4.3 V, and it must not be more than 1.0 V above V_{DDP} . For the range up to $V_{DDP} + 1.0$ V also see the definition of the overload conditions in [Section 3.1.3](#).

Table 20 Standard Pads Class_A1

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Input leakage current	I_{OZA1} CC	-500	500	nA	$0\text{ V} \leq V_{IN} \leq V_{DDP}$
Input high voltage	V_{IHA1} SR	$0.6 \times V_{DDP}$	$V_{DDP} + 0.3$	V	max. 3.6 V
Input low voltage	V_{ILA1} SR	-0.3	$0.36 \times V_{DDP}$	V	
Output high voltage, POD ¹⁾ = weak	V_{OHA1} CC	$V_{DDP} - 0.4$	–	V	$I_{OH} \geq -400\text{ }\mu\text{A}$
		2.4	–	V	$I_{OH} \geq -500\text{ }\mu\text{A}$
$V_{DDP} - 0.4$		–	V	$I_{OH} \geq -1.4\text{ mA}$	
2.4		–	V	$I_{OH} \geq -2\text{ mA}$	
Output low voltage	V_{OLA1} CC	–	0.4	V	$I_{OL} \leq 500\text{ }\mu\text{A}$; POD ¹⁾ = weak
		–	0.4	V	$I_{OL} \leq 2\text{ mA}$; POD ¹⁾ = medium
Fall time	t_{FA1} CC	–	150	ns	$C_L = 20\text{ pF}$; POD ¹⁾ = weak
		–	50	ns	$C_L = 50\text{ pF}$; POD ¹⁾ = medium
Rise time	t_{RA1} CC	–	150	ns	$C_L = 20\text{ pF}$; POD ¹⁾ = weak
		–	50	ns	$C_L = 50\text{ pF}$; POD ¹⁾ = medium

1) POD = Pin Out Driver

Table 21 Standard Pads Class_A1+

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Input leakage current	I_{OZA1+} CC	-1	1	μA	$0\text{ V} \leq V_{IN} \leq V_{DDP}$
Input high voltage	V_{IHA1+} SR	$0.6 \times V_{DDP}$	$V_{DDP} + 0.3$	V	max. 3.6 V
Input low voltage	V_{ILA1+} SR	-0.3	$0.36 \times V_{DDP}$	V	

Table 30 OSC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{OSC} SR	4	–	40	MHz	Direct Input Mode selected
		4	–	25	MHz	External Crystal Mode selected
Oscillator start-up time ¹⁾²⁾	t_{OSCS} CC	–	–	10	ms	
Input voltage at XTAL1	V_{IX} SR	-0.5	–	$V_{\text{DDP}} + 0.5$	V	
Input amplitude (peak-to-peak) at XTAL1 ²⁾³⁾	V_{PPX} SR	$0.4 \times V_{\text{DDP}}$	–	$V_{\text{DDP}} + 1.0$	V	
Input high voltage at XTAL1 ⁴⁾	V_{IHBX} SR	1.0	–	$V_{\text{DDP}} + 0.5$	V	
Input low voltage at XTAL1 ⁴⁾	V_{ILBX} SR	-0.5	–	0.4	V	
Input leakage current at XTAL1	I_{ILX1} CC	-100	–	100	nA	Oscillator power down $0 \text{ V} \leq V_{\text{IX}} \leq V_{\text{DDP}}$

1) t_{OSCS} is defined from the moment the oscillator is enabled with SCU_OSCHPCTRL.MODE until the oscillations reach an amplitude at XTAL1 of $0.4 \times V_{\text{DDP}}$.

2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.

3) If the shaper unit is enabled and not bypassed.

4) If the shaper unit is bypassed, dedicated DC-thresholds have to be met.

3.2.9 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 33 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Erase Time per 256 Kbyte Sector	t_{ERP} CC	–	5	5.5	s	
Erase Time per 64 Kbyte Sector	t_{ERP} CC	–	1.2	1.4	s	
Erase Time per 16 Kbyte Logical Sector	t_{ERP} CC	–	0.3	0.4	s	
Program time per page ¹⁾	t_{PRP} CC	–	5.5	11	ms	
Erase suspend delay	$t_{\text{FL_ErSusp}}$ CC	–	–	15	ms	
Wait time after margin change	$t_{\text{FL_Margin Del}}$ CC	10	–	–	μs	
Wake-up time	t_{WU} CC	–	–	270	μs	
Read access time	t_{a} CC	22	–	–	ns	For operation with $1 / f_{\text{CPU}} < t_{\text{a}}$ wait states must be configured ²⁾
Data Retention Time, Physical Sector ³⁾⁴⁾	t_{RET} CC	20	–	–	years	Max. 1000 erase/program cycles
Data Retention Time, Logical Sector ³⁾⁴⁾	t_{RETL} CC	20	–	–	years	Max. 100 erase/program cycles
Data Retention Time, User Configuration Block (UCB) ³⁾⁴⁾	t_{RTU} CC	20	–	–	years	Max. 4 erase/program cycles per UCB

1) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes an additional time of 5.5 ms.

2) The following formula applies to the wait state configuration: $\text{FCON.WSPFLASH} \times (1 / f_{\text{CPU}}) \geq t_{\text{a}}$.

3) Storage and inactive time included.

4) Values given are valid for an average weighted junction temperature of $T_{\text{J}} = 110^{\circ}\text{C}$.

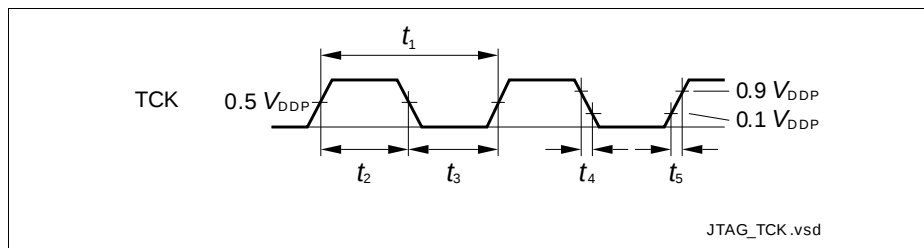


Figure 27 Test Clock Timing (TCK)

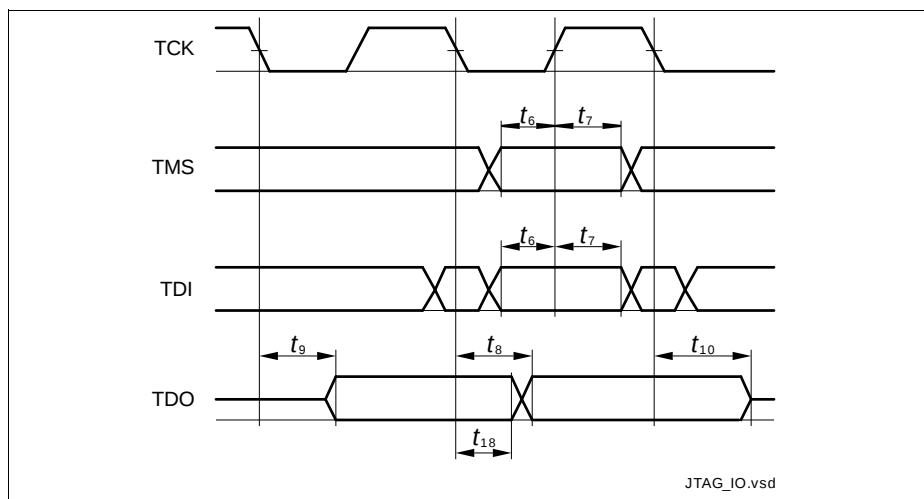


Figure 28 JTAG Timing

Table 46 USIC IIC Fast Mode Timing¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	$20 + 0.1 \cdot C_b$ 2)	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	$20 + 0.1 \cdot C_b$ 2)	-	300	ns	
Data hold time	t_3 CC/SR	0	-	-	μs	
Data set-up time	t_4 CC/SR	100	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	1.3	-	-	μs	
HIGH period of SCL clock	t_6 CC/SR	0.6	-	-	μs	
Hold time for (repeated) START condition	t_7 CC/SR	0.6	-	-	μs	
Set-up time for repeated START condition	t_8 CC/SR	0.6	-	-	μs	
Set-up time for STOP condition	t_9 CC/SR	0.6	-	-	μs	
Bus free time between a STOP and START condition	t_{10} CC/SR	1.3	-	-	μs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2) C_b refers to the total capacitance of one bus line in pF.

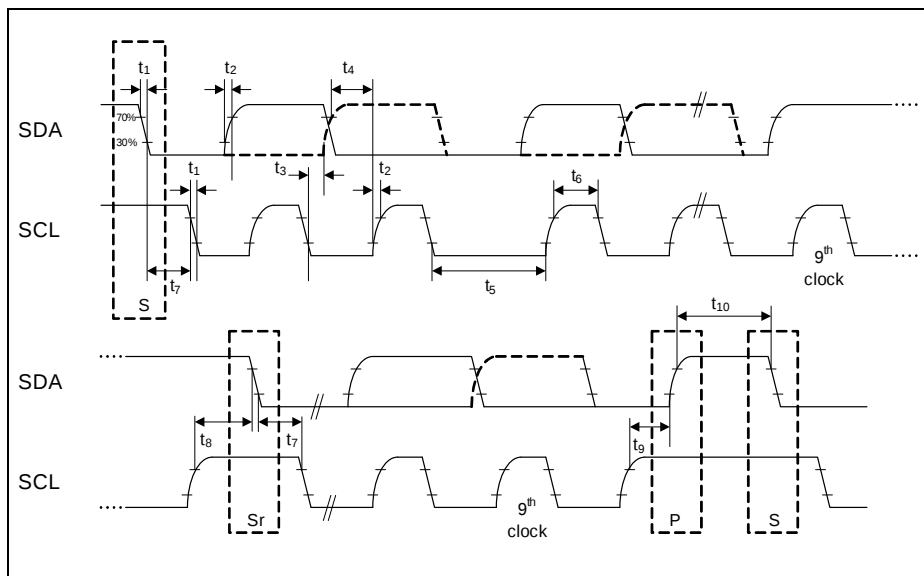


Figure 34 USIC IIC Stand and Fast Mode Timing

3.3.9.4 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 47 USIC IIS Master Transmitter Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_1 CC	33.3	—	—	ns	
Clock high time	t_2 CC	$0.35 \times t_{1min}$	—	—	ns	
Clock low time	t_3 CC	$0.35 \times t_{1min}$	—	—	ns	
Hold time	t_4 CC	0	—	—	ns	
Clock rise time	t_5 CC	—	—	$0.15 \times t_{1min}$	ns	

Table 50 SD Card Bus Timing for Full-Speed Mode¹⁾ (cont'd)

Parameter	Symbol	Values		Unit	Note/ Test Condition
		Min.	Max.		
SD card output valid time	t_{ODLY}	—	14	ns	
SD card output hold time	t_{OH}	0	—	ns	

1) Reference card timing values for calculation examples. Not subject to production test and not characterized.

Full-Speed Output Path (Write)

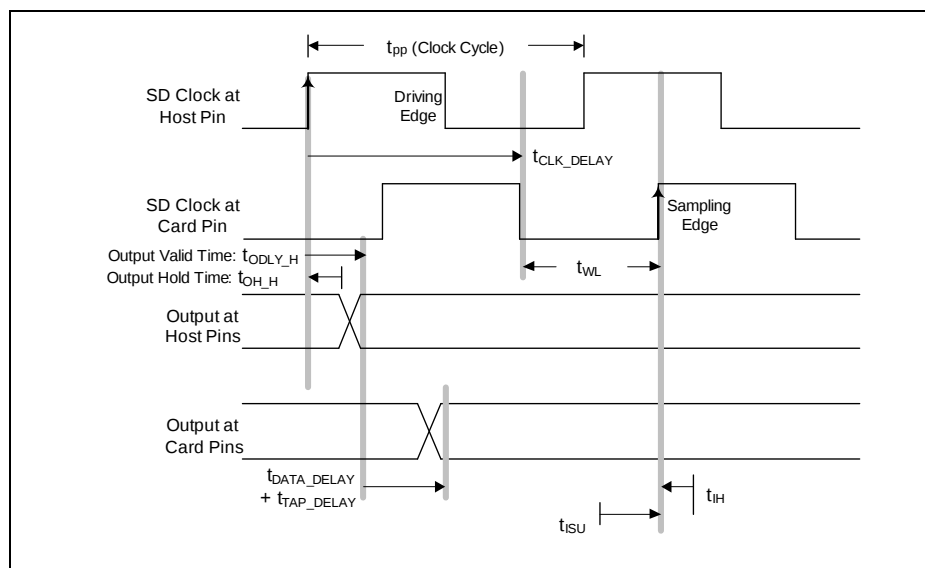


Figure 37 Full-Speed Output Path

Full-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

No clock delay:

(1)

$$t_{ODLY_F} + t_{DATA_DELAY} + t_{TAP_DELAY} + t_{ISU} < t_{WL}$$

3.3.10.4 EBU SDRAM Access Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply, with Class A2 pins and $C_L = 16\text{ pF}$.

Table 58 EBU SDRAM Access SDCLKO Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
SDCLKO period	t_1	CC	12.5	—	—	ns	—
SDCLKO high time	t_2	SR	5.5	—	—	ns	—
SDCLKO low time	t_3	SR	3.75	—	—	ns	—
SDCLKO rise time	t_4	SR	—	—	3.0	ns	—
SDCLKO fall time	t_5	SR	—	—	3.0	ns	—

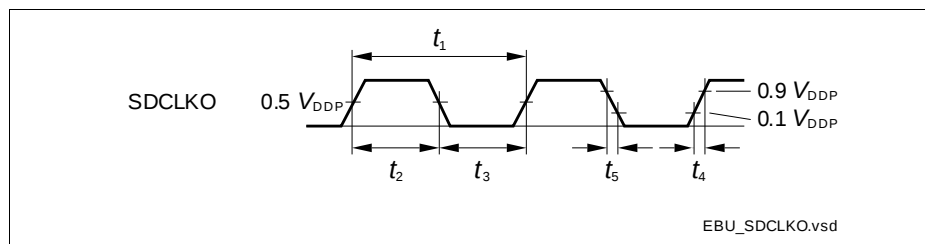


Figure 47 EBU SDRAM Access CLKOUT Timing

3.3.12.3 ETH MII Parameters

In the following, the parameters of the MII (Media Independent Interface) are described.

Table 62 ETH MII Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Clock period, 10 Mbps	t_7	SR	400	–	–	ns	$C_L = 25 \text{ pF}$
Clock high time, 10 Mbps	t_8	SR	140	–	260	ns	
Clock low time, 10 Mbps	t_9	SR	140	–	260	ns	
Clock period, 100 Mbps	t_7	SR	40	–	–	ns	
Clock high time, 100 Mbps	t_8	SR	14	–	26	ns	
Clock low time, 100 Mbps	t_9	SR	14	–	26	ns	
Input setup time	t_{10}	SR	10	–	–	ns	
Input hold time	t_{11}	SR	10	–	–	ns	
Output valid time	t_{12}	CC	0	–	25	ns	

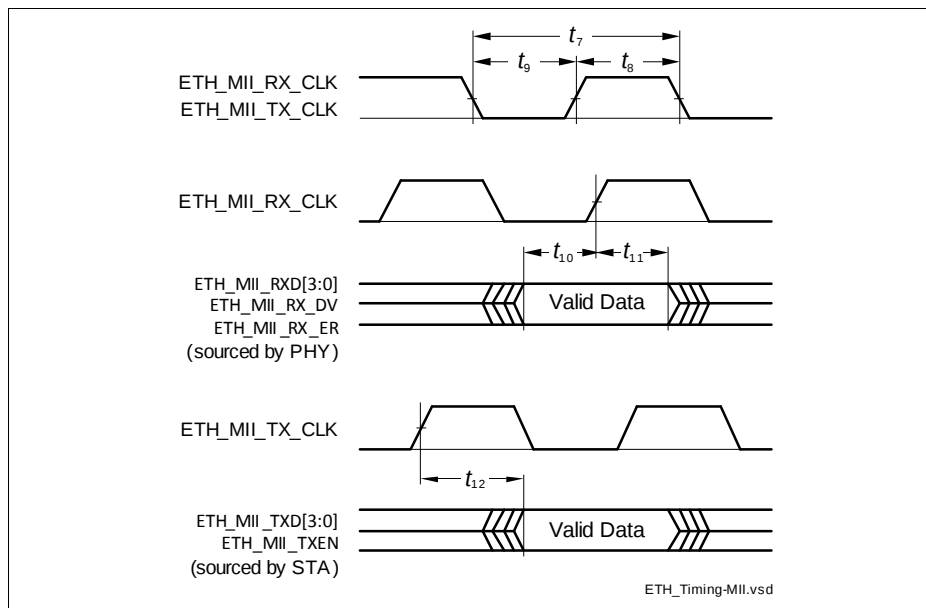


Figure 53 ETH MII Signal Timing

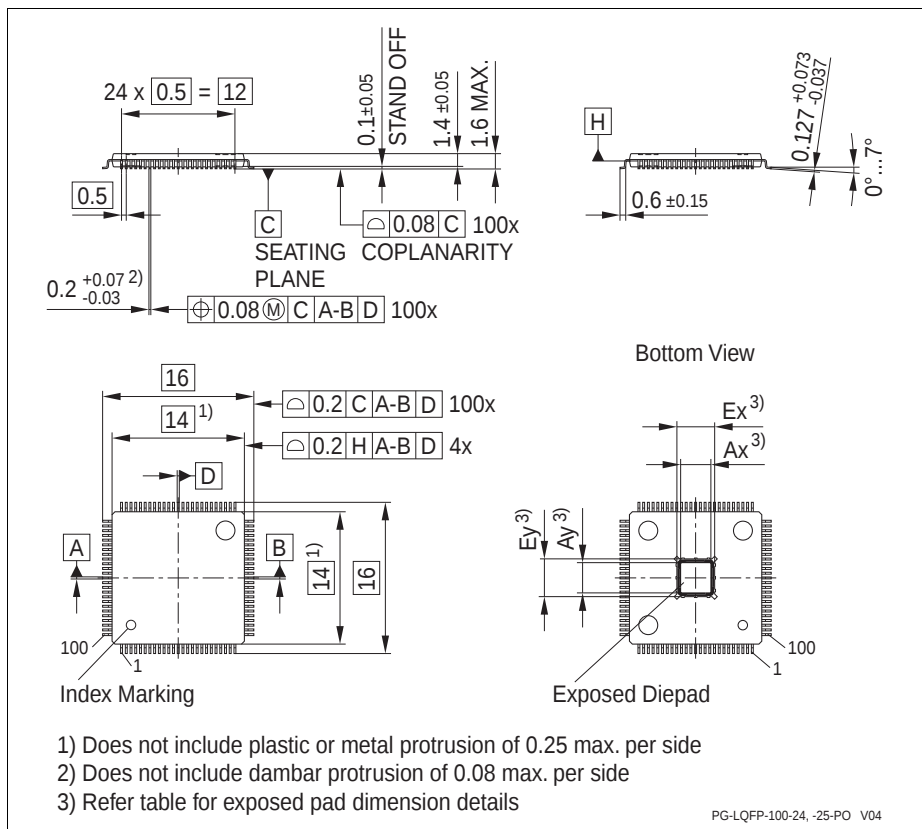


Figure 58 PG-LQFP-100-25 (Plastic Green Low Profile Quad Flat Package)

4.3 Quality Declarations

The qualification of the XMC4500 is executed according to the JEDEC standard JESD47H.

Note: For automotive applications refer to the Infineon automotive microcontrollers.

Table 67 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation lifetime	t_{OP} CC	20	–	–	a	$T_J \leq 109^\circ\text{C}$, device permanent on
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	–	–	2 000	V	EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM} SR	–	–	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	–	–	3	–	JEDEC J-STD-020D
Soldering temperature	T_{SDR} SR	–	–	260	$^\circ\text{C}$	Profile according to JEDEC J-STD-020D