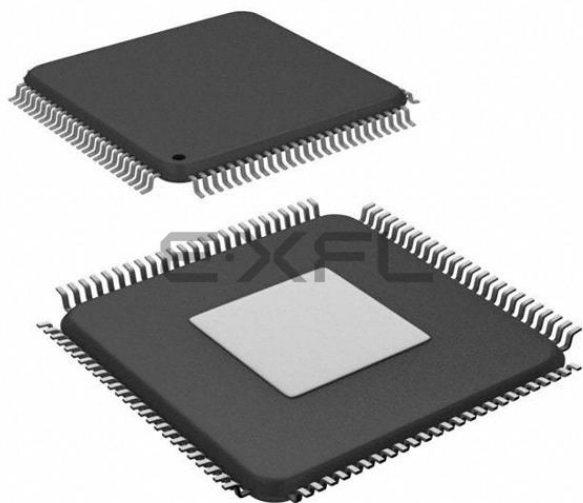




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Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, SPI, UART, USB
Peripherals	DMA, I ² S, LED, POR, PWM, WDT
Number of I/O	55
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-11
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4500f100f1024acxqma1

Summary of Features

- Flexible CRC Engine (FCE) for multiple bit error detection

On-Chip Memories

- 16 KB on-chip boot ROM
- 64 KB on-chip high-speed program memory
- 64 KB on-chip high speed data memory
- 32 KB on-chip high-speed communication
- 1024 KB on-chip Flash Memory with 4 KB instruction cache

Communication Peripherals

- Ethernet MAC module capable of 10/100 Mbit/s transfer rates
- Universal Serial Bus, USB 2.0 host, Full-Speed OTG, with integrated PHY
- Controller Area Network interface (MultiCAN), Full-CAN/Basic-CAN with 3 nodes, 64 message objects (MO), data rate up to 1MBit/s
- Six Universal Serial Interface Channels (USIC), providing 6 serial channels, usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces
- LED and Touch-Sense Controller (LEDTS) for Human-Machine interface
- SD and Multi-Media Card interface (SDMMC) for data storage memory cards
- External Bus Interface Unit (EBU) enabling communication with external memories and off-chip peripherals

Analog Frontend Peripherals

- Four Analog-Digital Converters (VADC) of 12-bit resolution, 8 channels each, with input out-of-range comparators
- Delta Sigma Demodulator with four channels, digital input stage for A/D signal conversion
- Digital-Analogue Converter (DAC) with two channels of 12-bit resolution

Industrial Control Peripherals

- Two Capture/Compare Units 8 (CCU8) for motor control and power conversion
- Four Capture/Compare Units 4 (CCU4) for use as general purpose timers
- Two Position Interfaces (POSIF) for servo motor positioning
- Window Watchdog Timer (WDT) for safety sensitive applications
- Die Temperature Sensor (DTS)
- Real Time Clock module with alarm support
- System Control Unit (SCU) for system configuration and control

Summary of Features
Table 4 Flash Memory Ranges (cont'd)

Total Flash Size	Cached Range	Uncached Range
768 Kbytes	0800 0000 _H – 080B FFFF _H	0C00 0000 _H – 0C0B FFFF _H
1,024 Kbytes	0800 0000 _H – 080F FFFF _H	0C00 0000 _H – 0C0F FFFF _H

Table 5 SRAM Memory Ranges

Total SRAM Size	Program SRAM	System Data SRAM	Communication Data SRAM
128 Kbytes	1000 0000 _H – 1000 FFFF _H	2000 0000 _H – 2000 FFFF _H	–
160 Kbytes	1000 0000 _H – 1000 FFFF _H	2000 0000 _H – 2000 FFFF _H	3000 0000 _H – 3000 7FFF _H

Table 6 ADC Channels¹⁾

Package	VADC G0	VADC G1	VADC G2	VADC G3
PG-LQFP-144 PG-LFBGA-144	CH0..CH7	CH0..CH7	CH0..CH7	CH0..CH7
PG-LQFP-100	CH0..CH7	CH0..CH7	CH0..CH3	CH0..CH3

1) Some pins in a package may be connected to more than one channel. For the detailed mapping see the Port I/O Function table.

1.5 Identification Registers

The identification registers allow software to identify the marking.

Table 7 XMC4500 Identification Registers

Register Name	Value	Marking
SCU_IDCHIP	0004 5002 _H	EES-AA, ES-AA
SCU_IDCHIP	0004 5003 _H	ES-AB, AB
SCU_IDCHIP	0004 5004 _H	AC
JTAG IDCODE	101D B083 _H	EES-AA, ES-AA
JTAG IDCODE	101D B083 _H	ES-AB, AB
JTAG IDCODE	401D B083 _H	AC

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

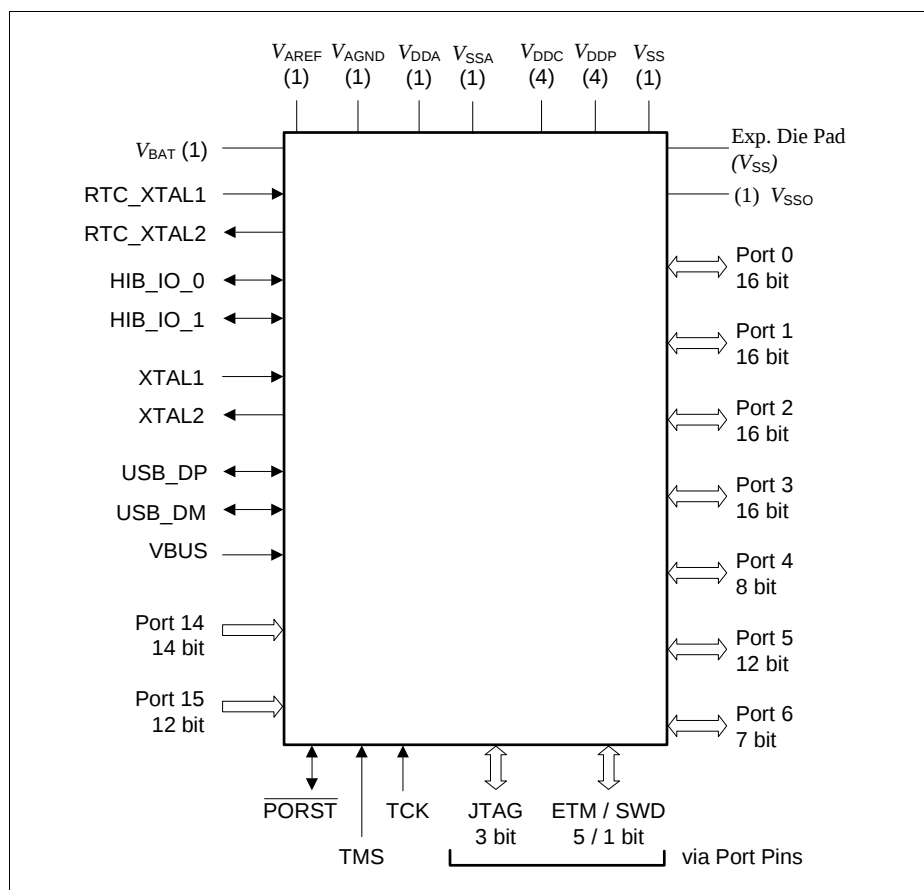


Figure 2 XMC4500 Logic Symbol PG-LQFP-144

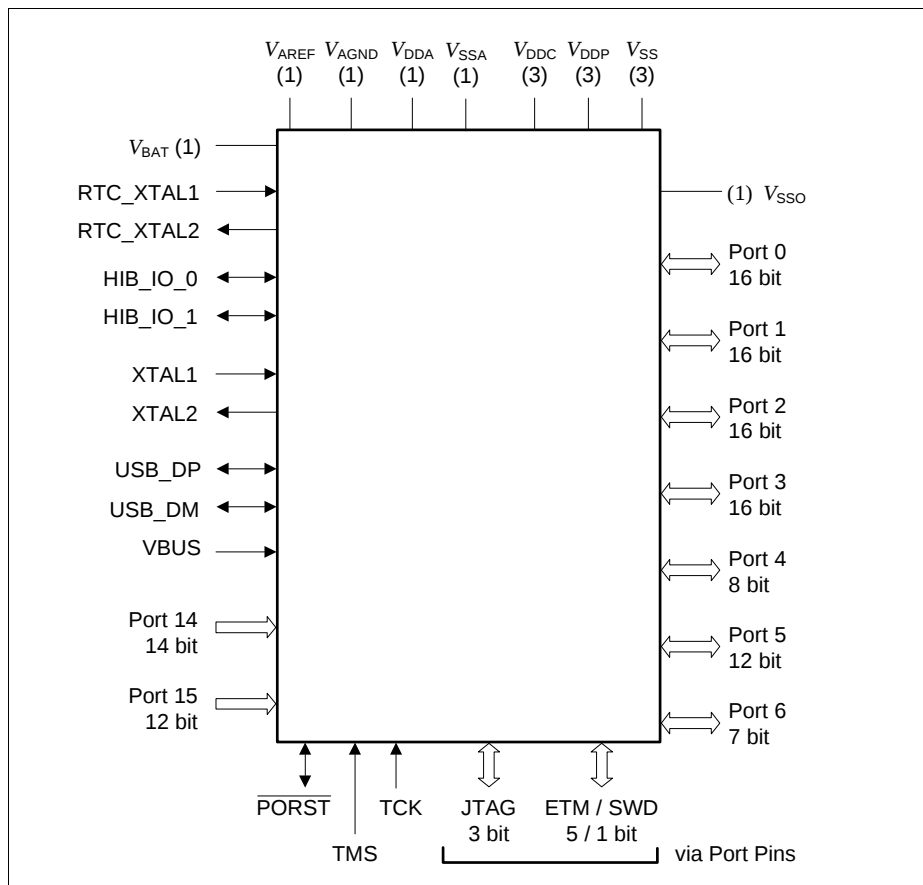


Figure 3 XMC4500 Logic Symbol PG-LFBGA-144

General Device Information

	1	2	3	4	5	6	7	8	9	10	11	12	
A	VSS	VDDC	P0.2	P0.3	P0.5	P0.6	P3.6	P0.8	P4.1	P1.8	VDDP	VSS	A
B	VDDP	P3.1	P3.2	P0.10	P0.4	P3.5	P0.7	P4.0	P1.6	P1.7	P1.9	VDDC	B
C	P3.0	P3.13	P0.1	P0.0	P0.13	P0.15	P4.4	P4.6	P4.7	P1.4	P1.2	P1.3	C
D	USB_D M	P3.12	P3.11	P0.9	P0.12	P3.14	P3.15	P4.5	P1.0	P1.5	P1.11	P1.10	D
E	USB_D P	VBUS	P3.8	P3.7	P0.11	P0.14	P3.4	P4.2	P1.1	P1.14	P1.12	P1.13	E
F	RTC_X TAL2	RTC_X TAL1	HIB_I O_1	HIB_I O_0	P3.9	P3.10	P3.3	P4.3	P6.1	P6.4	P6.5	P6.6	F
G	VBAT	P15.3	P15.5	P15.4	P15.6	P15.7	TMS	TCK	P6.3	P6.0	PORST	P1.15	G
H	P15.2	P14.15	P14.14	P14.13	P5.10	P5.8	P5.2	P5.1	P5.0	P6.2	XTAL1	XTAL2	H
J	P14.12	P14.7	P14.6	P14.3	P5.11	P2.15	P5.7	P5.5	P2.6	P5.3	P2.0	VSSO	J
K	P14.4	P14.5	P14.2	P15.15	P15.12	P5.9	P2.14	P5.6	P2.7	P5.4	P2.2	P2.1	K
L	VDDA	P14.1	P14.0	P15.14	P14.9	P15.9	P2.12	P2.10	P2.8	P2.4	P2.3	VDDP	L
M	VSSA	VAGND	VAREF	P15.13	P14.8	P15.8	P2.13	P2.11	P2.9	P2.5	VDDC	VSS	M
	1	2	3	4	5	6	7	8	9	10	11	12	

XMC4500- (top view)

Figure 6 XMC4500 PG-LFBGA-144 Pin Configuration (top view)

Table 11 Port I/O Functions (cont'd)

Function	Outputs						Inputs									
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P1.5	CAN. N1_TXD	U0C0. DOUT0	U0C0. OUT23	CCU81. OUT10	U0C0. DOUT0		U0C0. HWIN0		U0C0. DX0A	CAN. N0_RXDA	ERU0. ZA0	ERU1. 0A0	CCU41. IN1C	DSD. DIN2B		
P1.6		U0C0. SCLKOUT			SDMMC. DATA1_OUT	EBU. AD10	SDMMC. DATA1_IN	EBU. D10	DSD. DIN2A							
P1.7		U0C0. DOUT0	DSD. MCLK2		SDMMC. DATA2_OUT	EBU. AD11	SDMMC. DATA2_IN	EBU. D11		DSD. MCLK2A						
P1.8		U0C0. SELO1	DSD. MCLK1		SDMMC. DATA4_OUT	EBU. AD12	SDMMC. DATA4_IN	EBU. D12	CAN. N2_RXDA	DSD. MCLK1A						
P1.9		CAN. N2_TXD			SDMMC. DATA5_OUT	EBU. AD13	SDMMC. DATA5_IN	EBU. D13		DSD. MCLK0A						
P1.10	ETH0. MDC	U0C0. SCLKOUT	CCU81. OUT21				SDMMC. SDCD						CCU41. IN2C			
P1.11		U0C0. SELO0	CCU81. OUT11		ETH0. MDO		ETH0. MDIC						CCU41. IN2C			
P1.12	ETH0. TX_EN	CAN. N1_TXD	CCU81. OUT01		SDMMC. DATA6_OUT	EBU. AD16	SDMMC. DATA6_IN	EBU. D16								
P1.13	ETH0. TXD0	U0C1. SELO3	CCU81. OUT20		SDMMC. DATA7_OUT	EBU. AD17	SDMMC. DATA7_IN	EBU. D17	CAN. N1_RXDC							
P1.14	ETH0. TXD1	U0C1. SELO2	CCU81. OUT10			EBU. AD18		EBU. D18								
P1.15	SCU. EXTCLK	DSD. MCLK2	CCU81. OUT00			EBU. AD19		EBU. D19		DSD. MCLK2B		ERU1. 1A0				
P2.0		CCU81. OUT21	DSD. CGPWMN	LEDTS0. COL1	ETH0. MDO	EBU. AD20	ETH0. MDIB	EBU. D20			ERU0. 0B3		CCU40. IN1C			
P2.1		CCU81. OUT11	DSD. CGPWMN	LEDTS0. COL0	DB.TDQ/ TRACESWO	EBU. AD21		EBU. D21	ETH0. CLK_RMIIA			ERU1. 0B0	CCU40. IN0C			ETH0. CLKRXA
P2.2	VADC. EMUX00	CCU81. OUT01	CCU41. OUT3	LEDTS0. LINE0	LEDTS0. EXTENDED0	EBU. AD22	LEDTS0. TSIN0A	EBU. D22	ETH0. RXD0A	U0C1. DX0A	ERU0. 1B2		CCU41. IN3A			
P2.3	VADC. EMUX01	U0C1. SELO0	CCU41. OUT2	LEDTS0. LINE1	LEDTS0. EXTENDED1	EBU. AD23	LEDTS0. TSIN1A	EBU. D23	ETH0. RXD1A	U0C1. DX2A	ERU0. 1A2	POSIF1. IN2A	CCU41. IN2A			
P2.4	VADC. EMUX02	U0C1. SCLKOUT	CCU41. OUT1	LEDTS0. LINE2	LEDTS0. EXTENDED2	EBU. AD24	LEDTS0. TSIN2A	EBU. D24	ETH0. RXERA	U0C1. DX1A	ERU0. 0B2	POSIF1. IN1A	CCU41. IN1A			
P2.5	ETH0. TX_EN	U0C1. DOUT0	CCU41. OUT0	LEDTS0. LINE3	LEDTS0. EXTENDED3	EBU. AD25	LEDTS0. TSIN3A	EBU. D25	ETH0. RXDVA	U0C1. DX0B	ERU0. 0A2	POSIF1. IN0A	CCU41. IN0A		ETH0. CRS_DVA	
P2.6	U2C0. SELO4		CCU80. OUT13	LEDTS0. COL3	U2C0. DOUT3		U2C0. HWIN3		DSD. DIN1B	CAN. N1_RXDA	ERU0. 1B3		CCU40. IN3C			
P2.7	ETH0. MDC	CAN. N1_TXD	CCU80. OUT03	LEDTS0. COL2						DSD. DIN0B		ERU1. 1B0	CCU40. IN2C			
P2.8	ETH0. TXD0		CCU80. OUT32	LEDTS0. LINE4	LEDTS0. EXTENDED4	EBU. AD26	LEDTS0. TSIN4A	EBU. D26	DAC. TRIGGERS				CCU40. IN0B	CCU40. IN1B	CCU40. IN2B	CCU40. IN3B
P2.9	ETH0. TXD1		CCU80. OUT22	LEDTS0. LINE5	LEDTS0. EXTENDED5	EBU. AD27	LEDTS0. TSIN5A	EBU. D27	DAC. TRIGGER4				CCU41. IN0B	CCU41. IN1B	CCU41. IN2B	CCU41. IN3B
P2.10	VADC. EMUX10				DB. ETM_TRACEDA TA3	EBU. AD28		EBU. D28								
P2.11	ETH0. TXER		CCU80. OUT22		DB. ETM_TRACEDA TA2	EBU. AD29		EBU. D29								

Table 11 Port I/O Functions (cont'd)

Function	Outputs						Inputs								
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input
P6.6			DSD. MCLK3		DE. ETM_TRACEDA TA0	EBU. BC3			DSD. MCLK3A	ETH0. CLK_TXB					
P14.0									VADC. G0CH0						
P14.1									VADC. G0CH1						
P14.2									VADC. G0CH2	VADC. G1CH2					
P14.3									VADC. G0CH3	VADC. G1CH3			CAN. N0_RXDB		
P14.4									VADC. G0CH4		VADC. G2CH0				
P14.5									VADC. G0CH5		VADC. G2CH1		POSIF0. IN2B		
P14.6									VADC. G0CH6				POSIF0. IN1B	G0ORC6	
P14.7									VADC. G0CH7				POSIF0. IN0B	G0ORC7	
P14.8					DAC. OUT_0					VADC. G1CH0		VADC. G3CH2	ETH0. RXD0C		
P14.9					DAC. OUT_1					VADC. G1CH1		VADC. G3CH3	ETH0. RXD1C		
P14.12										VADC. G1CH4					
P14.13										VADC. G1CH5					
P14.14										VADC. G1CH6				G1ORC6	
P14.15										VADC. G1CH7				G1ORC7	
P15.2											VADC. G2CH2				
P15.3											VADC. G2CH3				
P15.4											VADC. G2CH4				
P15.5											VADC. G2CH5				
P15.6											VADC. G2CH6				
P15.7											VADC. G2CH7				
P15.8												VADC. G3CH0	ETH0. CLK_RMIIIC		ETH0. CLKRXIC
P15.9												VADC. G3CH1	ETH0. CRS_DVC		ETH0. RXDVC

Table 11 Port I/O Functions (cont'd)

Function	Outputs						Inputs								
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input
P15.12												VADC_G3CH4			
P15.13												VADC_G3CH5			
P15.14												VADC_G3CH6			
P15.15												VADC_G3CH7			
USB_DP															
USB_DM															
HIB_IO_0	HIBOUT	WWDT. SERVICE_OUT							WAKEUPA						
HIB_IO_1	HIBOUT	WWDT. SERVICE_OUT							WAKEUPB						
TCK							DB.TCK/ SWCLK								
TMS					DB.TMS/ SWDIO										
PORST															
XTAL1									U0C0. DX0F	U0C1. DX0F	U1C0. DX0F	U1C1. DX0F	U2C0. DX0F	U2C1. DX0F	
XTAL2															
RTC_XTAL1											ERU0. 1B1				
RTC_XTAL2															

3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 12 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Storage temperature	T_{ST}	SR	-65	–	150	°C	–
Junction temperature	T_J	SR	-40	–	150	°C	–
Voltage at 3.3 V power supply pins with respect to V_{SS}	V_{DDP}	SR	–	–	4.3	V	–
Voltage on any Class A and dedicated input pin with respect to V_{SS}	V_{IN}	SR	-1.0	–	$V_{DDP} + 1.0$ or max. 4.3	V	whichever is lower
Voltage on any analog input pin with respect to V_{AGND}	V_{AIN} V_{AREF}	SR	-1.0	–	$V_{DDP} + 1.0$ or max. 4.3	V	whichever is lower
Input current on any pin during overload condition	I_{IN}	SR	-10	–	+10	mA	
Absolute maximum sum of all input circuit currents for one port group during overload condition ¹⁾	ΣI_{IN}	SR	-25	–	+25	mA	
Absolute maximum sum of all input circuit currents during overload condition	ΣI_{IN}	SR	-100	–	+100	mA	

1) The port groups are defined in [Table 16](#).

Figure 10 explains the input voltage ranges of V_{IN} and V_{AIN} and its dependency to the supply level of V_{DDP} . The input voltage must not exceed 4.3 V, and it must not be more than 1.0 V above V_{DDP} . For the range up to $V_{DDP} + 1.0$ V also see the definition of the overload conditions in [Section 3.1.3](#).

Electrical Parameters
Table 22 Standard Pads Class_A2

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Fall time	t_{FA2} CC	–	150	ns	$C_L = 20$ pF; POD = weak
		–	50	ns	$C_L = 50$ pF; POD = medium
		–	3.7	ns	$C_L = 50$ pF; POD = strong; edge = sharp
		–	7	ns	$C_L = 50$ pF; POD = strong; edge = medium
		–	16	ns	$C_L = 50$ pF; POD = strong; edge = soft
Rise time	t_{RA2} CC	–	150	ns	$C_L = 20$ pF; POD = weak
		–	50	ns	$C_L = 50$ pF; POD = medium
		–	3.7	ns	$C_L = 50$ pF; POD = strong; edge = sharp
		–	7.0	ns	$C_L = 50$ pF; POD = strong; edge = medium
		–	16	ns	$C_L = 50$ pF; POD = strong; edge = soft

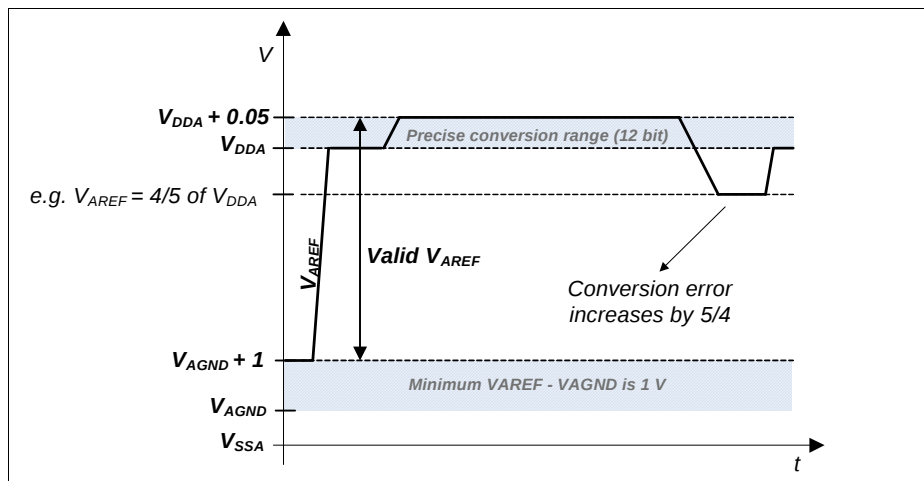


Figure 14 VADC Reference Voltage Range

The power-up calibration of the VADC requires a maximum number of $4\,352\,f_{\text{ADCl}}$ cycles.

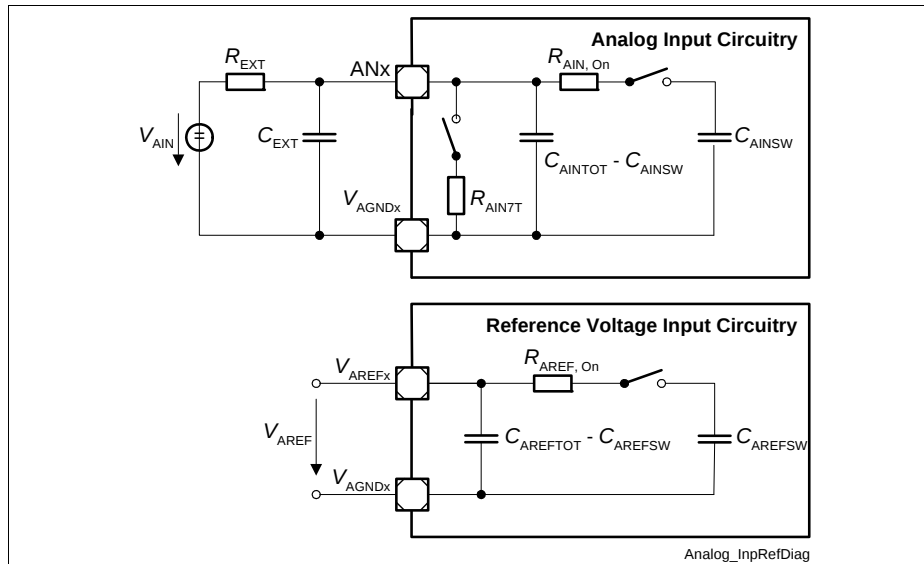


Figure 15 VADC Input Circuits

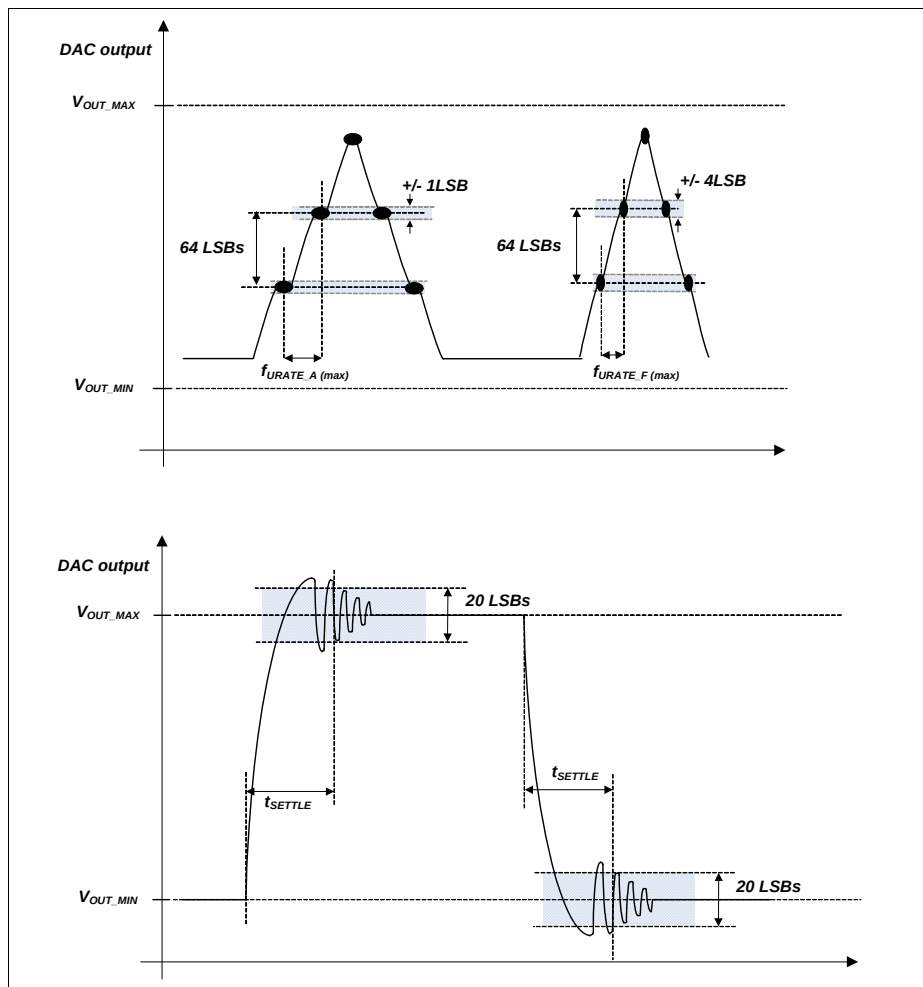


Figure 17 DAC Conversion Examples

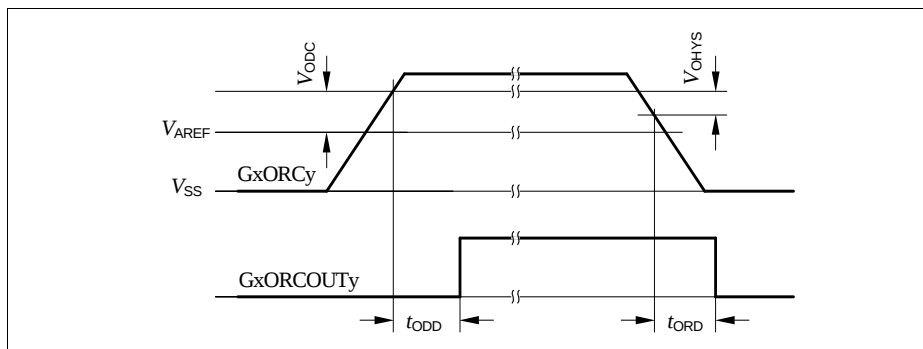


Figure 18 GxORCOUTy Trigger Generation

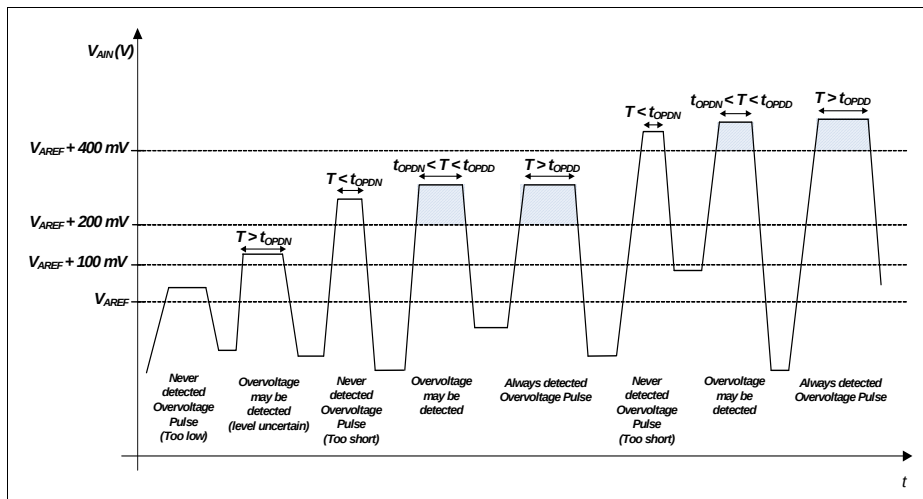


Figure 19 ORC Detection Ranges

Table 31 RTC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{OSC} SR	–	32.768	–	kHz	
Oscillator start-up time ¹⁾²⁾³⁾	t_{OSCS} CC	–	–	5	s	
Input voltage at RTC_XTAL1	V_{IX} SR	-0.3	–	$V_{BAT} + 0.3$	V	
Input amplitude (peak-to-peak) at RTC_XTAL1 ²⁾⁴⁾	V_{PPX} SR	0.4	–	–	V	
Input high voltage at RTC_XTAL1 ⁵⁾	V_{IHBX} SR	$0.6 \times V_{BAT}$	–	$V_{BAT} + 0.3$	V	
Input low voltage at RTC_XTAL1 ⁵⁾	V_{ILBX} SR	-0.3	–	$0.36 \times V_{BAT}$	V	
Input Hysteresis for RTC_XTAL1 ⁵⁾⁶⁾	V_{HYSX} CC	$0.1 \times V_{BAT}$	–	–	V	$3.0 \text{ V} \leq V_{BAT} < 3.6 \text{ V}$
		$0.03 \times V_{BAT}$	–	–	V	$V_{BAT} < 3.0 \text{ V}$
Input leakage current at RTC_XTAL1	I_{ILX1} CC	-100	–	100	nA	Oscillator power down $0 \text{ V} \leq V_{IX} \leq V_{BAT}$

1) t_{OSCS} is defined from the moment the oscillator is enabled by the user with SCU_OSCULCTRL.MODE until the oscillations reach an amplitude at RTC_XTAL1 of 400 mV.

2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.

3) For a reliable start of the oscillation in crystal mode it is required that $V_{BAT} \geq 3.0 \text{ V}$. A running oscillation is maintained across the full V_{BAT} voltage range.

4) If the shaper unit is enabled and not bypassed.

5) If the shaper unit is bypassed, dedicated DC-thresholds have to be met.

6) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

Electrical Parameters
Table 32 Power Supply Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Sleep supply current ⁴⁾ Peripherals disabled Frequency: $f_{CPU} / f_{PERIPH} / f_{CCU}$ in MHz	I_{DDPS} CC		–	110	–	mA	120 / 120 / 120
			–	100	–		120 / 60 / 60
			–	77	–		60 / 60 / 120
			–	59	–		24 / 24 / 24
			–	48	–		1 / 1 / 1
			–	46	–		100 / 100 / 100
$f_{CPU} / f_{PERIPH} / f_{CCU}$ in kHz Deep Sleep supply current ⁵⁾ Flash in Sleep mode Frequency: $f_{CPU} / f_{PERIPH} / f_{CCU}$ in MHz $f_{CPU} / f_{PERIPH} / f_{CCU}$ in kHz	I_{DDPD} CC		–	20	–	mA	24 / 24 / 24
			–	12	–		4 / 4 / 4
			–	10	–		1 / 1 / 1
			–	6	–		100 / 100 / 100 ⁶⁾
Hibernate supply current RTC on ⁷⁾	I_{DDPH} CC		–	10	–	μ A	$V_{BAT} = 3.3$ V
			–	7.5	–		$V_{BAT} = 2.4$ V
			–	6.2	–		$V_{BAT} = 2.0$ V
Hibernate supply current RTC off ⁸⁾	I_{DDPH} CC		–	9.2	–	μ A	$V_{BAT} = 3.3$ V
			–	6.7	–		$V_{BAT} = 2.4$ V
			–	5.6	–		$V_{BAT} = 2.0$ V
Worst case active supply current ⁹⁾	I_{DDPA} CC		–	–	180 ¹⁰⁾	mA	$V_{DDP} = 3.6$ V, $T_J = 150$ °C
V_{DDA} power supply current	I_{DDA} CC		–	–	– ¹¹⁾	mA	
I_{DDP} current at $\overline{PORST}$ Low	I_{DDP_PORST} CC		–	–	16	mA	$V_{DDP} = 3.6$ V, $T_J = 150$ °C
Power Dissipation	P_{DISS} CC		–	–	1	W	$V_{DDP} = 3.6$ V, $T_J = 150$ °C
Wake-up time from Sleep to Active mode	t_{SSA} CC		–	6	–	cycles	

Table 35 Power Sequencing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Positive Load Step Current	ΔI_{PLS} SR	-	—	50	mA	Load increase on V_{DDP} $\Delta t \leq 10$ ns
Negative Load Step Current	ΔI_{NLS} SR	-	—	150	mA	Load decrease on V_{DDP} $\Delta t \leq 10$ ns
V_{DDC} Voltage Over- / Undershoot from Load Step	ΔV_{LS} CC	-	—	± 100	mV	For maximum positive or negative load step
Positive Load Step Settling Time	t_{PLSS} SR	50	—	-	μ s	
Negative Load Step Settling Time	t_{NLSS} SR	100	—	-	μ s	
External Buffer Capacitor on V_{DDC}	C_{EXT} SR	-	10	-	μ F	In addition $C = 100$ nF capacitor on each V_{DDC} pin

Positive Load Step Examples

System assumptions:

$f_{CPU} = f_{SYS}$, target frequency $f_{CPU} = 120$ MHz, main PLL $f_{VCO} = 480$ MHz, stepping done by K2 divider, t_{PLSS} between individual steps:

24 MHz - 48 MHz - 68 MHz - 96 MHz - 120 MHz (K2 steps 20 - 10 - 7 - 5 - 4)

24 MHz - 68 MHz - 96 MHz - 120 MHz (K2 steps 20 - 7 - 5 - 4)

24 MHz - 68 MHz - 120 MHz (K2 steps 20 - 7 - 4)

3.3.9.3 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 45 USIC IIC Standard Mode Timing¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	-	-	1000	ns	
Data hold time	t_3 CC/SR	0	-	-	μs	
Data set-up time	t_4 CC/SR	250	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	-	-	μs	
HIGH period of SCL clock	t_6 CC/SR	4.0	-	-	μs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	-	-	μs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	-	-	μs	
Set-up time for STOP condition	t_9 CC/SR	4.0	-	-	μs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	-	-	μs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

Multiplexed Write Timing

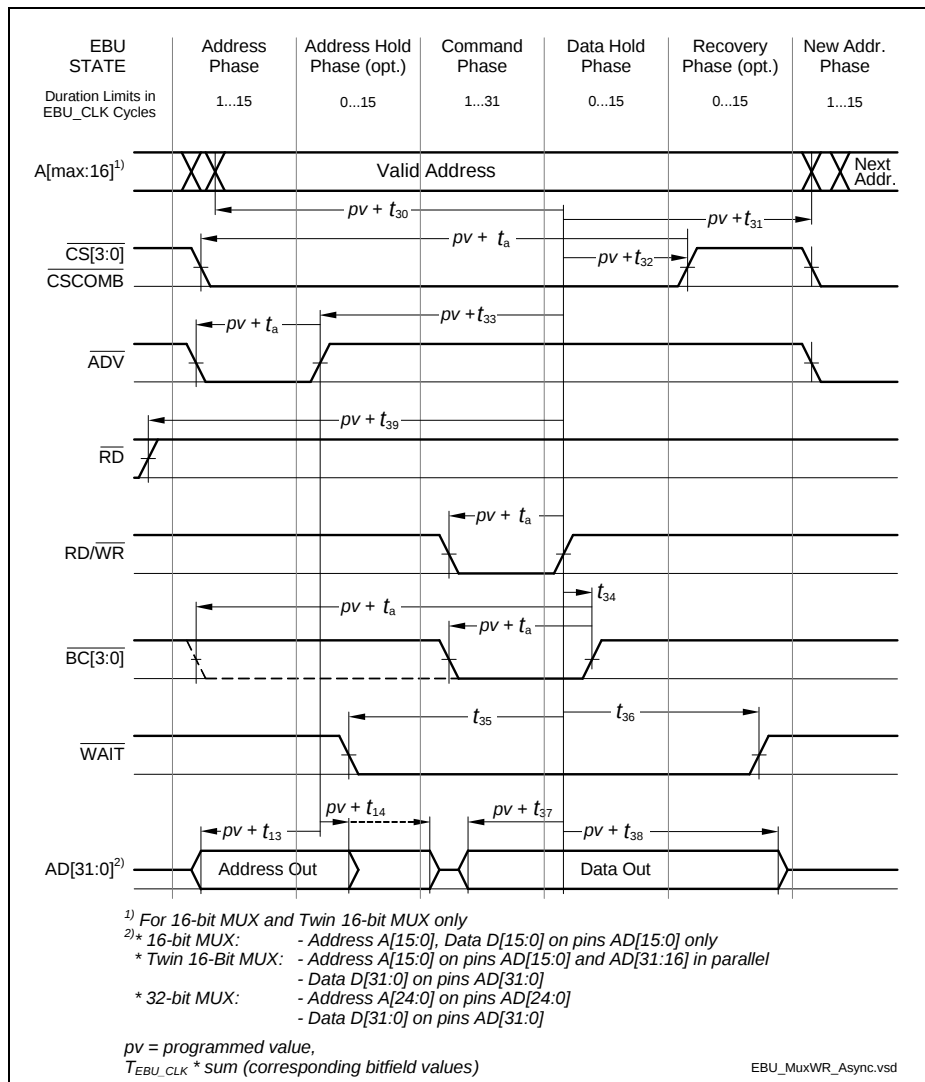


Figure 43 Multiplexed Write Access

4.3 Quality Declarations

The qualification of the XMC4500 is executed according to the JEDEC standard JESD47H.

Note: For automotive applications refer to the Infineon automotive microcontrollers.

Table 67 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation lifetime	t_{OP} CC	20	–	–	a	$T_J \leq 109^\circ\text{C}$, device permanent on
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	–	–	2 000	V	EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM} SR	–	–	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	–	–	3	–	JEDEC J-STD-020D
Soldering temperature	T_{SDR} SR	–	–	260	$^\circ\text{C}$	Profile according to JEDEC J-STD-020D

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