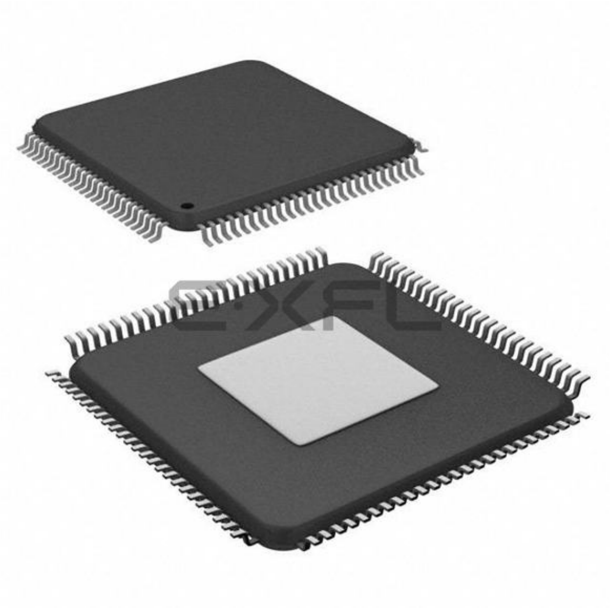


Welcome to E-XFL.COM

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 120MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, LINbus, SPI, UART, USB |
| Peripherals | DMA, I²S, LED, POR, PWM, WDT |
| Number of I/O | 55 |
| Program Memory Size | 768KB (768K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 160K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3.13V ~ 3.63V |
| Data Converters | A/D 24x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP Exposed Pad |
| Supplier Device Package | PG-LQFP-100-11 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xmc4500f100f768acxqma1 |

# Table of Contents

**Table 2 Features of XMC4500 Device Types** (cont'd)

| Derivative[1)] | LEDTS Intf. | SDMMC Intf. | EBU Intf.[2)] | ETH Intf.[3)] | USB Intf. | USIC Chan. | MultiCAN Nodes, MO |
|---|---|---|---|---|---|---|---|
| XMC4504-F144x512 | 1 | 1 | SDM | - | - | 3 x 2 | - |
| XMC4504-F100x512 | 1 | 1 | M16 | - | - | 3 x 2 | - |

1) x is a placeholder for the supported temperature range.

2) Memory types supported S=SDRAM, D=DEMUX, M=MUX 16-bit and 32-bit, M16=MUX 16-bit

3) Supported interfaces, M=MII, R=RMII.

**Table 3 Features of XMC4500 Device Types**

| Derivative[1)] | ADC Chan. | DSD Chan. | DAC Chan. | CCU4 Slice | CCU8 Slice | POSIF Intf. |
|---|---|---|---|---|---|---|
| XMC4500-E144x1024 | 32 | 4 | 2 | 4 x 4 | 2 x 4 | 2 |
| XMC4500-F144x1024 | 32 | 4 | 2 | 4 x 4 | 2 x 4 | 2 |
| XMC4500-F100x1024 | 24 | 4 | 2 | 4 x 4 | 2 x 4 | 2 |
| XMC4500-F144x768 | 32 | 4 | 2 | 4 x 4 | 2 x 4 | 2 |
| XMC4500-F100x768 | 24 | 4 | 2 | 4 x 4 | 2 x 4 | 2 |
| XMC4502-F100x768 | 24 | 4 | 2 | 4 x 4 | 2 x 4 | 2 |
| XMC4504-F144x512 | 32 | 4 | 2 | 4 x 4 | 2 x 4 | 2 |
| XMC4504-F100x512 | 24 | 4 | 2 | 4 x 4 | 2 x 4 | 2 |

1) x is a placeholder for the supported temperature range.

## 1.4 Definition of Feature Variants

The XMC4500 types are offered with several memory sizes and number of available VADC channels. **Table 4** describes the location of the available Flash memory, **Table 5** describes the location of the available SRAMs, **Table 6** the available VADC channels.

**Table 4 Flash Memory Ranges**

| Total Flash Size | Cached Range | Uncached Range |
|---|---|---|
| 512 Kbytes | $0800\ 0000_H$ – $0807\ FFFF_H$ | $0C00\ 0000_H$ – $0C07\ FFFF_H$ |

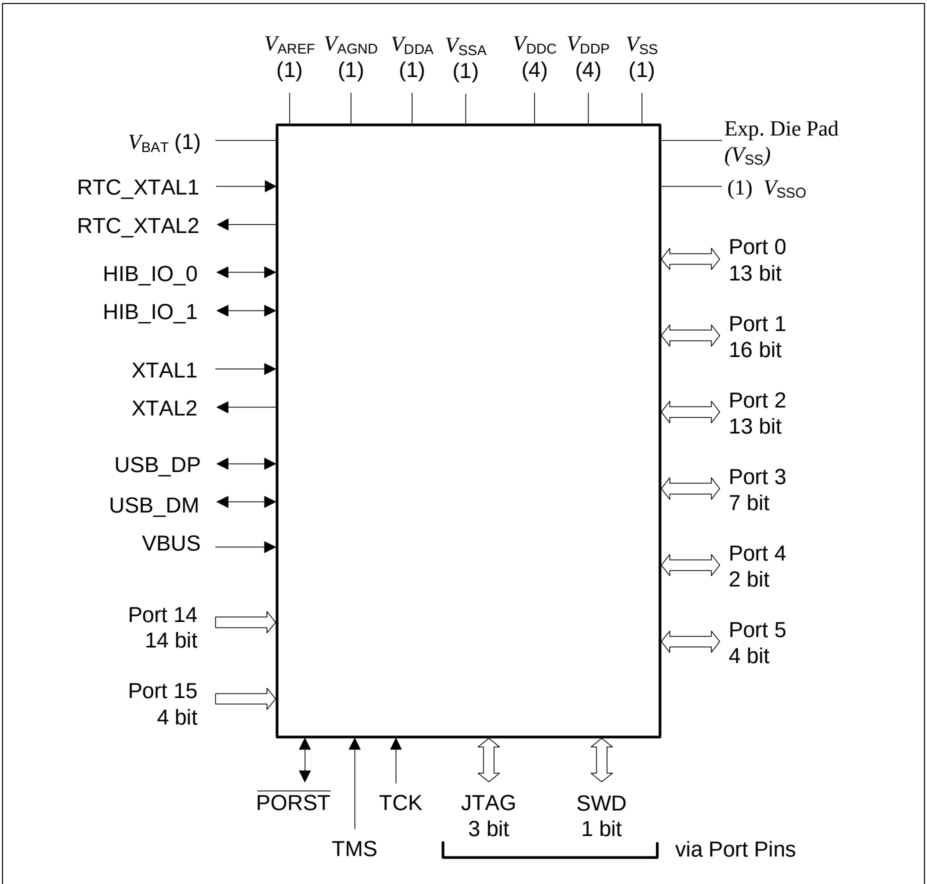



**Figure 4 XMC4500 Logic Symbol PG-LQFP-100**

### 2.2.1 Package Pin Summary

The following general scheme is used to describe each pin:

**Table 8 Package Pin Mapping Description**

| Function | Package A | Package B | ... | Pad Type | Notes |
|---|---|---|---|---|---|
| Name | N | Ax | ... | A2 | |

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the dedicated pins (i.e. PORST) and supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type (A1, A1+, A2, special=special pad, In=input pad, AN/DIG_IN=analog and digital input, Power=power supply). Details about the pad properties are defined in the Electrical Parameters.

In the “Notes”, special information to the respective pin/function is given, i.e. deviations from the default configuration after reset. Per default the regular Port pins are configured as direct input with no internal pull device active.

**Table 9 Package Pin Mapping**

| Function | LQFP-144 | LFBGA-144 | LQFP-100 | Pad Type | Notes |
|---|---|---|---|---|---|
| P0.0 | 2 | C4 | 2 | A1+ | |
| P0.1 | 1 | C3 | 1 | A1+ | |
| P0.2 | 144 | A3 | 100 | A2 | |
| P0.3 | 143 | A4 | 99 | A2 | |
| P0.4 | 142 | B5 | 98 | A2 | |
| P0.5 | 141 | A5 | 97 | A2 | |
| P0.6 | 140 | A6 | 96 | A2 | |
| P0.7 | 128 | B7 | 89 | A2 | After a system reset, via HWSEL this pin selects the DB.TDI function. |
| P0.8 | 127 | A8 | 88 | A2 | After a system reset, via HWSEL this pin selects the DB.TRST function, with a weak pull-down active. |
| P0.9 | 4 | D4 | 4 | A2 | |
| P0.10 | 3 | B4 | 3 | A1+ | |

## 2.3 Power Connection Scheme

Figure 9. shows a reference power connection scheme for the XMC4500.

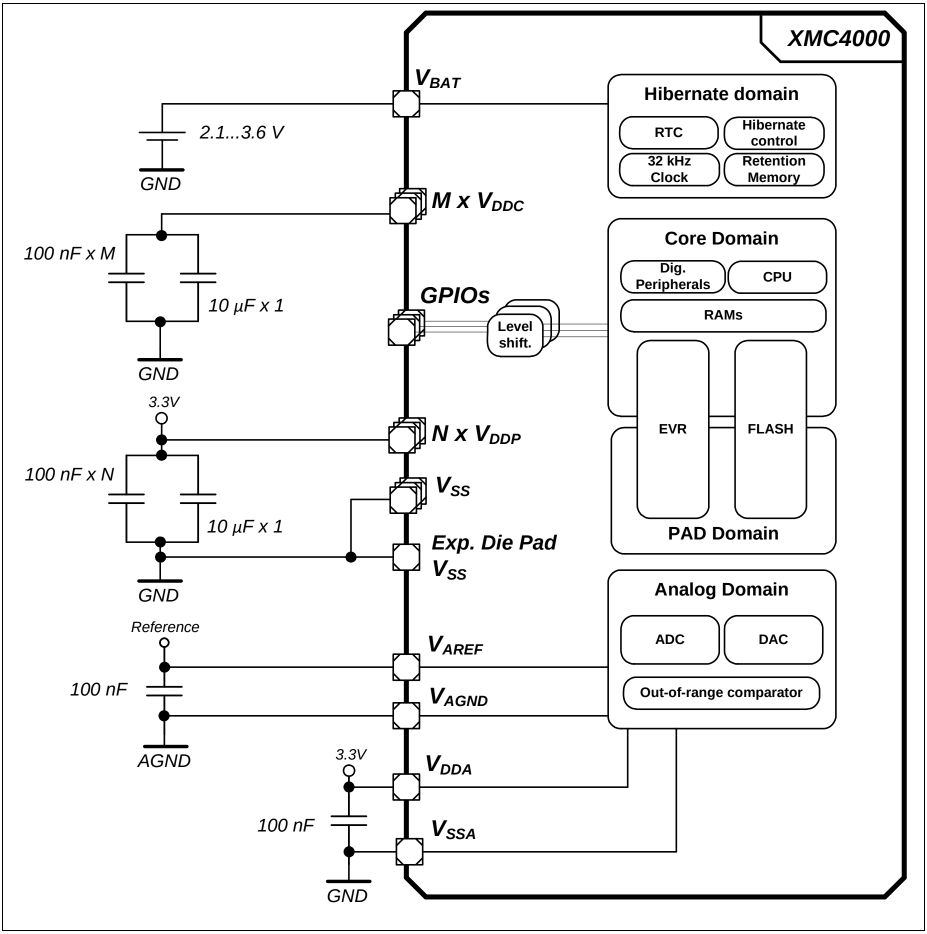



**Figure 9 Power Connection Scheme**

Every power supply pin needs to be connected. Different pins of the same supply need also to be externally connected. As example, all $V_{DDP}$ pins must be connected externally to one $V_{DDP}$ net. In this reference scheme one 100 nF capacitor is connected at each supply pin against $V_{SS}$. An additional 10 µF capacitor is connected to the $V_{DDP}$ nets and an additional 10 uF capacitor to the $V_{DDC}$ nets.

# 3 Electrical Parameters

## 3.1 General Parameters

### 3.1.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the XMC4500 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with a two-letter abbreviation in column “Symbol”:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics, which are a distinctive feature of the XMC4500 and must be regarded for system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC4500 is designed in.

### 3.1.4 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and their basic characteristics.

**Table 17 Pad Driver and Pad Classes Overview**

| Class | Power Supply | Type | Sub-Class | Speed Grade | Load | Termination |
|---|---|---|---|---|---|---|
| **A** | 3.3 V | LVTTL I/O | **A1** (e.g. GPIO) | 6 MHz | 100 pF | No |
| | | | **A1+** (e.g. serial I/Os) | 25 MHz | 50 pF | Series termination recommended |
| | | | **A2** (e.g. ext. Bus) | 80 MHz | 15 pF | Series termination recommended |

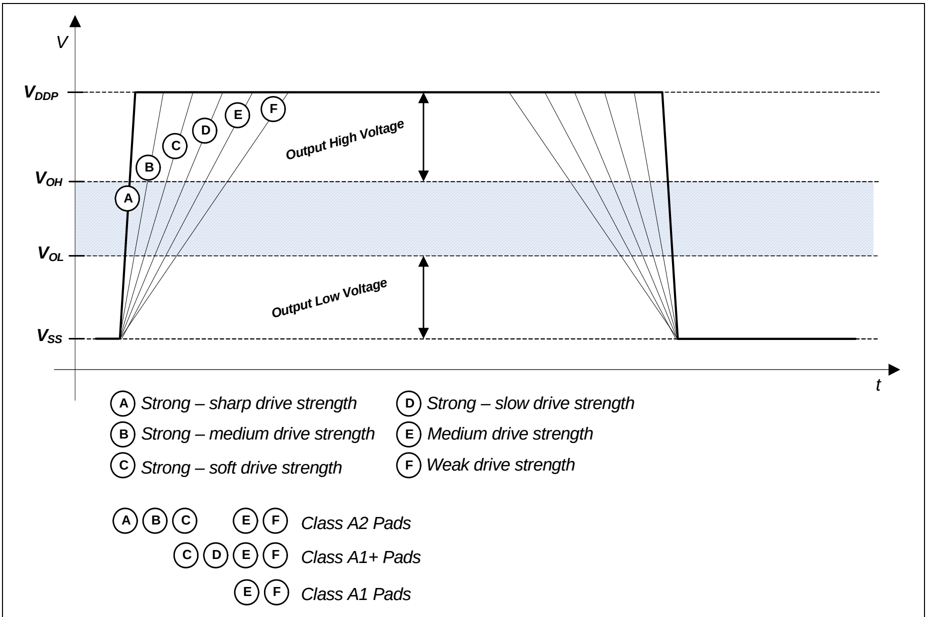



**Figure 12 Output Slopes with different Pad Driver Modes**

**Figure 12** is a qualitative display of the resulting output slope performance with different output driver modes. The detailed input and output characteristics are listed in **Section 3.2.1**.

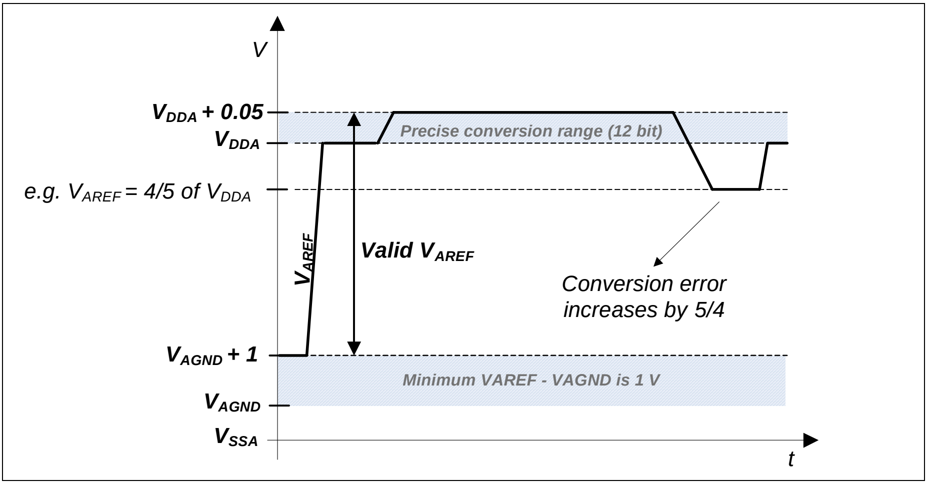



**Figure 14 VADC Reference Voltage Range**

The power-up calibration of the VADC requires a maximum number of 4 352 $f_{ADCI}$ cycles.

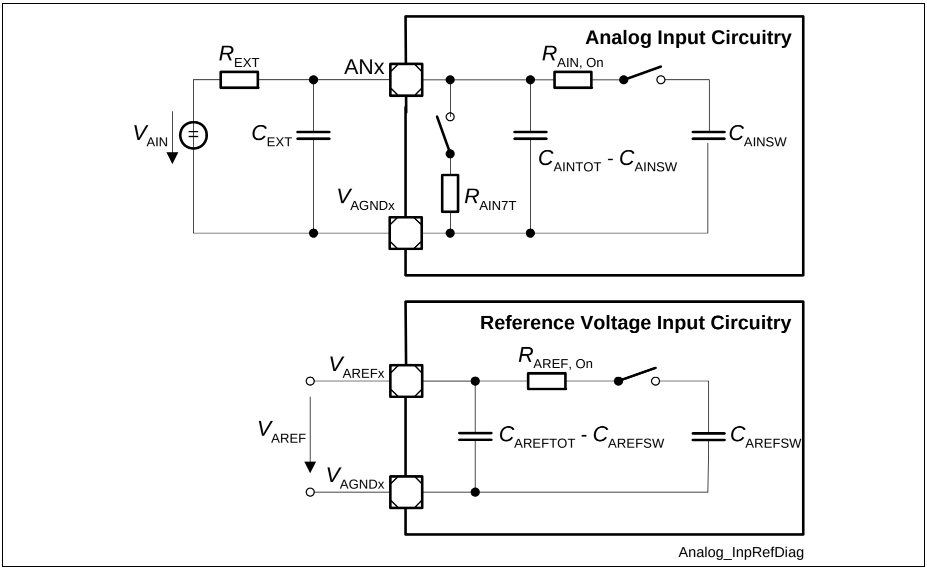



**Figure 15 VADC Input Circuits**

### 3.2.3 Digital to Analog Converters (DAC)

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 25 DAC Parameters** (Operating Conditions apply)

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| RMS supply current | $I_{DD}$ | CC | – | 2.5 | 4 | mA | per active DAC channel, without load currents of DAC outputs |
| Resolution | $RES$ | CC | – | 12 | – | Bit | |
| Update rate | $f_{URATE\_A}$ | CC | – | | 2 | Msample/s | data rate, where DAC can follow 64 LSB code jumps to ± 1LSB accuracy |
| Update rate | $f_{URATE\_F}$ | CC | – | | 5 | Msample/s | data rate, where DAC can follow 64 LSB code jumps to ± 4 LSB accuracy |
| Settling time | $t_{SETTLE}$ | CC | – | 1 | 2 | µs | at full scale jump, output voltage reaches target value ± 20 LSB |
| Slew rate | $SR$ | CC | 2 | 5 | – | V/µs | |
| Minimum output voltage | $V_{OUT\_MIN}$ | CC | – | 0.3 | – | V | code value unsigned: $000_H$; signed: $800_H$ |
| Maximum output voltage | $V_{OUT\_MAX}$ | CC | – | 2.5 | – | V | code value unsigned: $FFF_H$; signed: $7FF_H$ |
| Integral non-linearity | $INL$ | CC | -4 | ±2.5 | 4 | LSB | $R_L \geq 5$ kOhm, $C_L \leq 50$ pF |
| Differential non-linearity | $DNL$ | CC | -2 | ±1 | 2 | LSB | $R_L \geq 5$ kOhm, $C_L \leq 50$ pF |

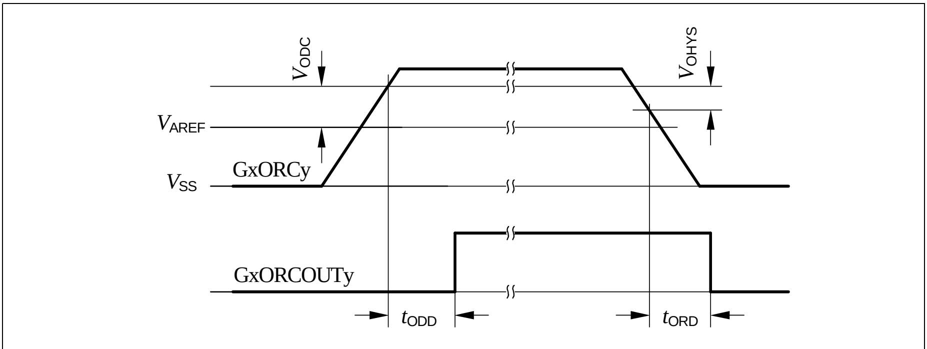



**Figure 18 GxORCOUTy Trigger Generation**

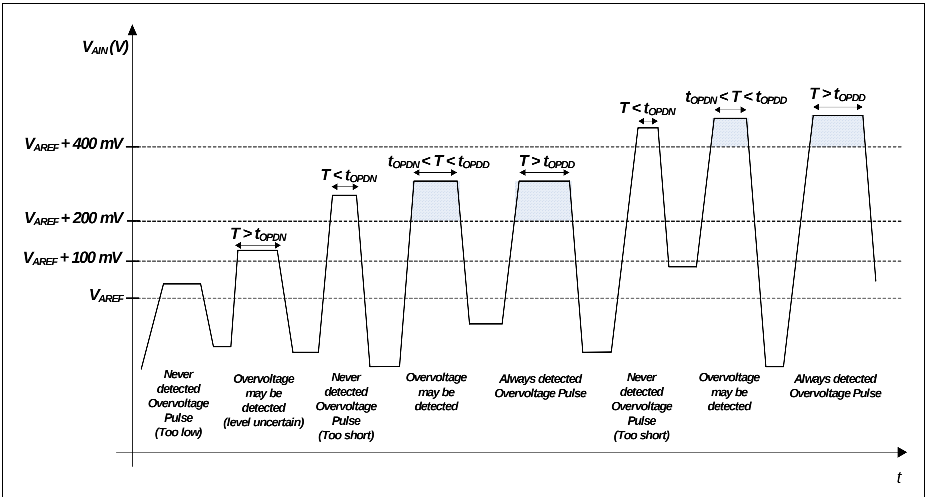



**Figure 19 ORC Detection Ranges**

### 3.2.8 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

If not stated otherwise, the operating conditions for the parameters in the following table are:
$V_{DDP}$ = 3.3 V, $T_A$ = 25 °C

**Table 32 Power Supply Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Active supply current[1)10)] Peripherals enabled Frequency: $f_{CPU}$ / $f_{PERIPH}$ / $f_{CCU}$ in MHz | $I_{DDPA}$ | CC | – | 122 | – | mA | 120 / 120 / 120 |
| | | | – | 110 | – | | 120 / 60 / 60 |
| | | | – | 85 | – | | 60 / 60 / 120 |
| | | | – | 65 | – | | 24 / 24 / 24 |
| | | | – | 52 | – | | 1 / 1 / 1 |
| Active supply current Code execution from RAM Flash in Sleep mode | $I_{DDPA}$ | CC | – | 98 | – | mA | 120 / 120 / 120 |
| | | | – | 80 | – | | 120 / 60 / 60 |
| Active supply current[2)] Peripherals disabled Frequency: $f_{CPU}$ / $f_{PERIPH}$ / $f_{CCU}$ in MHz | $I_{DDPA}$ | CC | – | 115 | – | mA | 120 / 120 / 120 |
| | | | – | 105 | – | | 120 / 60 / 60 |
| | | | – | 80 | – | | 60 / 60 / 120 |
| | | | – | 63 | – | | 24 / 24 / 24 |
| | | | – | 50 | – | | 1 / 1 / 1 |
| Sleep supply current[3)] Peripherals enabled Frequency: $f_{CPU}$ / $f_{PERIPH}$ / $f_{CCU}$ in MHz | $I_{DDPS}$ | CC | – | 115 | – | mA | 120 / 120 / 120 |
| | | | – | 105 | – | | 120 / 60 / 60 |
| | | | – | 83 | – | | 60 / 60 / 120 |
| | | | – | 60 | – | | 24 / 24 / 24 |
| | | | – | 48 | – | | 1 / 1 / 1 |
| $f_{CPU}$ / $f_{PERIPH}$ / $f_{CCU}$ in kHz | | | – | 46 | – | | 100 / 100 / 100 |

2) Maximum threshold for reset deassertion.
3) The $V_{DDP}$ monitoring has a typical hysteresis of $V_{PORHYS}$ = 180 mV.
4) If $t_{PR}$ is not met, low spikes on $\overline{PORST}$ may be seen during start up (e.g. reset pulses generated by the supply monitoring due to a slow ramping $V_{DDP}$).

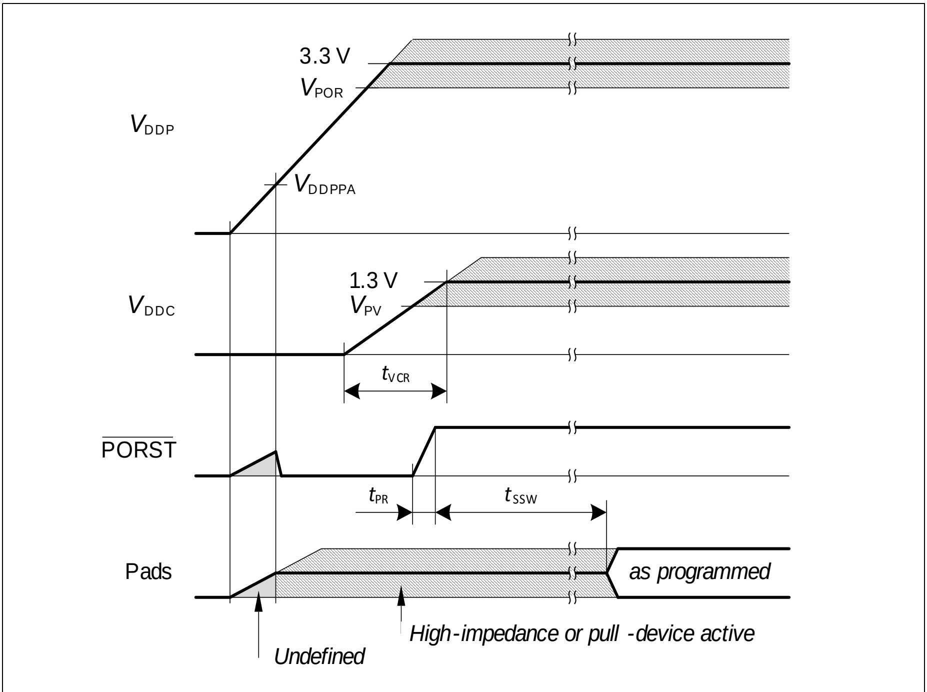



**Figure 26 Power-Up Behavior**

### 3.3.3 Power Sequencing

While starting up and shutting down as well as when switching power modes of the system it is important to limit the current load steps. A typical cause for such load steps is changing the CPU frequency $f_{CPU}$. Load steps exceeding the below defined values may cause a power on reset triggered by the supply monitor.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

### 3.3.8 Embedded Trace Macro Cell (ETM) Timing

The data timing refers to the active clock edge. The XMC4500 ETM uses the half-rate clocking mode. In this mode both, the rising and falling clock edges are active clock edges.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

*Note: Operating conditions apply, with $C_L \leq 15$ pF.*

**Table 41 ETM Interface Timing Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| TRACECLK period | $t_1$ | CC | 16.7 | – | – | ns | – |
| TRACECLK high time | $t_2$ | CC | 2 | – | – | ns | – |
| TRACECLK low time | $t_3$ | CC | 2 | – | – | ns | – |
| TRACECLK and TRACEDATA rise time | $t_4$ | CC | – | – | 3 | ns | – |
| TRACECLK and TRACEDATA fall time | $t_5$ | CC | – | – | 3 | ns | – |
| TRACEDATA output valid time | $t_6$ | CC | -2 | – | 3 | ns | – |

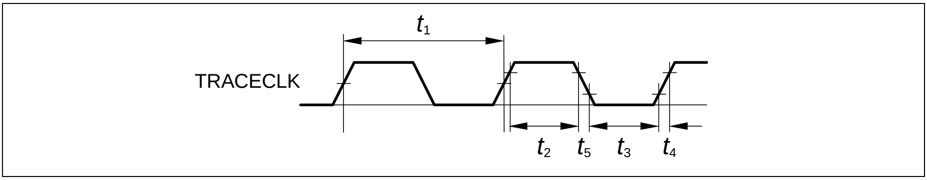



**Figure 30 ETM Clock Timing**

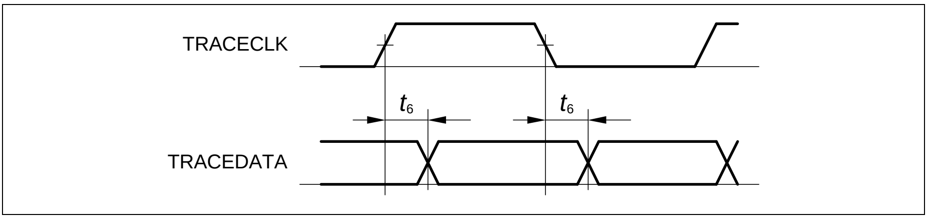



**Figure 31 ETM Data Timing**

**Table 46 USIC IIC Fast Mode Timing[1)]**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Fall time of both SDA and SCL | $t_1$ CC/SR | 20 + 0.1*$C_b$ [2)] | - | 300 | ns | |
| Rise time of both SDA and SCL | $t_2$ CC/SR | 20 + 0.1*$C_b$ [2)] | - | 300 | ns | |
| Data hold time | $t_3$ CC/SR | 0 | - | - | µs | |
| Data set-up time | $t_4$ CC/SR | 100 | - | - | ns | |
| LOW period of SCL clock | $t_5$ CC/SR | 1.3 | - | - | µs | |
| HIGH period of SCL clock | $t_6$ CC/SR | 0.6 | - | - | µs | |
| Hold time for (repeated) START condition | $t_7$ CC/SR | 0.6 | - | - | µs | |
| Set-up time for repeated START condition | $t_8$ CC/SR | 0.6 | - | - | µs | |
| Set-up time for STOP condition | $t_9$ CC/SR | 0.6 | - | - | µs | |
| Bus free time between a STOP and START condition | $t_{10}$ CC/SR | 1.3 | - | - | µs | |
| Capacitive load for each bus line | $C_b$ SR | - | - | 400 | pF | |

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2) $C_b$ refers to the total capacitance of one bus line in pF.

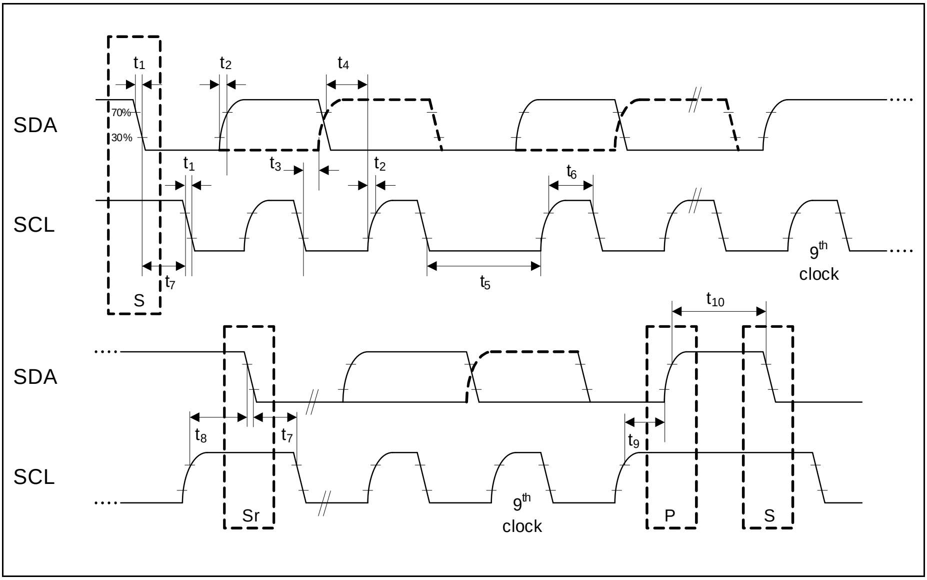



**Figure 34 USIC IIC Stand and Fast Mode Timing**

### 3.3.9.4 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 47 USIC IIS Master Transmitter Timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Clock period | $t_1$ CC | 33.3 | – | – | ns | |
| Clock high time | $t_2$ CC | 0.35 x $t_{1min}$ | – | – | ns | |
| Clock low time | $t_3$ CC | 0.35 x $t_{1min}$ | – | – | ns | |
| Hold time | $t_4$ CC | 0 | – | – | ns | |
| Clock rise time | $t_5$ CC | – | – | 0.15 x $t_{1min}$ | ns | |

With clock delay:

(2)

$$t_{ODLY\_F} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ISU} < t_{WL} + t_{CLK\_DELAY}$$

(3)

$$t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{WL} < t_{PP} + t_{CLK\_DELAY} - t_{ISU} - t_{ODLY\_F}$$

$$t_{DATA\_DELAY} + t_{TAP\_DELAY} + 20 < 40 + t_{CLK\_DELAY} - 5 - 10$$

$$t_{DATA\_DELAY} < 5 + t_{CLK\_DELAY} - t_{TAP\_DELAY}$$

The data can be delayed versus clock up to 5 ns in ideal case of $t_{WL}$= 20 ns.

### Full-Speed Write Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

(4)

$$t_{CLK\_DELAY} < t_{WL} + t_{OH\_F} + t_{DATA\_DELAY} + t_{TAP\_DELAY} - t_{IH}$$

$$t_{CLK\_DELAY} < 20 + t_{DATA\_DELAY} + t_{TAP\_DELAY} - 5$$

$$t_{DATA\_DELAY} < 15 + t_{CLK\_DELAY} + t_{TAP\_DELAY}$$

The clock can be delayed versus data up to 18.2 ns (external delay line) in ideal case of $t_{WL}$= 20 ns, with maximum $t_{TAP\_DELAY}$ = 3.2 ns programmed.

**Table 52 SD Card Bus Timing for High-Speed Mode[1)]**

| Parameter | Symbol | Values | | Unit | Note/ Test Condition |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| SD card input setup time | $t_{ISU}$ | 6 | – | ns | |
| SD card input hold time | $t_{IH}$ | 2 | – | ns | |
| SD card output valid time | $t_{ODLY}$ | – | 14 | ns | |
| SD card output hold time | $t_{OH}$ | 2.5 | – | ns | |

1) Reference card timing values for calculation examples. Not subject to production test and not characterized.

### High-Speed Output Path (Write)

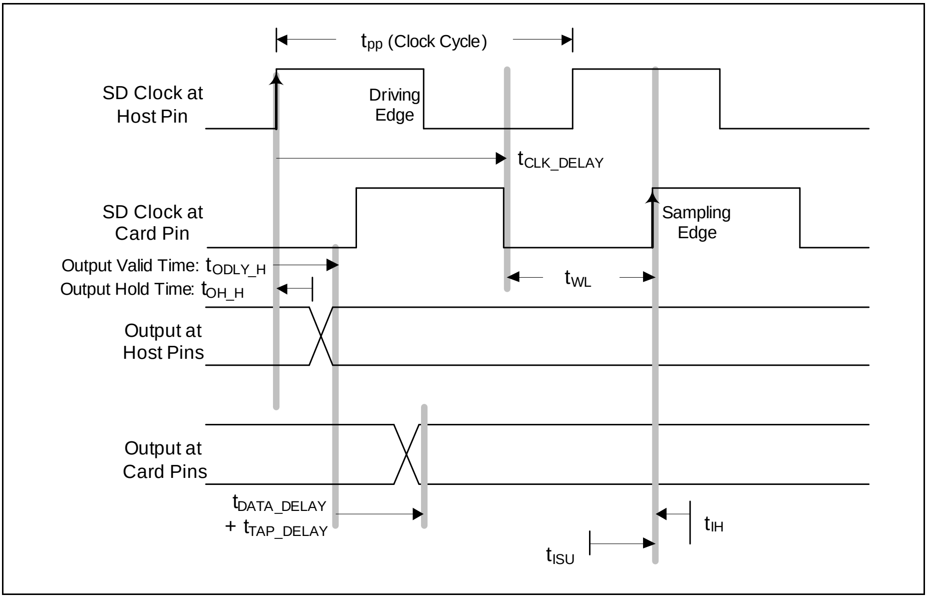



**Figure 39 High-Speed Output Path**

### High-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

**High-Speed Read Meeting Hold (Minimum Delay)**

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

(12)

$$t_{CLK\_DELAY} + t_{OH} + t_{DATA\_DELAY} + t_{TAP\_DELAY} > t_{IH\_H}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} > t_{IH\_H} - t_{OH} - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} > 2 - 2{,}5 - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} > -0{,}5 - t_{TAP\_DELAY}$$

The data + clock delay must be greater than -0.5 ns for a 20 ns clock cycle. This is always fulfilled.

### 3.3.10 EBU Timing

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

*Note: Operating Conditions apply, with Class A2 pins and $C_L$ = 16 pF.*

#### 3.3.10.1 EBU Asynchronous Timing

*Note: For each timing, the accumulated PLL jitter must be added separately.*

**Table 53 Common Timing Parameters for all Asynchronous Timings**

| Parameter | | | Symbol | Limit Values | | Unit | Edge Setting |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | | |
| Pulse width deviation from the ideal programmed width due to the A2 pad asymmetry, strong driver mode, rise delay - fall delay. $C_L$ = 16 pF. | | CC | $t_a$ | -1 | 1.5 | ns | sharp |
| | | | | -2 | 1 | | medium |
| AD(24:16) output delay | to $\overline{ADV}$ rising edge, multiplexed read / write | CC | $t_{13}$ | -5.5 | 2 | | – |
| AD(24:16) output delay | | CC | $t_{14}$ | -5.5 | 2 | | – |

3) If the clock feedback is not enabled, the input signals are latched using the internal clock in the same way as for asynchronous access. Thus, $t_5$, $t_6$, $t_7$ and $t_8$ from the asynchronous timing apply.

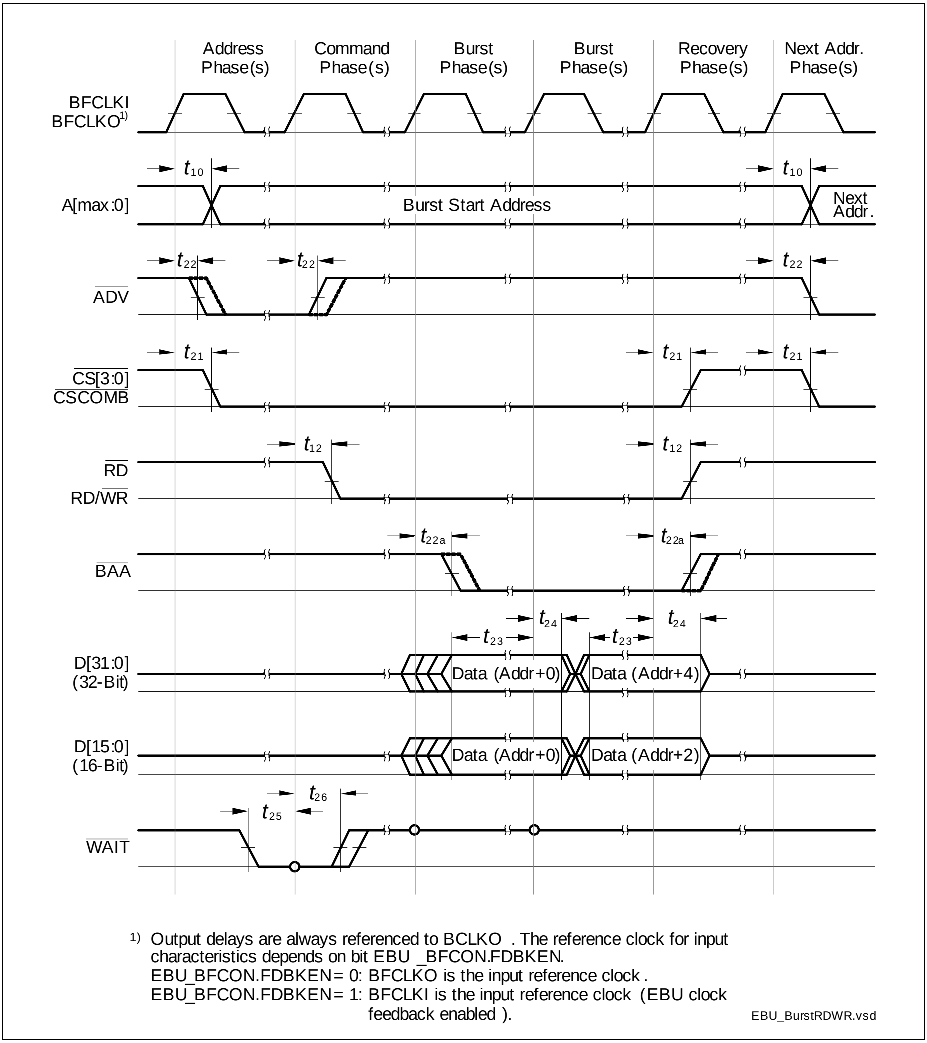
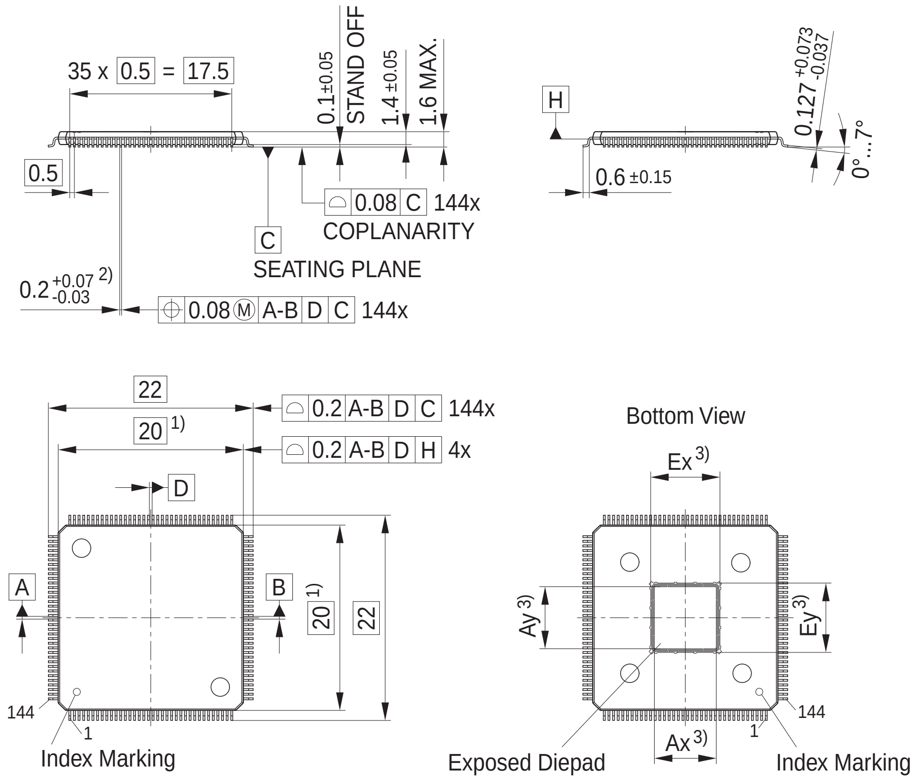



**Figure 45 EBU Burst Mode Read / Write Access Timing**




1) Does not include plastic or metal protrusion of 0.25 max. per side
2) Does not include dambar protrusion
3) Refer table for exposed pad dimension

**Figure 56** **PG-LQFP-144-24** (Plastic Green Low Profile Quad Flat Package)