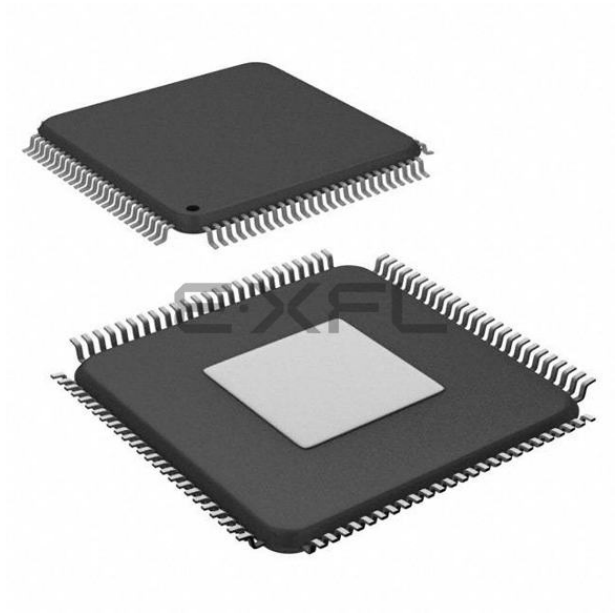
Infineon Technologies - XMC4500F100K1024ABXQSA1 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, SPI, UART, USB
Peripherals	DMA, I²S, LED, POR, PWM, WDT
Number of I/O	55
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-11
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4500f100k1024abxqsa1

- Flexible CRC Engine (FCE) for multiple bit error detection

On-Chip Memories

- 16 KB on-chip boot ROM
- 64 KB on-chip high-speed program memory
- 64 KB on-chip high speed data memory
- 32 KB on-chip high-speed communication
- 1024 KB on-chip Flash Memory with 4 KB instruction cache

Communication Peripherals

- Ethernet MAC module capable of 10/100 Mbit/s transfer rates
- Universal Serial Bus, USB 2.0 host, Full-Speed OTG, with integrated PHY
- Controller Area Network interface (MultiCAN), Full-CAN/Basic-CAN with 3 nodes, 64 message objects (MO), data rate up to 1MBit/s
- Six Universal Serial Interface Channels (USIC),providing 6 serial channels, usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces
- LED and Touch-Sense Controller (LEDTS) for Human-Machine interface
- SD and Multi-Media Card interface (SDMMC) for data storage memory cards
- External Bus Interface Unit (EBU) enabling communication with external memories and off-chip peripherals

Analog Frontend Peripherals

- Four Analog-Digital Converters (VADC) of 12-bit resolution, 8 channels each, with input out-of-range comparators
- Delta Sigma Demodulator with four channels, digital input stage for A/D signal conversion
- Digital-Analogue Converter (DAC) with two channels of 12-bit resolution

Industrial Control Peripherals

- Two Capture/Compare Units 8 (CCU8) for motor control and power conversion
- Four Capture/Compare Units 4 (CCU4) for use as general purpose timers
- Two Position Interfaces (POSIF) for servo motor positioning
- Window Watchdog Timer (WDT) for safety sensitive applications
- Die Temperature Sensor (DTS)
- Real Time Clock module with alarm support
- System Control Unit (SCU) for system configuration and control

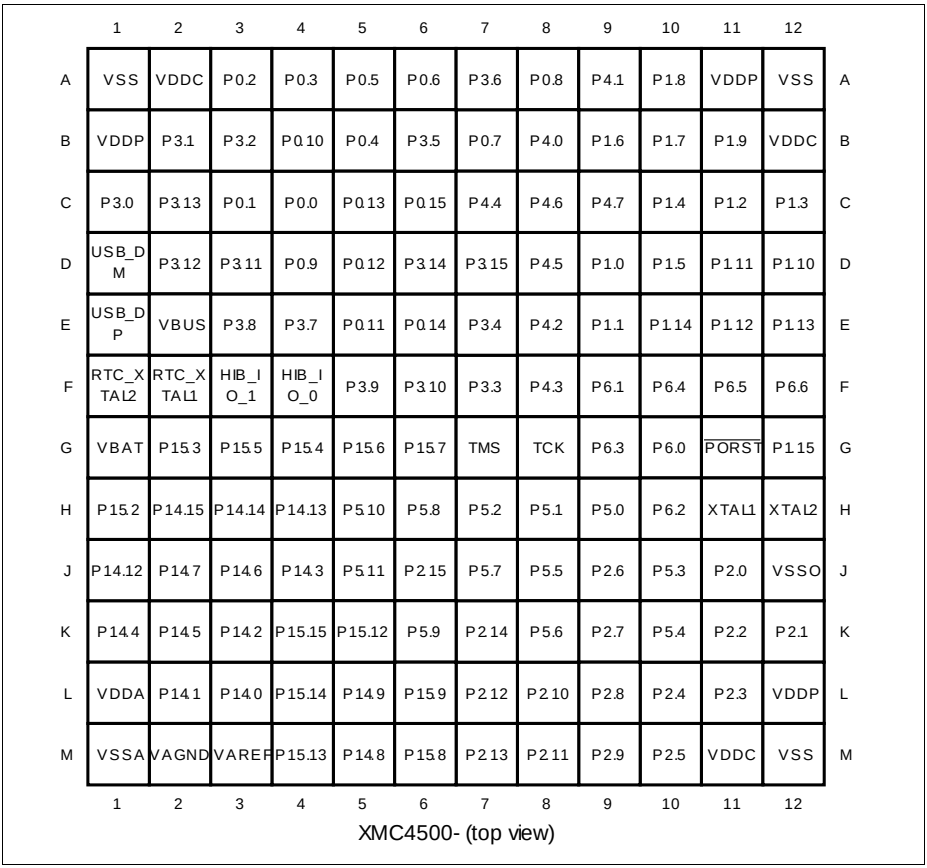

Figure 6 XMC4500 PG-LFBGA-144 Pin Configuration (top view)

2.2.2 Port I/O Functions

The following general scheme is used to describe each Port pin:

Table 10 Port I/O Function Description

Function	Outputs			Inputs		
	ALT1	ALTn	HWO0	HWI0	Input	Input
P0.0		MODA.OUT	MODB.OUT	MODB.INA	MODC.INA	
Pn.y	MODA.OUT				MODA.INA	MODC.INB

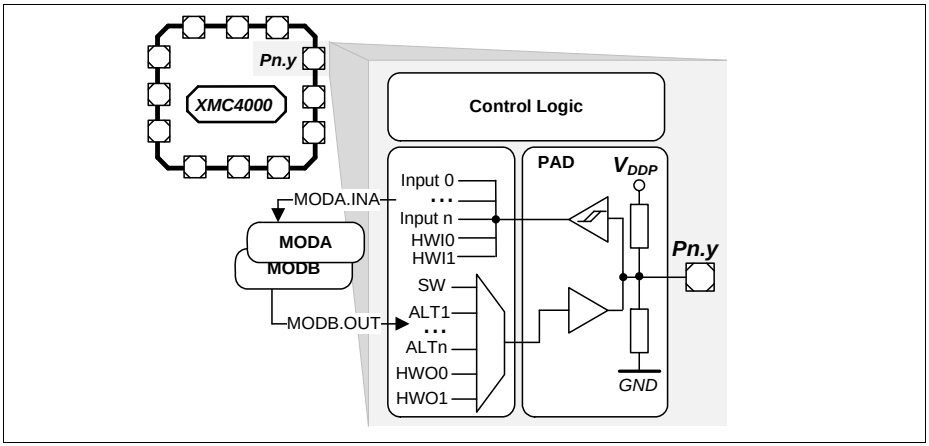

Figure 8 Simplified Port Structure

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to four alternate output functions (ALT1/2/3/4) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.
The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

By Pn_HWSEL it is possible to select between different hardware “masters” (HWO0/HWI0, HWO1/HWI1). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers.

Table 11 Port I/O Functions (cont'd)

Function	Outputs						Inputs									
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P4.3	U2C1. SELO2	U0C0. SELO5	CCU43. OUT3										CCU43. IN3A			
P4.4		U0C0. SELO4	CCU43. OUT2		U2C1. DOUT3		U2C1. HWIN3						CCU43. IN2A			
P4.5		U0C0. SELO3	CCU43. OUT1		U2C1. DOUT2		U2C1. HWIN2						CCU43. IN1A			
P4.6		U0C0. SELO2	CCU43. OUT0		U2C1. DOUT1		U2C1. HWIN1		CAN. N2_RXDC				CCU43. IN0A			
P4.7		CAN. N2_TXD			U2C1. DOUT0		U2C1. HWIN0		U0C0. DX0C				CCU43. IN0C			
P5.0	U2C0. DOUT0	DSD. CGPWMN	CCU81. OUT33		U2C0. DOUT0		U2C0. HWIN0		U2C0. DX0B	ETH0. RXD0D	U0C0. DX0D		CCU81. IN0A	CCU81. IN1A	CCU81. IN2A	CCU81. IN3A
P5.1	U0C0. DOUT0	DSD. CGPWMP	CCU81. OUT32		U2C0. DOUT1		U2C0. HWIN1		U2C0. DX0A	ETH0. RXD1D			CCU81. IN0B			
P5.2	U2C0. SCLKOUT		CCU81. OUT23						U2C0. DX1A	ETH0. CRS_DVD			CCU81. IN1B			ETH0. RXDVD
P5.3	U2C0. SELO0		CCU81. OUT22		EBU. CKE	EBU. A20			U2C0. DX2A	ETH0. RXERD			CCU81. IN2B			
P5.4	U2C0. SELO1		CCU81. OUT13		$\overline{\text{EBU.}}$ RAS	EBU. A21				ETH0. CRSD			CCU81. IN3B			
P5.5	U2C0. SELO2		CCU81. OUT12		$\overline{\text{EBU.}}$ CAS	EBU. A22				ETH0. COLD						
P5.6	U2C0. SELO3		CCU81. OUT03		EBU. BFCLKO	EBU. A23			EBU. BFCLKI							
P5.7			CCU81. OUT02	LEDTS0. COLA	U2C0. DOUT2		U2C0. HWIN2									
P5.8		U1C0. SCLKOUT	CCU80. OUT01		EBU. SDCLKO	$\overline{\text{EBU.}}$ CS2			ETH0. RXD2A	U1C0. DX1B						
P5.9		U1C0. SELO0	CCU80. OUT20	ETH0. TX_EN	EBU. BFCLKO	$\overline{\text{EBU.}}$ CS3			ETH0. RXD3A	U1C0. DX2B						
P5.10		U1C0. MCLKOUT	CCU80. OUT10	LEDTS0. LINE7	LEDTS0. EXTENDED7		LEDTS0. TSIN7A		ETH0. CLK_TXA							
P5.11		U1C0. SELO1	CCU80. OUT00						ETH0. CRSA							
P6.0	ETH0. TXD2	U0C1. SELO1	CCU81. OUT31		DB. ETM_TRACECLK	EBU. A16										
P6.1	ETH0. TXD3	U0C1. SELO0	CCU81. OUT30		DB. ETM_TRACEDATA3	EBU. A17			U0C1. DX2C							
P6.2	ETH0. TXER	U0C1. SCLKOUT	CCU43. OUT3		DB. ETM_TRACEDATA2	EBU. A18			U0C1. DX1C							
P6.3			CCU43. OUT2						U0C1. DX0C	ETH0. RXD3B						
P6.4		U0C1. DOUT0	CCU43. OUT1		EBU. SDCLKO	EBU. A19			EBU. SDCLKI	ETH0. RXD2B						
P6.5		U0C1. MCLKOUT	CCU43. OUT0		DB. ETM_TRACEDATA1	$\overline{\text{EBU.}}$ BC2			DSD. DIN3A	ETH0. CLK_RMIID						ETH0. CLKRXD

Table 14 PN-Junction Characterisitics for positive Overload

Pad Type	I_{OV} = 5 mA, T_J = -40 °C	I_{OV} = 5 mA, T_J = 150 °C
A1 / A1+	$V_{IN} = V_{DDP}$ + 1.0 V	$V_{IN} = V_{DDP}$ + 0.75 V
A2	$V_{IN} = V_{DDP}$ + 0.7 V	$V_{IN} = V_{DDP}$ + 0.6 V
AN/DIG_IN	$V_{IN} = V_{DDP}$ + 1.0 V	$V_{IN} = V_{DDP}$ + 0.75 V

Table 15 PN-Junction Characterisitics for negative Overload

Pad Type	I_{OV} = 5 mA, T_J = -40 °C	I_{OV} = 5 mA, T_J = 150 °C
A1 / A1+	$V_{IN} = V_{SS}$ - 1.0 V	$V_{IN} = V_{SS}$ - 0.75 V
A2	$V_{IN} = V_{SS}$ - 0.7 V	$V_{IN} = V_{SS}$ - 0.6 V
AN/DIG_IN	$V_{IN} = V_{DDP}$ - 1.0 V	$V_{IN} = V_{DDP}$ - 0.75 V

Table 16 Port Groups for Overload and Short-Circuit Current Sum Parameters

Group	Pins
1	P0.[15:0], P3.[15:0]
2	P14.[15:0], P15.[15:0]
3	P2.[15:0], P5.[11:0]
4	P1.[15:0], P4.[7:0], P6.[6:0]

3.2 DC Parameters

3.2.1 Input/Output Pins

The digital input stage of the shared analog/digital input pins is identical to the input stage of the standard digital input/output pins.
The Pull-up on the $\overline{\text{PORST}}$ pin is identical to the Pull-up on the standard digital input/output pins.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 19 Standard Pad Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Pin capacitance (digital inputs/outputs)	C_{IO} CC	–		10	pF	
Pull-down current	$\lvert I_{PDL}\rvert$ CC	150		–	µA	1) $V_{IN} \geq 0.6 \times V_{DDP}$
		–		10	µA	2) $V_{IN} \leq 0.36 \times V_{DDP}$
Pull-Up current	$\lvert I_{PUH}\rvert$ CC	–		10	µA	2) $V_{IN} \geq 0.6 \times V_{DDP}$
		100		–	µA	1) $V_{IN} \leq 0.36 \times V_{DDP}$
Input Hysteresis for pads of all A classes[3]	$HYSA$ CC	$0.1 \times V_{DDP}$		–	V	
$\overline{\text{PORST}}$ spike filter always blocked pulse duration	t_{SF1} CC	–		10	ns	
$\overline{\text{PORST}}$ spike filter pass-through pulse duration	t_{SF2} CC	100		–	ns	
$\overline{\text{PORST}}$ pull-down current	$\lvert I_{PPD}\rvert$ CC	13		–	mA	V_{IN} = 1.0 V

1) Current required to override the pull device with the opposite logic level (“force current”). With active pull device, at load currents between force and keep current the input state is undefined.

2) Load current at which the pull device still maintains the valid logic level (“keep current”). With active pull device, at load currents between force and keep current the input state is undefined.

3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

Table 25 DAC Parameters (Operating Conditions apply) (cont'd)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Offset error	ED_{OFF}	CC		±20		mV	
Gain error	ED_{G_IN}	CC	-6.5	-1.5	3	%	
Startup time	$t_{STARTUP}$	CC	–	15	30	µs	time from output enabling till code valid ±16 LSB
3dB Bandwidth of Output Buffer	f_{C1}	CC	2.5	5	–	MHz	verified by design
Output sourcing current	I_{OUT_SOURCE}	CC	–	-30	–	mA	
Output sinking current	I_{OUT_SINK}	CC	–	0.6	–	mA	
Output resistance	R_{OUT}	CC	–	50	–	Ohm	
Load resistance	R_L	SR	5	–	–	kOhm	
Load capacitance	C_L	SR	–	–	50	pF	
Signal-to-Noise Ratio	*SNR*	CC	–	70	–	dB	examination bandwidth < 25 kHz
Total Harmonic Distortion	*THD*	CC	–	70	–	dB	examination bandwidth < 25 kHz
Power Supply Rejection Ratio	*PSRR*	CC	–	56	–	dB	to V_{DDA} verified by design

Conversion Calculation

Unsigned:

DACxDATA = 4095 × (V_{OUT} - V_{OUT_MIN}) / (V_{OUT_MAX} - V_{OUT_MIN})

Signed:

DACxDATA = 4095 × (V_{OUT} - V_{OUT_MIN}) / (V_{OUT_MAX} - V_{OUT_MIN}) - 2048

3.2.8 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

If not stated otherwise, the operating conditions for the parameters in the following table are:
V_{DDP} = 3.3 V, T_A = 25 °C

Table 32 Power Supply Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Active supply current[1)10)] Peripherals enabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPA}	CC	–	122	–	mA	120 / 120 / 120
			–	110	–		120 / 60 / 60
			–	85	–		60 / 60 / 120
			–	65	–		24 / 24 / 24
			–	52	–		1 / 1 / 1
Active supply current Code execution from RAM Flash in Sleep mode	I_{DDPA}	CC	–	98	–	mA	120 / 120 / 120
			–	80	–		120 / 60 / 60
Active supply current[2)] Peripherals disabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPA}	CC	–	115	–	mA	120 / 120 / 120
			–	105	–		120 / 60 / 60
			–	80	–		60 / 60 / 120
			–	63	–		24 / 24 / 24
			–	50	–		1 / 1 / 1
Sleep supply current[3)] Peripherals enabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPS}	CC	–	115	–	mA	120 / 120 / 120
			–	105	–		120 / 60 / 60
			–	83	–		60 / 60 / 120
			–	60	–		24 / 24 / 24
			–	48	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz			–	46	–		100 / 100 / 100

Table 35 Power Sequencing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Positive Load Step Current	ΔI_{PLS} SR	-	–	50	mA	Load increase on V_{DDP} $\Delta t \leq 10$ ns
Negative Load Step Current	ΔI_{NLS} SR	-	–	150	mA	Load decrease on V_{DDP} $\Delta t \leq 10$ ns
V_{DDC} Voltage Over- / Undershoot from Load Step	ΔV_{LS} CC	-	–	±100	mV	For maximum positive or negative load step
Positive Load Step Settling Time	t_{PLSS} SR	50	–	-	µs	
Negative Load Step Settling Time	t_{NLSS} SR	100	–	-	µs	
External Buffer Capacitor on V_{DDC}	C_{EXT} SR	-	10	-	µF	In addition C = 100 nF capacitor on each V_{DDC} pin

Positive Load Step Examples

System assumptions:
$f_{CPU} = f_{SYS}$, target frequency f_{CPU} = 120 MHz, main PLL f_{VCO} = 480 MHz, stepping done by K2 divider, t_{PLSS} between individual steps:

24 MHz - 48 MHz - 68 MHz - 96 MHz - 120 MHz (K2 steps 20 - 10 - 7 - 5 - 4)
24 MHz - 68 MHz - 96 MHz - 120 MHz (K2 steps 20 - 7 - 5 - 4)
24 MHz - 68 MHz - 120 MHz (K2 steps 20 - 7 - 4)

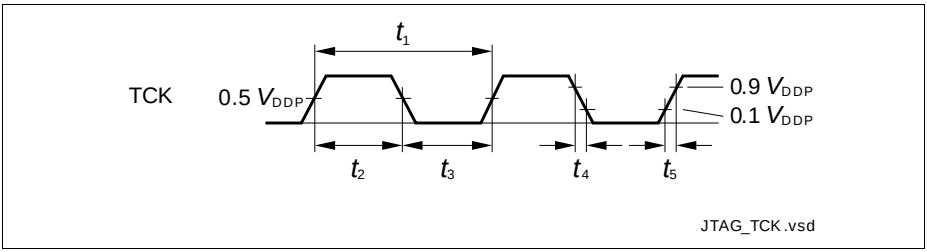

Figure 27 Test Clock Timing (TCK)

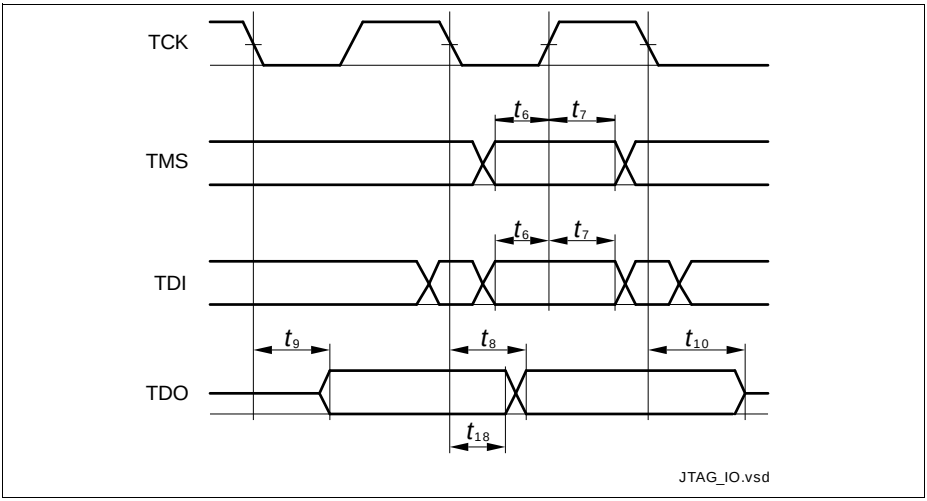

Figure 28 JTAG Timing

Table 46 USIC IIC Fast Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	20 + 0.1*C_b [2)]	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	20 + 0.1*C_b [2)]	-	300	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	100	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	1.3	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	0.6	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	0.6	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	0.6	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	0.6	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	1.3	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2) C_b refers to the total capacitance of one bus line in pF.

3.3.9.5 SDMMC Interface Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply, total external capacitive load C_L = 40 pF.

AC Timing Specifications (Full-Speed Mode)

Table 49 SDMMC Timing for Full-Speed Mode

Parameter	Symbol		Values		Unit	Note/ Test Condition
			Min.	Max.		
Clock frequency in full speed transfer mode ($1/t_{pp}$)	f_{pp}	CC	0	24	MHz	
Clock cycle in full speed transfer mode	t_{pp}	CC	40	–	ns	
Clock low time	t_{WL}	CC	10	–	ns	
Clock high time	t_{WH}	CC	10	–	ns	
Clock rise time	t_{TLH}	CC	–	10	ns	
Clock fall time	t_{THL}	CC	–	10	ns	
Inputs setup to clock rising edge	t_{ISU_F}	SR	2	–	ns	
Inputs hold after clock rising edge	t_{IH_F}	SR	2	–	ns	
Outputs valid time in full speed mode	t_{ODLY_F}	CC	–	10	ns	
Outputs hold time in full speed mode	t_{OH_F}	CC	0	–	ns	

Table 50 SD Card Bus Timing for Full-Speed Mode[1)]

Parameter	Symbol	Values		Unit	Note/ Test Condition
		Min.	Max.		
SD card input setup time	t_{ISU}	5	–	ns	
SD card input hold time	t_{IH}	5	–	ns	

Table 50 SD Card Bus Timing for Full-Speed Mode[1)] (cont'd)

Parameter	Symbol	Values		Unit	Note/ Test Condition
		Min.	Max.		
SD card output valid time	t_{ODLY}	–	14	ns	
SD card output hold time	t_{OH}	0	–	ns	

1) Reference card timing values for calculation examples. Not subject to production test and not characterized.

Full-Speed Output Path (Write)

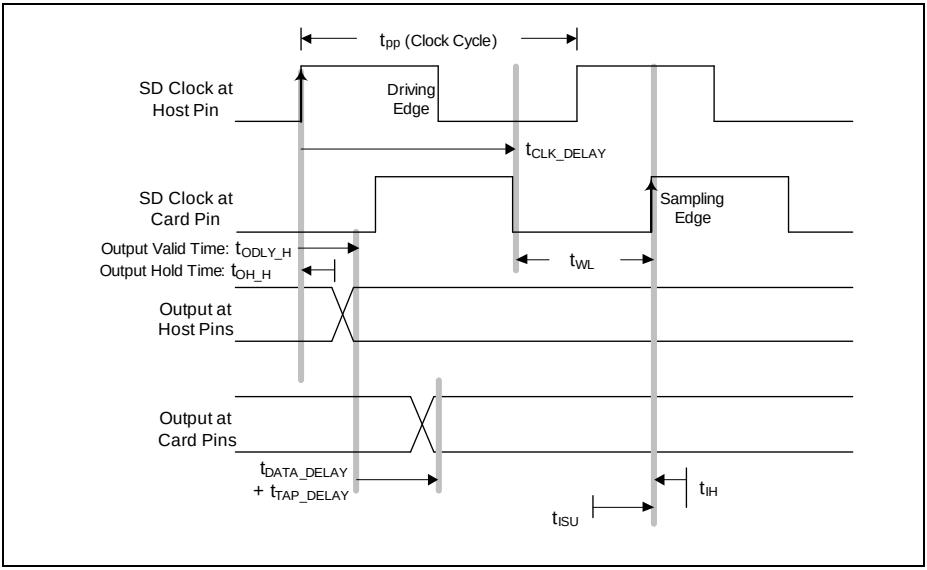

Figure 37 Full-Speed Output Path

Full-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

No clock delay:

(1)

$$t_{ODLY\_F} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ISU} < t_{WL}$$

Table 52 SD Card Bus Timing for High-Speed Mode[1)]

Parameter	Symbol	Values		Unit	Note/ Test Condition
		Min.	Max.		
SD card input setup time	t_{ISU}	6	–	ns	
SD card input hold time	t_{IH}	2	–	ns	
SD card output valid time	t_{ODLY}	–	14	ns	
SD card output hold time	t_{OH}	2.5	–	ns	

1) Reference card timing values for calculation examples. Not subject to production test and not characterized.

High-Speed Output Path (Write)

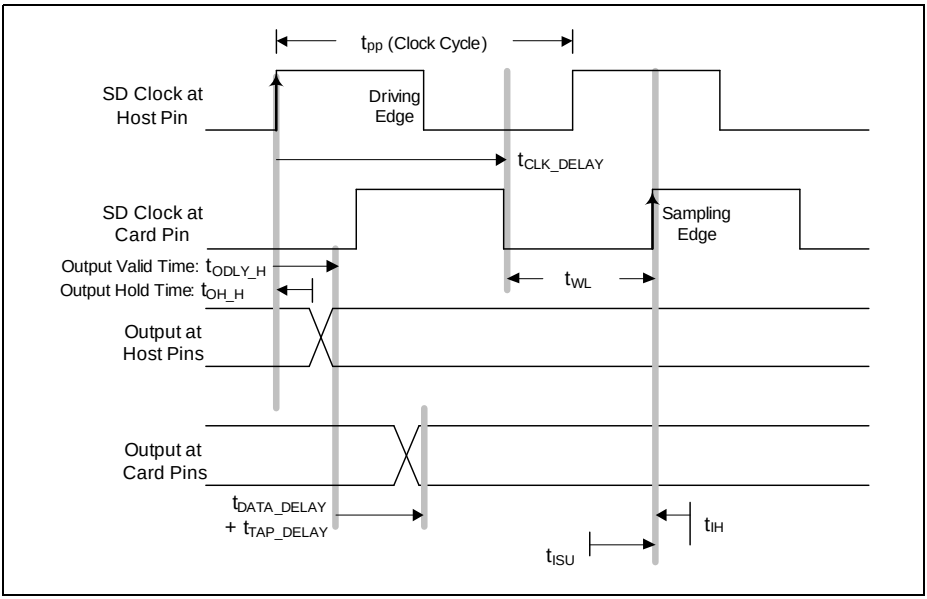

Figure 39 High-Speed Output Path

High-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

Multiplexed Read Timing

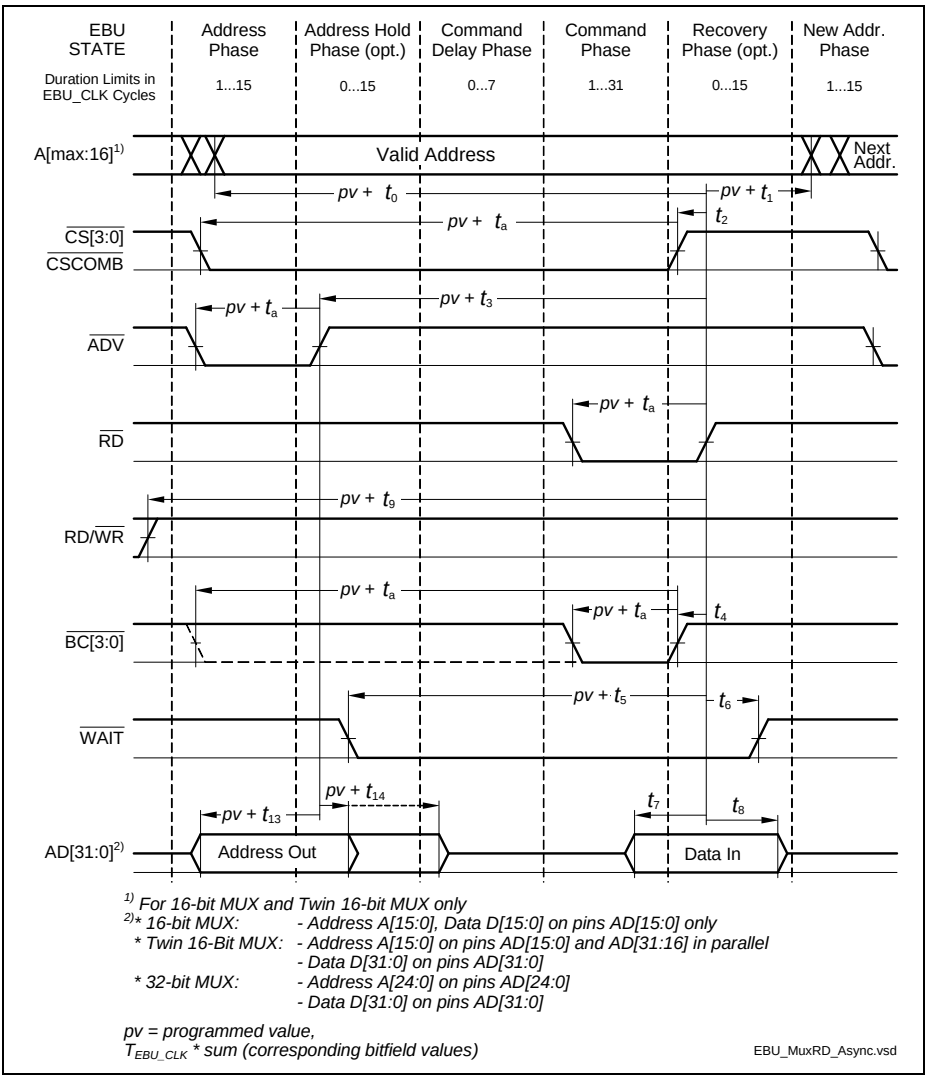

Figure 41 Multiplexed Read Access

3.3.10.3 EBU Arbitration Signal Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 57 EBU Arbitration Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Output delay from BFCLKO rising edge	t_1	CC	–	–	16	ns	C_L = 50 pF
Data setup to BFCLKO falling edge	t_2	SR	11	–	–	ns	–
Data hold from BFCLKO falling edge	t_3	SR	2	–	–	ns	–

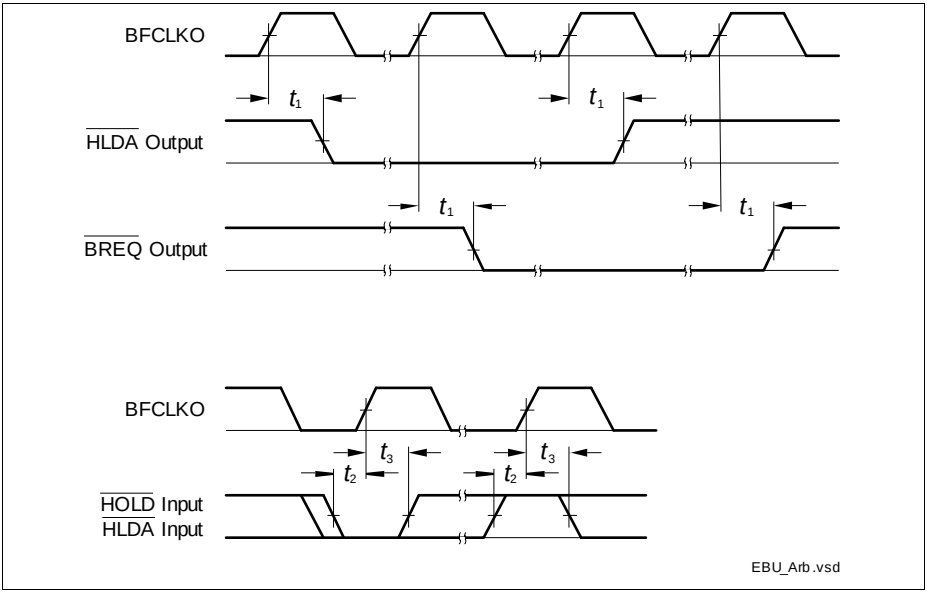

Figure 46 EBU Arbitration Signal Timing

3.3.12.3 ETH MII Parameters

In the following, the parameters of the MII (Media Independent Interface) are described.

Table 62 ETH MII Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Clock period, 10 Mbps	t_7	SR	400	–	–	ns	C_L = 25 pF
Clock high time, 10 Mbps	t_8	SR	140	–	260	ns	
Clock low time, 10 Mbps	t_9	SR	140	–	260	ns	
Clock period, 100 Mbps	t_7	SR	40	–	–	ns	
Clock high time, 100 Mbps	t_8	SR	14	–	26	ns	
Clock low time, 100 Mbps	t_9	SR	14	–	26	ns	
Input setup time	t_{10}	SR	10	–	–	ns	
Input hold time	t_{11}	SR	10	–	–	ns	
Output valid time	t_{12}	CC	0	–	25	ns	

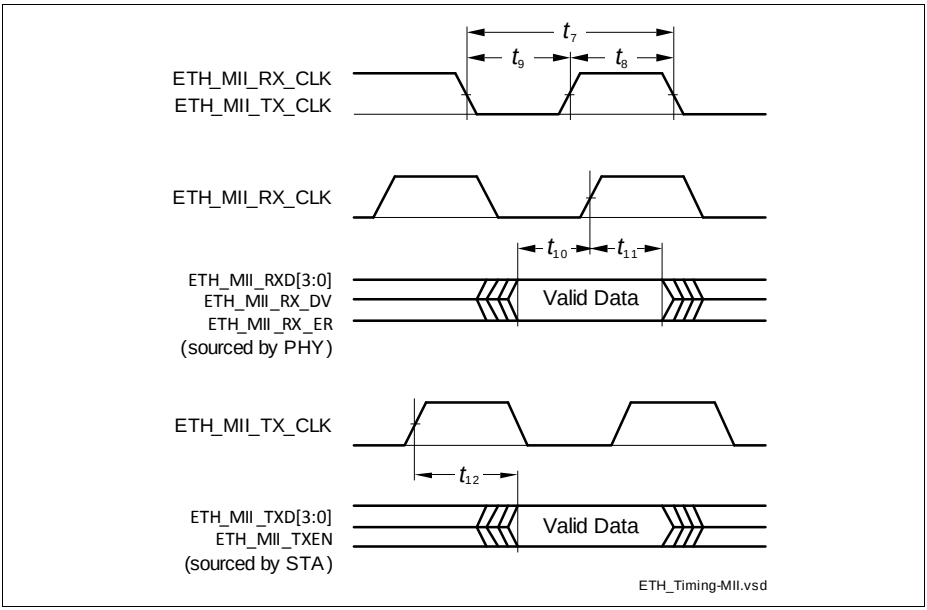

Figure 53 ETH MII Signal Timing

Table 66 Differences PG-LQFP-100-11 to PG-LQFP-100-24

Change	PG-LQFP-100-11	PG-LQFP-100-25
Thermal Resistance Junction Ambient ($R_{\Theta JA}$)	23.0 K/W	19.5 K/W
Lead Width	$0.22^{\pm 0.05}$ mm	$0.2^{+0.07}_{-0.03}$ mm
Lead Thickness	$0.15^{+0.05}_{-0.06}$ mm	$0.127^{+0.073}_{-0.037}$ mm
Exposed Die Pad outer dimensions	7.0 mm × 7.0 mm	7.0 mm × 7.0 mm
Exposed Die Pad U-Groove inner dimensions	n.a.	6.2 mm × 6.2 mm

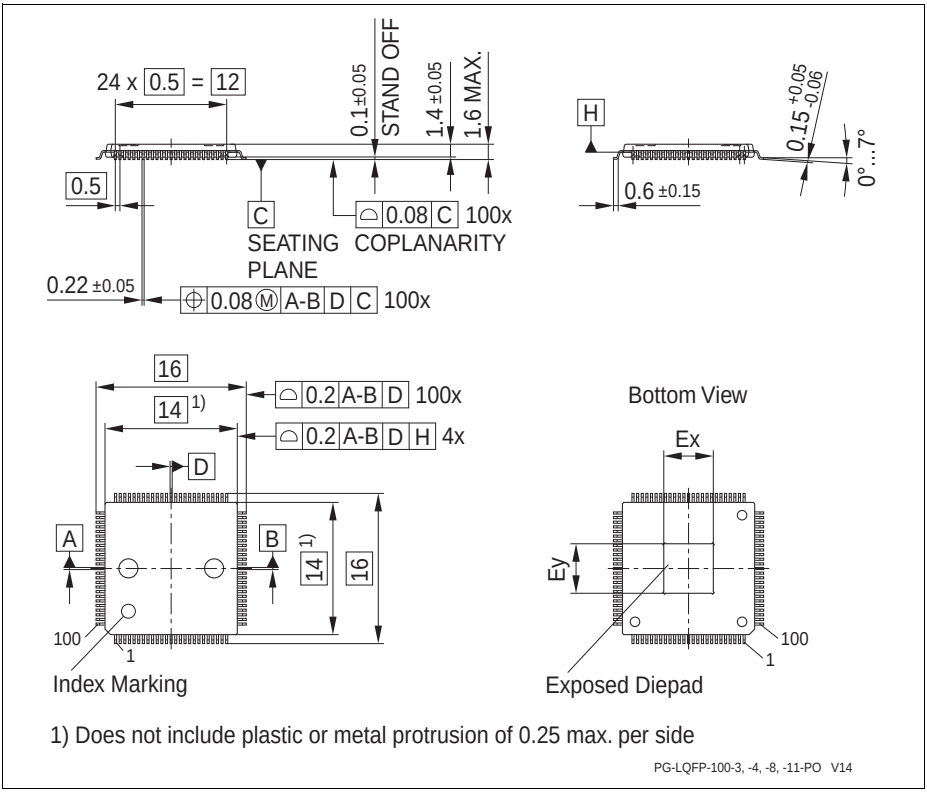

Figure 57 PG-LQFP-100-11 (Plastic Green Low Profile Quad Flat Package)

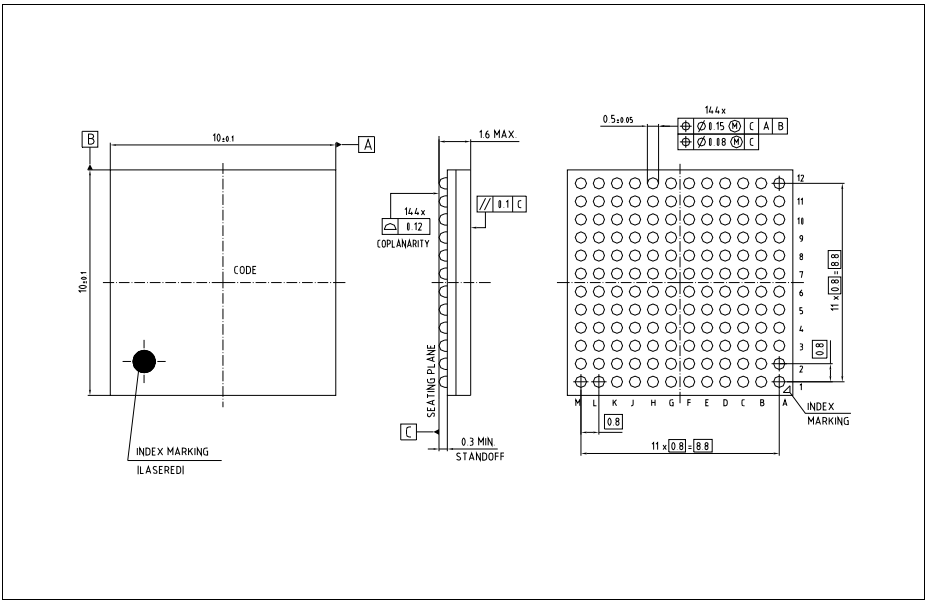

Figure 59 PG-LFBGA-144-10 (Plastic Green Low Profile Fine Pitch Ball Grid Array)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page “Packages”: **http://www.infineon.com/packages**

4.3 Quality Declarations

The qualification of the XMC4500 is executed according to the JEDEC standard JESD47H.

Note: For automotive applications refer to the Infineon automotive microcontrollers.

Table 67 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation lifetime	t_{OP} CC	20	–	–	a	$T_J \leq 109°C$, device permanent on
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	–	–	2 000	V	EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM} SR	–	–	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	–	–	3	–	JEDEC J-STD-020D
Soldering temperature	T_{SDR} SR	–	–	260	°C	Profile according to JEDEC J-STD-020D