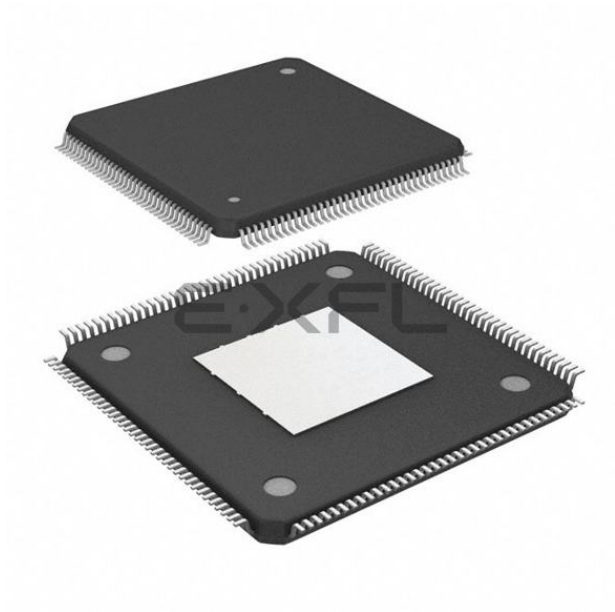
# Infineon Technologies - XMC4500F144F768ACXQMA1 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 120MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, LINbus, SPI, UART, USB |
| Peripherals | DMA, I²S, LED, POR, PWM, WDT |
| Number of I/O | 91 |
| Program Memory Size | 768KB (768K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 160K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3.13V ~ 3.63V |
| Data Converters | A/D 32x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP Exposed Pad |
| Supplier Device Package | PG-LQFP-144-13 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xmc4500f144f768acxqma1 |

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# XMC4500

Microcontroller Series
for Industrial Applications

XMC4000 Family

ARM® Cortex®-M4
32-bit processor core

## Data Sheet

V1.4 2016-01

Microcontrollers

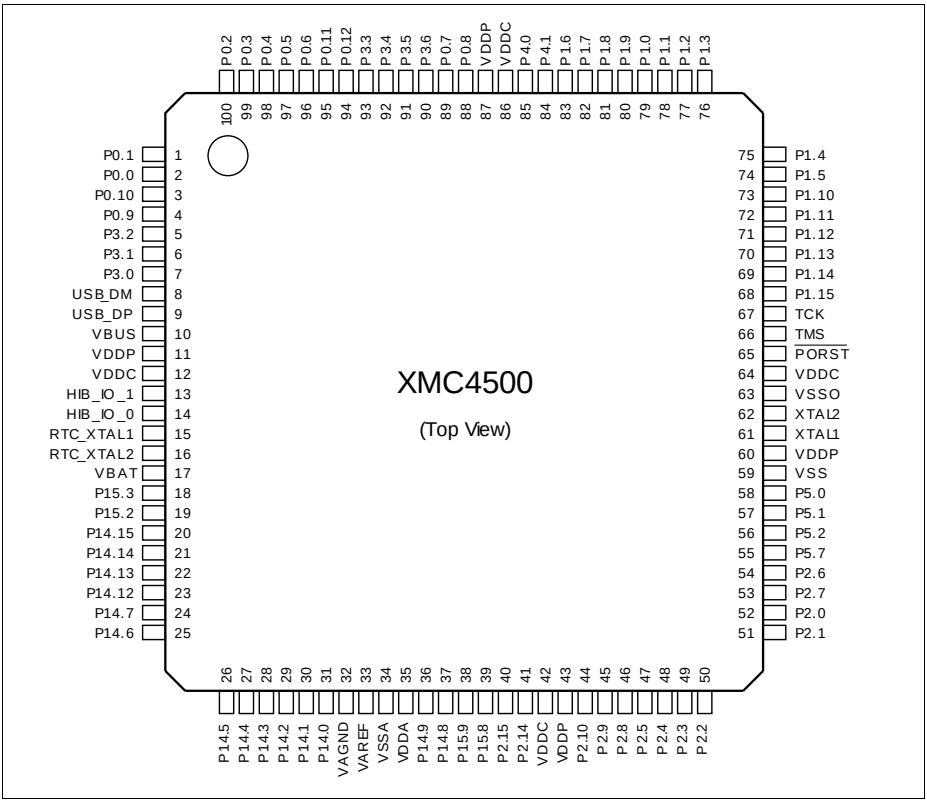


**Figure 7 XMC4500 PG-LQFP-100 Pin Configuration** (top view)

**Table 11 Port I/O Functions** (cont'd)

| Function | Outputs | | | | | | Inputs | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | ALT1 | ALT2 | ALT3 | ALT4 | HWO0 | HWO1 | HWI0 | HWI1 | Input | Input | Input | Input | Input | Input | Input | Input |
| P15.12 | | | | | | | | | | | | VADC. G3CH4 | | | | |
| P15.13 | | | | | | | | | | | | VADC. G3CH5 | | | | |
| P15.14 | | | | | | | | | | | | VADC. G3CH6 | | | | |
| P15.15 | | | | | | | | | | | | VADC. G3CH7 | | | | |
| USB_DP | | | | | | | | | | | | | | | | |
| USB_DM | | | | | | | | | | | | | | | | |
| HIB_IO_0 | HIBOUT | WWDT. SERVICE_OUT | | | | | | | WAKEUPA | | | | | | | |
| HIB_IO_1 | HIBOUT | WWDT. SERVICE_OUT | | | | | | | WAKEUPB | | | | | | | |
| TCK | | | | | | | DB.TCK/ SWCLK | | | | | | | | | |
| TMS | | | | | DB.TMS/ SWDIO | | | | | | | | | | | |
| $\overline{\text{PORST}}$ | | | | | | | | | | | | | | | | |
| XTAL1 | | | | | | | | | U0C0. DX0F | U0C1. DX0F | U1C0. DX0F | U1C1. DX0F | U2C0. DX0F | U2C1. DX0F | | |
| XTAL2 | | | | | | | | | | | | | | | | |
| RTC_XTAL1 | | | | | | | | | | | ERU0. 1B1 | | | | | |
| RTC_XTAL2 | | | | | | | | | | | | | | | | |

## 2.3 Power Connection Scheme

**Figure 9**. shows a reference power connection scheme for the XMC4500.

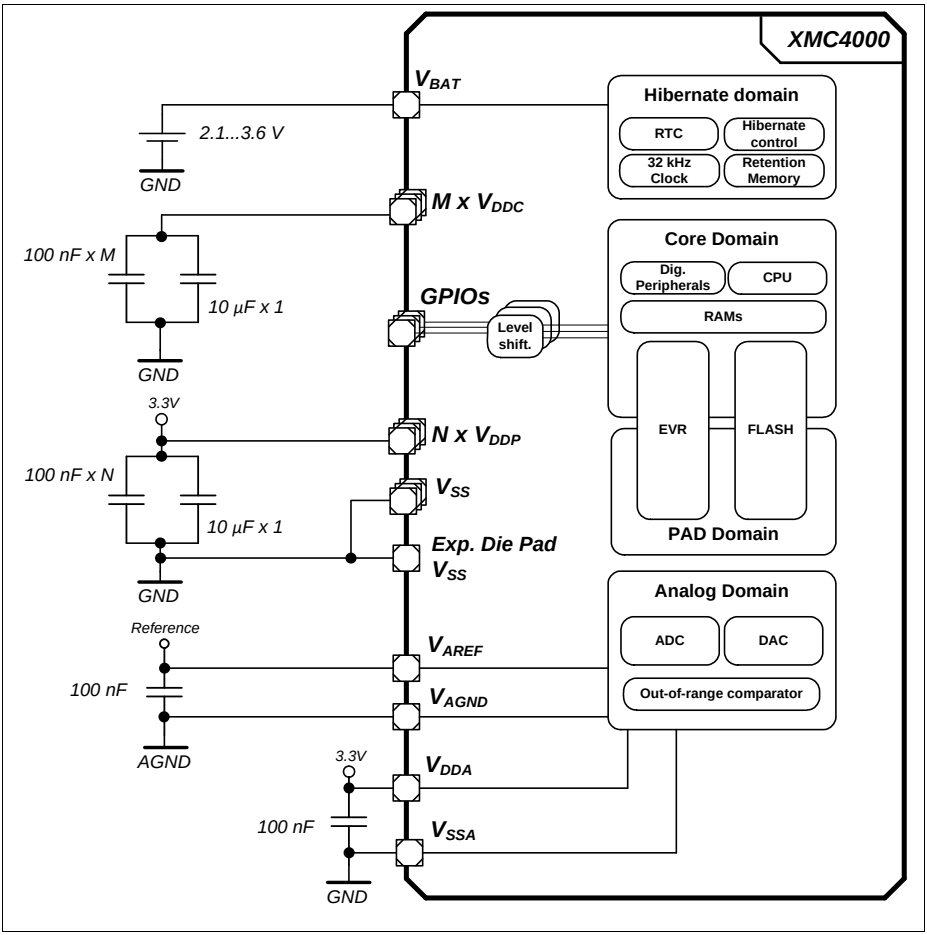


**Figure 9 Power Connection Scheme**

Every power supply pin needs to be connected. Different pins of the same supply need also to be externally connected. As example, all $V_{DDP}$ pins must be connected externally to one $V_{DDP}$ net. In this reference scheme one 100 nF capacitor is connected at each supply pin against $V_{SS}$. An additional 10 µF capacitor is connected to the $V_{DDP}$ nets and an additional 10 uF capacitor to the $V_{DDC}$ nets.

**Table 13 Overload Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input current on any port pin during overload condition | $I_{OV}$ SR | -5 | – | 5 | mA | |
| Absolute sum of all input circuit currents for one port group during overload condition[1)] | $I_{OVG}$ SR | – | – | 20 | mA | $\Sigma\|I_{OVx}\|$, for all $I_{OVx} < 0$ mA |
| | | – | – | 20 | mA | $\Sigma\|I_{OVx}\|$, for all $I_{OVx} > 0$ mA |
| Absolute sum of all input circuit currents during overload condition | $I_{OVS}$ SR | – | – | 80 | mA | $\Sigma I_{OVG}$ |

1) The port groups are defined in **Table 16**.

**Figure 11** shows the path of the input currents during overload via the ESD protection structures. The diodes against $V_{DDP}$ and ground are a simplified representation of these ESD protection structures.

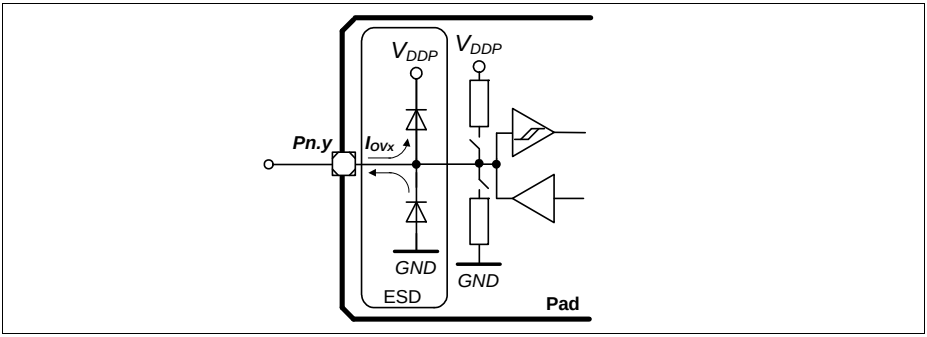


**Figure 11 Input Overload Current via ESD structures**

**Table 14** and **Table 15** list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the **Absolute Maximum Ratings** must not be exceeded during overload.

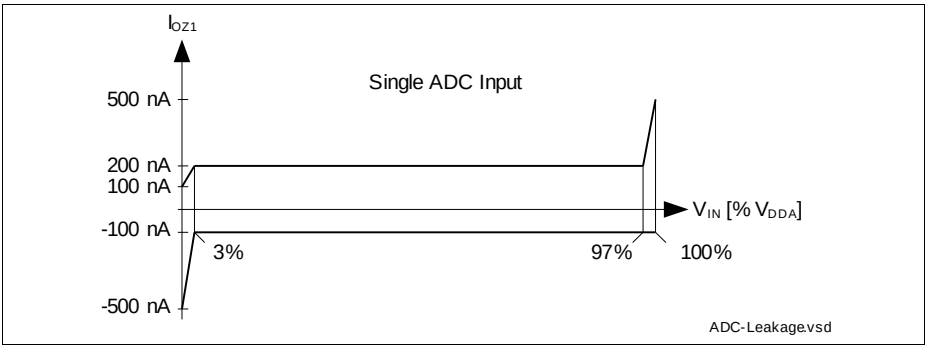


**Figure 16 VADC Analog Input Leakage Current**

### Conversion Time

**Table 24 Conversion Time** (Operating Conditions apply)

| Parameter | Symbol | Values | Unit | Note |
|---|---|---|---|---|
| Conversion time | $t_C$ CC | $2 \times T_{ADC}$ + $(2 + N + STC + PC + DM) \times T_{ADCI}$ | µs | N = 8, 10, 12 for N-bit conversion<br>$T_{ADC} = 1 / f_{PERIPH}$<br>$T_{ADCI} = 1 / f_{ADCI}$ |

- STC defines additional clock cycles to extend the sample time
- PC adds two cycles if post-calibration is enabled
- DM adds one cycle for an extended conversion time of the MSB

### Conversion Time Examples

System assumptions:
$f_{ADC}$ = 120 MHz i.e. $t_{ADC}$ = 8.33 ns, DIVA = 3, $f_{ADCI}$ = 30 MHz i.e. $t_{ADCI}$ = 33.3 ns
According to the given formulas the following minimum conversion times can be achieved (STC = 0, DM = 0):

12-bit post-calibrated conversion (PC = 2):
$t_{CN12C} = (2 + 12 + 2) \times t_{ADCI} + 2 \times t_{ADC} = 16 \times 33.3$ ns $+ 2 \times 8.33$ ns = 550 ns
12-bit uncalibrated conversion:
$t_{CN12} = (2 + 12) \times t_{ADCI} + 2 \times t_{ADC} = 14 \times 33.3$ ns $+ 2 \times 8.33$ ns = 483 ns
10-bit uncalibrated conversion:
$t_{CN10} = (2 + 10) \times t_{ADCI} + 2 \times t_{ADC} = 12 \times 33.3$ ns $+ 2 \times 8.33$ ns = 417 ns
8-bit uncalibrated:
$t_{CN8} = (2 + 8) \times t_{ADCI} + 2 \times t_{ADC} = 10 \times 33.3$ ns $+ 2 \times 8.33$ ns = 350 ns

2) Maximum threshold for reset deassertion.
3) The $V_{DDP}$ monitoring has a typical hysteresis of $V_{PORHYS}$ = 180 mV.
4) If $t_{PR}$ is not met, low spikes on $\overline{PORST}$ may be seen during start up (e.g. reset pulses generated by the supply monitoring due to a slow ramping $V_{DDP}$).

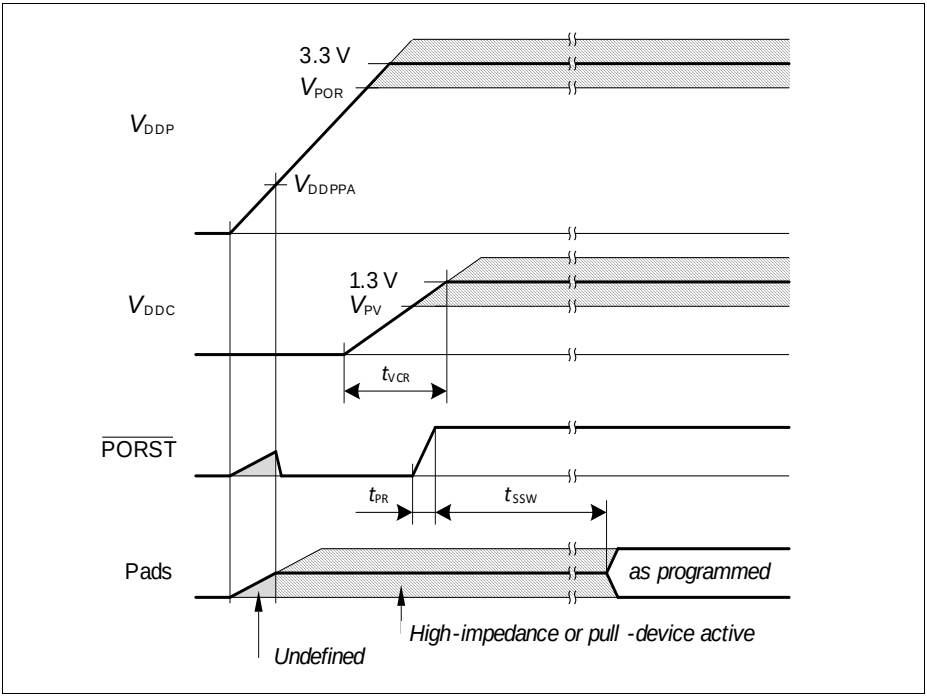


**Figure 26 Power-Up Behavior**

### 3.3.3 Power Sequencing

While starting up and shutting down as well as when switching power modes of the system it is important to limit the current load steps. A typical cause for such load steps is changing the CPU frequency $f_{CPU}$. Load steps exceeding the below defined values may cause a power on reset triggered by the supply monitor.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 35 Power Sequencing Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Positive Load Step Current | $\Delta I_{PLS}$ SR | - | – | 50 | mA | Load increase on $V_{DDP}$ $\Delta t \leq 10$ ns |
| Negative Load Step Current | $\Delta I_{NLS}$ SR | - | – | 150 | mA | Load decrease on $V_{DDP}$ $\Delta t \leq 10$ ns |
| $V_{DDC}$ Voltage Over- / Undershoot from Load Step | $\Delta V_{LS}$ CC | - | – | ±100 | mV | For maximum positive or negative load step |
| Positive Load Step Settling Time | $t_{PLSS}$ SR | 50 | – | - | µs | |
| Negative Load Step Settling Time | $t_{NLSS}$ SR | 100 | – | - | µs | |
| External Buffer Capacitor on $V_{DDC}$ | $C_{EXT}$ SR | - | 10 | - | µF | In addition $C$ = 100 nF capacitor on each $V_{DDC}$ pin |

**Positive Load Step Examples**

System assumptions:
$f_{CPU} = f_{SYS}$, target frequency $f_{CPU}$ = 120 MHz, main PLL $f_{VCO}$ = 480 MHz, stepping done by K2 divider, $t_{PLSS}$ between individual steps:

24 MHz - 48 MHz - 68 MHz - 96 MHz - 120 MHz (K2 steps 20 - 10 - 7 - 5 - 4)
24 MHz - 68 MHz - 96 MHz - 120 MHz (K2 steps 20 - 7 - 5 - 4)
24 MHz - 68 MHz - 120 MHz (K2 steps 20 - 7 - 4)

### Slow Internal Clock Source

**Table 38 Slow Internal Clock Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Nominal frequency | $f_{OSI}$ CC | – | 32.768 | – | kHz | |
| Accuracy | $\Delta f_{OSI}$ CC | -4 | – | 4 | % | $V_{BAT}$ = const. 0 °C ≤ $T_A$ ≤ 85 °C |
| | | -5 | – | 5 | % | $V_{BAT}$ = const. $T_A$ < 0 °C or $T_A$ > 85 °C |
| | | -5 | – | 5 | % | 2.4 V ≤ $V_{BAT}$, $T_A$ = 25 °C |
| | | -10 | – | 10 | % | 1.95 V ≤ $V_{BAT}$ < 2.4 V, $T_A$ = 25 °C |
| Start-up time | $t_{OSIS}$ CC | – | 50 | – | µs | |

### 3.3.8 Embedded Trace Macro Cell (ETM) Timing

The data timing refers to the active clock edge. The XMC4500 ETM uses the half-rate clocking mode. In this mode both, the rising and falling clock edges are active clock edges.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

*Note: Operating conditions apply, with $C_L \leq 15$ pF.*

**Table 41 ETM Interface Timing Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| TRACECLK period | $t_1$ | CC | 16.7 | – | – | ns | – |
| TRACECLK high time | $t_2$ | CC | 2 | – | – | ns | – |
| TRACECLK low time | $t_3$ | CC | 2 | – | – | ns | – |
| TRACECLK and TRACEDATA rise time | $t_4$ | CC | – | – | 3 | ns | – |
| TRACECLK and TRACEDATA fall time | $t_5$ | CC | – | – | 3 | ns | – |
| TRACEDATA output valid time | $t_6$ | CC | -2 | – | 3 | ns | – |

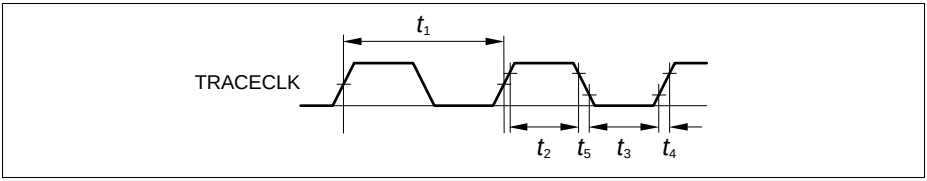


**Figure 30 ETM Clock Timing**

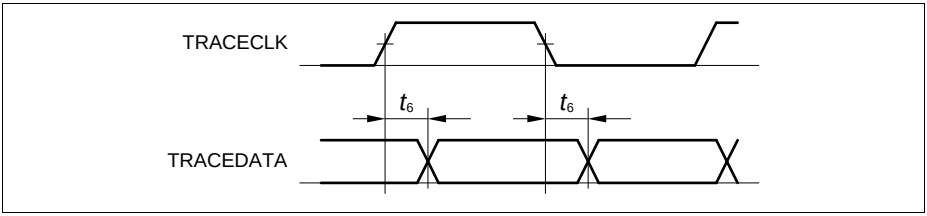


**Figure 31 ETM Data Timing**

## 3.3.9 Peripheral Timing

### 3.3.9.1 Delta-Sigma Demodulator Digital Interface Timing

The following parameters are applicable for the digital interface of the Delta-Sigma Demodulator (DSD).
The data timing is relative to the active clock edge. Depending on the operation mode of the connected modulator that can be the rising and falling clock edge.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 42 DSD Interface Timing Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| MCLK period in master mode | $t_1$ | CC | 33.3 | – | – | ns | $t_1 \geq 4 \times t_{PERIPH}$ [1] |
| MCLK high time in master mode | $t_2$ | CC | 9 | – | – | ns | $t_2 > t_{PERIPH}$ [1] |
| MCLK low time in master mode | $t_3$ | CC | 9 | – | – | ns | $t_3 > t_{PERIPH}$ [1] |
| MCLK period in slave mode | $t_1$ | SR | 33.3 | – | – | ns | $t_1 \geq 4 \times t_{PERIPH}$ [1] |
| MCLK high time in slave mode | $t_2$ | SR | $t_{PERIPH}$ | – | – | ns | [1] |
| MCLK low time in slave mode | $t_3$ | SR | $t_{PERIPH}$ | – | – | ns | [1] |
| DIN input setup time to the active clock edge | $t_4$ | SR | $t_{PERIPH}$ + 4 | – | – | ns | [1] |
| DIN input hold time from the active clock edge | $t_5$ | SR | $t_{PERIPH}$ + 3 | – | – | ns | [1] |

1) $t_{PERIPH} = 1 / f_{PERIPH}$

### Full-Speed Input Path (Read)

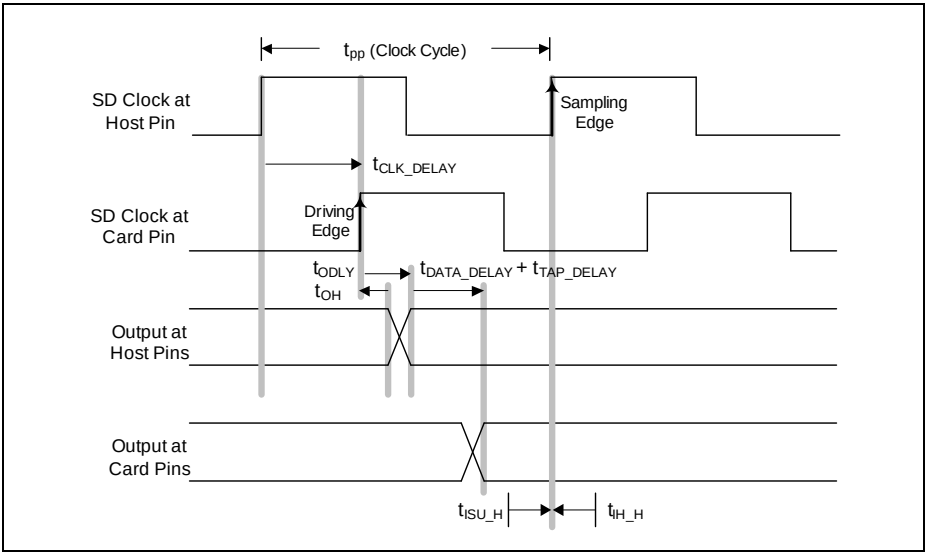


**Figure 38 Full-Speed Input Path**

### Full-Speed Read Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

(5)

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ODLY} + t_{ISU\_F} < 0{,}5 \times t_{pp}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < 0{,}5 \times t_{pp} - t_{ODLY} - t_{ISU\_F} - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < 20 - 14 - 2 - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < 4 - t_{TAP\_DELAY}$$

The data + clock delay can be up to 4 ns for a 40 ns clock cycle.

**High-Speed Read Meeting Hold (Minimum Delay)**

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

(12)

$$t_{CLK\_DELAY} + t_{OH} + t_{DATA\_DELAY} + t_{TAP\_DELAY} > t_{IH\_H}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} > t_{IH\_H} - t_{OH} - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} > 2 - 2{,}5 - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} > -0{,}5 - t_{TAP\_DELAY}$$

The data + clock delay must be greater than -0.5 ns for a 20 ns clock cycle. This is always fulfilled.

### 3.3.10 EBU Timing

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

*Note: Operating Conditions apply, with Class A2 pins and $C_L$ = 16 pF.*

#### 3.3.10.1 EBU Asynchronous Timing

*Note: For each timing, the accumulated PLL jitter must be added separately.*

**Table 53 Common Timing Parameters for all Asynchronous Timings**

| Parameter | | | Symbol | Limit Values | | Unit | Edge Setting |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | | |
| Pulse width deviation from the ideal programmed width due to the A2 pad asymmetry, strong driver mode, rise delay - fall delay. $C_L$ = 16 pF. | | CC | $t_a$ | -1 | 1.5 | ns | sharp |
| | | | | -2 | 1 | | medium |
| AD(24:16) output delay | to $\overline{ADV}$ rising edge, multiplexed read / write | CC | $t_{13}$ | -5.5 | 2 | | – |
| AD(24:16) output delay | | CC | $t_{14}$ | -5.5 | 2 | | – |

## Read Timing

**Table 54 Asynchronous Read Timing, Multiplexed and Demultiplexed**

| Parameter | | | Symbol | Limit Values | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min. | Max. | |
| A(24:16) output delay | to $\overline{RD}$ rising edge, deviation from the ideal programmed value. | CC | $t_0$ | -2.5 | 2.5 | ns |
| A(24:16) output delay | | CC | $t_1$ | -2.5 | 2.5 | |
| $\overline{CS}$ rising edge | | CC | $t_2$ | -2 | 2.5 | |
| $\overline{ADV}$ rising edge | | CC | $t_3$ | -1.5 | 4.5 | |
| $\overline{BC}$ rising edge | | CC | $t_4$ | -2.5 | 2.5 | |
| $\overline{WAIT}$ input setup | | SR | $t_5$ | 12 | – | |
| $\overline{WAIT}$ input hold | | SR | $t_6$ | 0 | – | |
| Data input setup | | SR | $t_7$ | 12 | – | |
| Data input hold | | SR | $t_8$ | 0 | – | |
| RD / $\overline{WR}$ output delay | | CC | $t_9$ | -2.5 | 1.5 | |

Multiplexed Write Timing

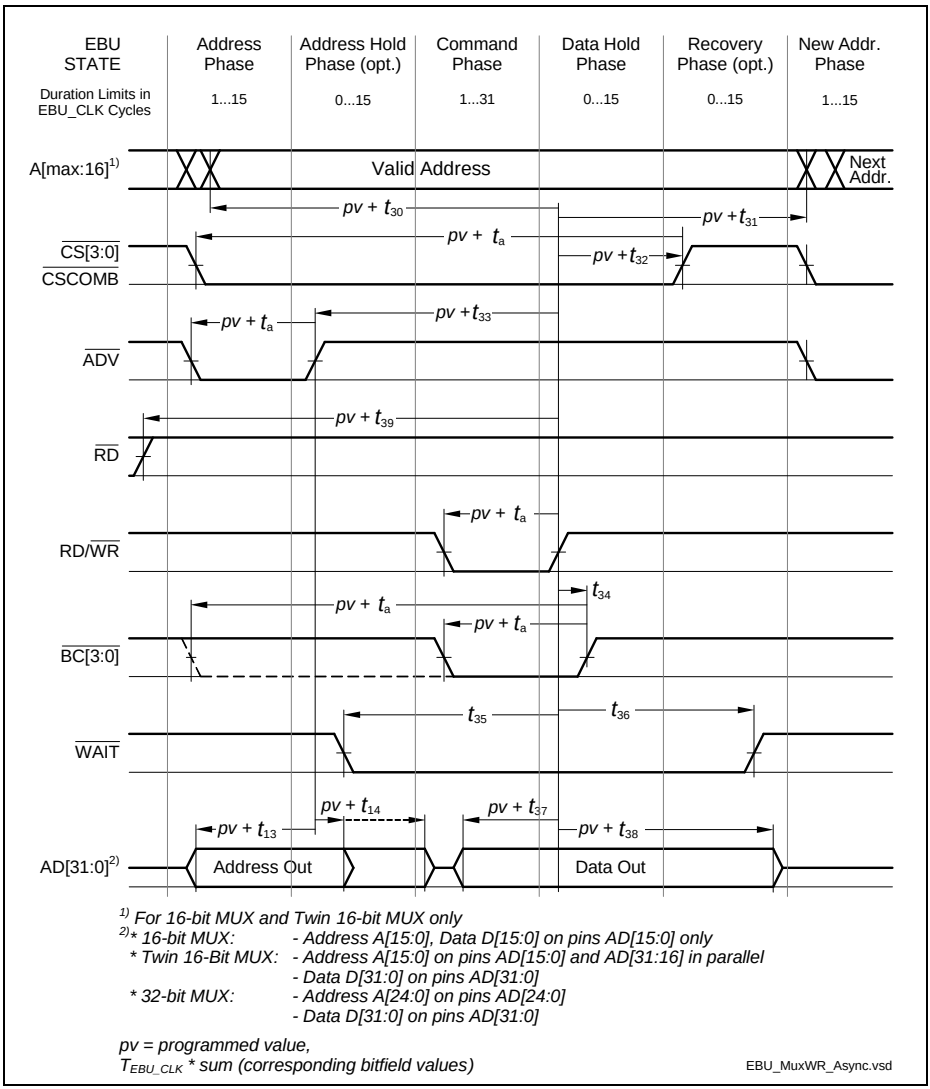


**Figure 43 Multiplexed Write Access**

### 3.3.10.3 EBU Arbitration Signal Timing

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

*Note: Operating Conditions apply.*

**Table 57 EBU Arbitration Signal Timing Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Output delay from BFCLKO rising edge | $t_1$ | CC | – | – | 16 | ns | $C_L$ = 50 pF |
| Data setup to BFCLKO falling edge | $t_2$ | SR | 11 | – | – | ns | – |
| Data hold from BFCLKO falling edge | $t_3$ | SR | 2 | – | – | ns | – |

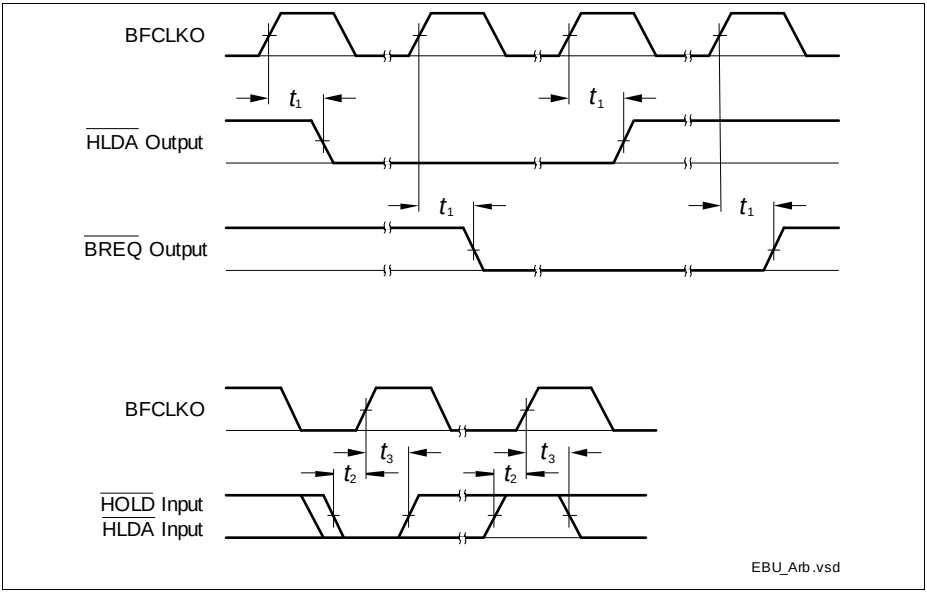


**Figure 46 EBU Arbitration Signal Timing**

**Table 59 EBU SDRAM Access Signal Timing Parameters**

| Parameter | | | Symbol | Limit Values | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min. | Max. | |
| A(15:0) output valid | from SDCLKO low-to-high transition | CC | $t_6$ | – | 9 | ns |
| A(15:0) output hold | | CC | $t_7$ | 3 | – | |
| $\overline{CS}$(3:0) low | | CC | $t_8$ | – | 9 | |
| $\overline{CS}$(3:0) high | | CC | $t_9$ | 3 | – | |
| $\overline{RAS}$ low | | CC | $t_{10}$ | – | 9 | |
| $\overline{RAS}$ high | | SR | $t_{11}$ | 3 | – | |
| $\overline{CAS}$ low | | SR | $t_{12}$ | – | 9 | |
| $\overline{CAS}$ high | | CC | $t_{13}$ | 3 | – | |
| RD/$\overline{WR}$ low | | CC | $t_{14}$ | – | 9 | |
| RD/$\overline{WR}$ high | | CC | $t_{15}$ | 3 | – | |
| $\overline{BC}$(3:0) low | | CC | $t_{16}$ | – | 9 | |
| $\overline{BC}$(3:0) high | | CC | $t_{17}$ | 3 | – | |
| D(15:0) output valid | | CC | $t_{18}$ | – | 9 | |
| D(15:0) output hold | | CC | $t_{19}$ | 3 | – | |
| CKE output valid[1)] | | CC | $t_{22}$ | – | 7 | |
| CKE output hold[1)] | | CC | $t_{23}$ | 2 | – | |
| D(15:0) input hold | | SR | $t_{21}$ | 3 | – | |
| D(15:0) input setup to SDCLKO low-to-high transition | | SR | $t_{20}$ | 4 | – | |

1) Not depicted in the read and write access timing figures below.

### 3.3.12.3 ETH MII Parameters

In the following, the parameters of the MII (Media Independent Interface) are described.

**Table 62 ETH MII Signal Timing Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Clock period, 10 Mbps | $t_7$ | SR | 400 | – | – | ns | $C_L$ = 25 pF |
| Clock high time, 10 Mbps | $t_8$ | SR | 140 | – | 260 | ns | |
| Clock low time, 10 Mbps | $t_9$ | SR | 140 | – | 260 | ns | |
| Clock period, 100 Mbps | $t_7$ | SR | 40 | – | – | ns | |
| Clock high time, 100 Mbps | $t_8$ | SR | 14 | – | 26 | ns | |
| Clock low time, 100 Mbps | $t_9$ | SR | 14 | – | 26 | ns | |
| Input setup time | $t_{10}$ | SR | 10 | – | – | ns | |
| Input hold time | $t_{11}$ | SR | 10 | – | – | ns | |
| Output valid time | $t_{12}$ | CC | 0 | – | 25 | ns | |

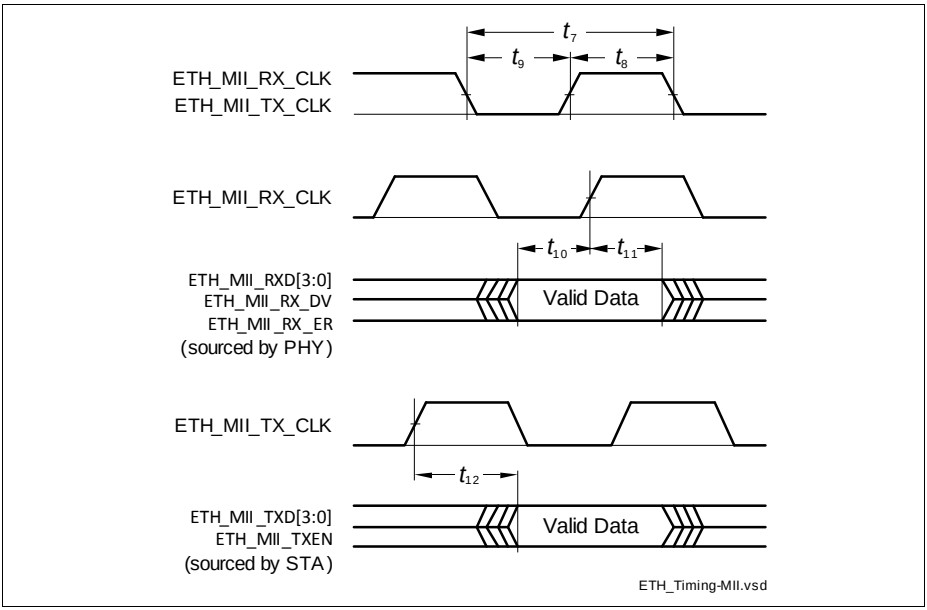


**Figure 53 ETH MII Signal Timing**

## 4.3 Quality Declarations

The qualification of the XMC4500 is executed according to the JEDEC standard JESD47H.

*Note: For automotive applications refer to the Infineon automotive microcontrollers.*

**Table 67 Quality Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Operation lifetime | $t_{OP}$ CC | 20 | – | – | a | $T_J \leq 109°C$, device permanent on |
| ESD susceptibility according to Human Body Model (HBM) | $V_{HBM}$ SR | – | – | 2 000 | V | EIA/JESD22-A114-B |
| ESD susceptibility according to Charged Device Model (CDM) | $V_{CDM}$ SR | – | – | 500 | V | Conforming to JESD22-C101-C |
| Moisture sensitivity level | $MSL$ CC | – | – | 3 | – | JEDEC J-STD-020D |
| Soldering temperature | $T_{SDR}$ SR | – | – | 260 | °C | Profile according to JEDEC J-STD-020D |