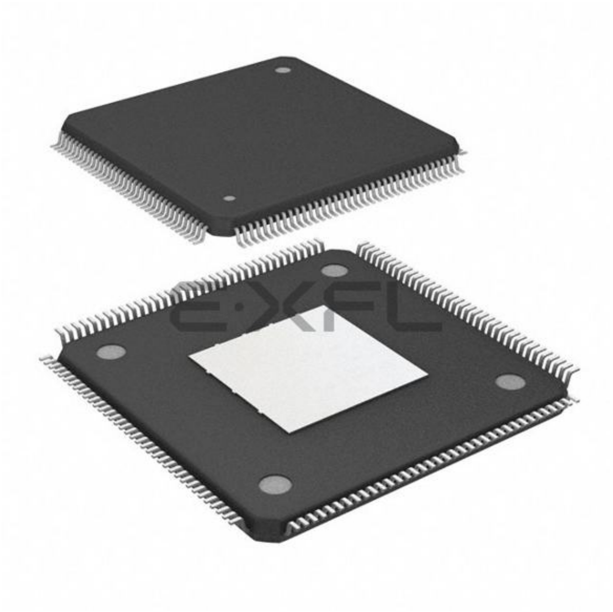
Infineon Technologies - XMC4500F144K768ACXQMA1 Datasheet



Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, SPI, UART, USB
Peripherals	DMA, I²S, LED, POR, PWM, WDT
Number of I/O	91
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-13
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4500f144k768acxqma1

1.2 Device Types

These device types are available and can be ordered through Infineon’s direct and/or distribution channels.

Table 1 Synopsis of XMC4500 Device Types

Derivative[1]	Package	Flash Kbytes	SRAM Kbytes
XMC4500-E144x1024	PG-LFBGA-144	1024	160
XMC4500-F144x1024	PG-LQFP-144	1024	160
XMC4500-F100x1024	PG-LQFP-100	1024	160
XMC4500-F144x768	PG-LQFP-144	768	160
XMC4500-F100x768	PG-LQFP-100	768	160
XMC4502-F100x768	PG-LQFP-100	768	160
XMC4504-F144x512	PG-LQFP-144	512	128
XMC4504-F100x512	PG-LQFP-100	512	128

1) x is a placeholder for the supported temperature range.

1.3 Device Type Features

The following table lists the available features per device type.

Table 2 Features of XMC4500 Device Types

Derivative[1]	LEDTS Intf.	SDMMC Intf.	EBU Intf.[2]	ETH Intf.[3]	USB Intf.	USIC Chan.	MultiCAN Nodes, MO
XMC4500-E144x1024	1	1	SDM	MR	1	3 x 2	N0, N1, N2 MO[0..63]
XMC4500-F144x1024	1	1	SDM	MR	1	3 x 2	N0, N1, N2 MO[0..63]
XMC4500-F100x1024	1	1	M16	R	1	3 x 2	N0, N1, N2 MO[0..63]
XMC4500-F144x768	1	1	SDM	MR	1	3 x 2	N0, N1, N2 MO[0..63]
XMC4500-F100x768	1	1	M16	R	1	3 x 2	N0, N1, N2 MO[0..63]
XMC4502-F100x768	1	1	M16	-	1	3 x 2	N0, N1, N2 MO[0..63]

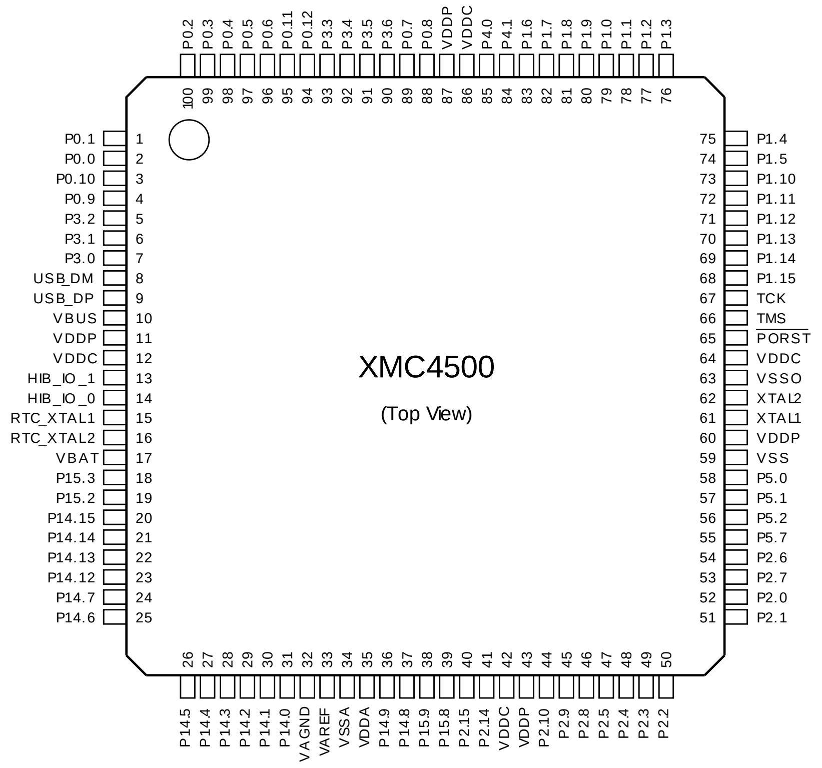


Figure 7 XMC4500 PG-LQFP-100 Pin Configuration (top view)

2.2.1 Package Pin Summary

The following general scheme is used to describe each pin:

Table 8 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type	Notes
Name	N	Ax	...	A2	

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the dedicated pins (i.e. $\overline{\text{PORST}}$) and supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type (A1, A1+, A2, special=special pad, In=input pad, AN/DIG_IN=analog and digital input, Power=power supply). Details about the pad properties are defined in the Electrical Parameters.

In the “Notes”, special information to the respective pin/function is given, i.e. deviations from the default configuration after reset. Per default the regular Port pins are configured as direct input with no internal pull device active.

Table 9 Package Pin Mapping

Function	LQFP-144	LFBGA-144	LQFP-100	Pad Type	Notes
P0.0	2	C4	2	A1+	
P0.1	1	C3	1	A1+	
P0.2	144	A3	100	A2	
P0.3	143	A4	99	A2	
P0.4	142	B5	98	A2	
P0.5	141	A5	97	A2	
P0.6	140	A6	96	A2	
P0.7	128	B7	89	A2	After a system reset, via HWSEL this pin selects the DB.TDI function.
P0.8	127	A8	88	A2	After a system reset, via HWSEL this pin selects the $\overline{\text{DB.TRST}}$ function, with a weak pull-down active.
P0.9	4	D4	4	A2	
P0.10	3	B4	3	A1+	

Table 9 Package Pin Mapping (cont'd)

Function	LQFP-144	LFBGA-144	LQFP-100	Pad Type	Notes
P0.11	139	E5	95	A1+	
P0.12	138	D5	94	A1+	
P0.13	137	C5	-	A1+	
P0.14	136	E6	-	A1+	
P0.15	135	C6	-	A1+	
P1.0	112	D9	79	A1+	
P1.1	111	E9	78	A1+	
P1.2	110	C11	77	A2	
P1.3	109	C12	76	A2	
P1.4	108	C10	75	A1+	
P1.5	107	D10	74	A1+	
P1.6	116	B9	83	A2	
P1.7	115	B10	82	A2	
P1.8	114	A10	81	A2	
P1.9	113	B11	80	A2	
P1.10	106	D12	73	A1+	
P1.11	105	D11	72	A1+	
P1.12	104	E11	71	A2	
P1.13	103	E12	70	A2	
P1.14	102	E10	69	A2	
P1.15	94	G12	68	A2	
P2.0	74	J11	52	A2	
P2.1	73	K12	51	A2	After a system reset, via HWSEL this pin selects the DB.TDO function.
P2.2	72	K11	50	A2	
P2.3	71	L11	49	A2	
P2.4	70	L10	48	A2	
P2.5	69	M10	47	A2	
P2.6	76	J9	54	A1+	
P2.7	75	K9	53	A1+	
P2.8	68	L9	46	A2	
P2.9	67	M9	45	A2	

Table 9 Package Pin Mapping (cont'd)

Function	**LQFP-144**	**LFBGA-144**	**LQFP-100**	**Pad Type**	**Notes**
P15.3	29	G2	18	AN/DIG_IN	
P15.4	28	G4	-	AN/DIG_IN	
P15.5	27	G3	-	AN/DIG_IN	
P15.6	26	G5	-	AN/DIG_IN	
P15.7	25	G6	-	AN/DIG_IN	
P15.8	54	M6	39	AN/DIG_IN	
P15.9	53	L6	38	AN/DIG_IN	
P15.12	50	K5	-	AN/DIG_IN	
P15.13	49	M4	-	AN/DIG_IN	
P15.14	44	L4	-	AN/DIG_IN	
P15.15	43	K4	-	AN/DIG_IN	
USB_DP	16	E1	9	special	
USB_DM	15	D1	8	special	
HIB_IO_0	21	F4	14	A1 special	At the first power-up and with every reset of the hibernate domain this pin is configured as open-drain output and drives "0". As output the medium driver mode is active.
HIB_IO_1	20	F3	13	A1 special	At the first power-up and with every reset of the hibernate domain this pin is configured as input with no pull device active. As output the medium driver mode is active.
TCK	93	G8	67	A1	Weak pull-down active.
TMS	92	G7	66	A1+	Weak pull-up active. As output the strong-soft driver mode is active.
$\overline{\text{PORST}}$	91	G11	65	special	Weak pull-up permanently active, strong pull-down controlled by EVR.
XTAL1	87	H11	61	clock_IN	
XTAL2	88	H12	62	clock_O	

2.2.2.1 Port I/O Function Table

Table 11 Port I/O Functions

Function	Outputs						Inputs									
	ALT1	**ALT2**	**ALT3**	**ALT4**	**HWO0**	**HWO1**	**HWI0**	**HWI1**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**
P0.0		CAN.N0_TXD	CCU80.OUT21	LEDTS0.COL2					U1C1.DX0D	ETH0.CLK_RMIIB	ERU0.0B0					ETH0.CLKRXB
P0.1	USB.DRIVEVBUS	U1C1.DOUT0	CCU80.OUT11	LEDTS0.COL3						ETH0.CRS_DVB	ERU0.0A0					ETH0.RXDVB
P0.2		U1C1.SELO1	CCU80.OUT01		U1C0.DOUT3	EBU.AD0	U1C0.HWIN3	EBU.D0	ETH0.RXD0B		ERU0.3B3					
P0.3			CCU80.OUT20		U1C0.DOUT2	EBU.AD1	U1C0.HWIN2	EBU.D1	ETH0.RXD1B			ERU1.3B0				
P0.4	ETH0.TX_EN		CCU80.OUT10		U1C0.DOUT1	EBU.AD2	U1C0.HWIN1	EBU.D2		U1C0.DX0A	ERU0.2B3					
P0.5	ETH0.TXD0	U1C0.DOUT0	CCU80.OUT00		U1C0.DOUT0	EBU.AD3	U1C0.HWIN0	EBU.D3		U1C0.DX0B		ERU1.3A0				
P0.6	ETH0.TXD1	U1C0.SELO0	CCU80.OUT30			EBU.ADV				U1C0.DX2A	ERU0.3B2		CCU80.IN2B			
P0.7	WWDT.SERVICE_OUT	U0C0.SELO0				EBU.AD6	DB.TDI	EBU.D6	U0C0.DX2B	DSD.DIN1A	ERU0.2B1		CCU80.IN0A	CCU80.IN1A	CCU80.IN2A	CCU80.IN3A
P0.8	SCU.EXTCLK	U0C0.SCLKOUT				EBU.AD7	DB.TRST	EBU.D7	U0C0.DX1B	DSD.DIN0A	ERU0.2A1		CCU80.IN1B			
P0.9		U1C1.SELO0	CCU80.OUT12	LEDTS0.COL0	ETH0.MDO	EBU.CS1	ETH0.MDIA		U1C1.DX2A	USB.ID	ERU0.1B0					
P0.10	ETH0.MDC	U1C1.SCLKOUT	CCU80.OUT02	LEDTS0.COL1					U1C1.DX1A		ERU0.1A0					
P0.11		U1C0.SCLKOUT	CCU80.OUT31		SDMMC.RST	EBU.BREQ			ETH0.RXERB	U1C0.DX1A	ERU0.3A2					
P0.12		U1C1.SELO0	CCU40.OUT3			EBU.HLDA		EBU.HLDA		U1C1.DX2B	ERU0.2B2					
P0.13		U1C1.SCLKOUT	CCU40.OUT2							U1C1.DX1B	ERU0.2A2					
P0.14		U1C0.SELO1	CCU40.OUT1		U1C1.DOUT3		U1C1.HWIN3						CCU42.IN3C			
P0.15		U1C0.SELO2	CCU40.OUT0		U1C1.DOUT2		U1C1.HWIN2						CCU42.IN2C			
P1.0	DSD.CGPWMN	U0C0.SELO0	CCU40.OUT3	ERU1.PDOUT3					U0C0.DX2A		ERU0.3B0		CCU40.IN3A			
P1.1	DSD.CGPWMP	U0C0.SCLKOUT	CCU40.OUT2	ERU1.PDOUT2			SDMMC.SDWC		U0C0.DX1A	POSIF0.IN2A	ERU0.3A0		CCU40.IN2A			
P1.2			CCU40.OUT1	ERU1.PDOUT1	U0C0.DOUT3	EBU.AD14	U0C0.HWIN3	EBU.D14		POSIF0.IN1A		ERU1.2B0	CCU40.IN1A			
P1.3		U0C0.MCLKOUT	CCU40.OUT0	ERU1.PDOUT0	U0C0.DOUT2	EBU.AD15	U0C0.HWIN2	EBU.D15		POSIF0.IN0A		ERU1.2A0	CCU40.IN0A			
P1.4	WWDT.SERVICE_OUT	CAN.N0_TXD	CCU80.OUT33	CCU81.OUT20	U0C0.DOUT1		U0C0.HWIN1		U0C0.DX0B	CAN.N1_RXDD	ERU0.2B0		CCU41.IN0C			

Table 11 Port I/O Functions (cont'd)

Function	Outputs						Inputs									
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P6.6			DSD.MCLK3		DB.ETM_TRACEDATA0	EBU.BC3			DSD.MCLK3A	ETH0.CLK_TXB						
P14.0									VADC.G0CH0							
P14.1									VADC.G0CH1							
P14.2									VADC.G0CH2	VADC.G1CH2						
P14.3									VADC.G0CH3	VADC.G1CH3			CAN.N0_RXDB			
P14.4									VADC.G0CH4		VADC.G2CH0					
P14.5									VADC.G0CH5		VADC.G2CH1		POSIF0.IN2B			
P14.6									VADC.G0CH6				POSIF0.IN1B		G0ORC6	
P14.7									VADC.G0CH7				POSIF0.IN0B		G0ORC7	
P14.8					DAC.OUT_0					VADC.G1CH0		VADC.G3CH2	ETH0.RXD0C			
P14.9					DAC.OUT_1					VADC.G1CH1		VADC.G3CH3	ETH0.RXD1C			
P14.12										VADC.G1CH4						
P14.13										VADC.G1CH5						
P14.14										VADC.G1CH6					G1ORC6	
P14.15										VADC.G1CH7					G1ORC7	
P15.2											VADC.G2CH2					
P15.3											VADC.G2CH3					
P15.4											VADC.G2CH4					
P15.5											VADC.G2CH5					
P15.6											VADC.G2CH6					
P15.7											VADC.G2CH7					
P15.8												VADC.G3CH0	ETH0.CLK_RMIIC			ETH0.CLKRXC
P15.9												VADC.G3CH1	ETH0.CRS_DVC			ETH0.RXDVC

Table 11 Port I/O Functions (cont'd)

Function	Outputs						Inputs									
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P15.12												VADC.G3CH4				
P15.13												VADC.G3CH5				
P15.14												VADC.G3CH6				
P15.15												VADC.G3CH7				
USB_DP																
USB_DM																
HIB_IO_0	HIBOUT	WWDT.SERVICE_OUT							WAKEUPA							
HIB_IO_1	HIBOUT	WWDT.SERVICE_OUT							WAKEUPB							
TCK							DB.TCK/SWCLK									
TMS					DB.TMS/SWDIO											
$\overline{\text{PORST}}$																
XTAL1									U0C0.DX0F	U0C1.DX0F	U1C0.DX0F	U1C1.DX0F	U2C0.DX0F	U2C1.DX0F		
XTAL2																
RTC_XTAL1											ERU0.1B1					
RTC_XTAL2																

3.2 DC Parameters

3.2.1 Input/Output Pins

The digital input stage of the shared analog/digital input pins is identical to the input stage of the standard digital input/output pins.
The Pull-up on the $\overline{\text{PORST}}$ pin is identical to the Pull-up on the standard digital input/output pins.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 19 Standard Pad Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Pin capacitance (digital inputs/outputs)	C_{IO} CC	–		10	pF	
Pull-down current	$\lvert I_{\text{PDL}} \rvert$ CC	150		–	µA	1) $V_{\text{IN}} \geq 0.6 \times V_{\text{DDP}}$
		–		10	µA	2) $V_{\text{IN}} \leq 0.36 \times V_{\text{DDP}}$
Pull-Up current	$\lvert I_{\text{PUH}} \rvert$ CC	–		10	µA	2) $V_{\text{IN}} \geq 0.6 \times V_{\text{DDP}}$
		100		–	µA	1) $V_{\text{IN}} \leq 0.36 \times V_{\text{DDP}}$
Input Hysteresis for pads of all A classes3)	$HYSA$ CC	0.1 × V_{DDP}		–	V	
$\overline{\text{PORST}}$ spike filter always blocked pulse duration	t_{SF1} CC	–		10	ns	
$\overline{\text{PORST}}$ spike filter pass-through pulse duration	t_{SF2} CC	100		–	ns	
$\overline{\text{PORST}}$ pull-down current	$\lvert I_{\text{PPD}} \rvert$ CC	13		–	mA	$V_{\text{IN}} = 1.0$ V

1) Current required to override the pull device with the opposite logic level ("force current").
With active pull device, at load currents between force and keep current the input state is undefined.

2) Load current at which the pull device still maintains the valid logic level ("keep current").
With active pull device, at load currents between force and keep current the input state is undefined.

3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

3.2.2 Analog to Digital Converters (VADC)

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 23 VADC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Analog reference voltage[5]	V_{AREF} SR	V_{AGND} + 1	–	V_{DDA} + 0.05[1]	V	
Analog reference ground[5]	V_{AGND} SR	V_{SSM} - 0.05	–	V_{AREF} - 1	V	
Analog reference voltage range[2][5]	V_{AREF} - V_{AGND} SR	1	–	V_{DDA} + 0.1	V	
Analog input voltage	V_{AIN} SR	V_{AGND}	–	V_{DDA}	V	
Input leakage at analog inputs[3]	I_{OZ1} CC	-100	–	200	nA	$0.03 \times V_{DDA} < V_{AIN} < 0.97 \times V_{DDA}$
		-500	–	100	nA	$0 \text{ V} \leq V_{AIN} \leq 0.03 \times V_{DDA}$
		-100	–	500	nA	$0.97 \times V_{DDA} \leq V_{AIN} \leq V_{DDA}$
Input leakage current at VAREF	I_{OZ2} CC	-1	–	1	µA	$0 \text{ V} \leq V_{AREF} \leq V_{DDA}$
Input leakage current at VAGND	I_{OZ3} CC	-1	–	1	µA	$0 \text{ V} \leq V_{AGND} \leq V_{DDA}$
Internal ADC clock	f_{ADCI} CC	2	–	30	MHz	$V_{DDA} = 3.3 \text{ V}$
Switched capacitance at the analog voltage inputs[4]	C_{AINSW} CC	–	7	20	pF	
Total capacitance of an analog input	C_{AINTOT} CC	–	25	30	pF	
Switched capacitance at the positive reference voltage input[5][6]	C_{AREFSW} CC	–	15	30	pF	
Total capacitance of the voltage reference inputs[5]	$C_{AREFTOT}$ CC	–	20	40	pF	

3.2.4 Out-of-Range Comparator (ORC)

The Out-of-Range Comparator (ORC) triggers on analog input voltages (V_{AIN}) above the analog reference[1] (V_{AREF}) on selected input pins (GxORCy) and generates a service request trigger (GxORCOUTy).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

The parameters in **Table 26** apply for the maximum reference voltage $V_{\mathrm{AREF}} = V_{\mathrm{DDA}}$ + 50 mV.

Table 26 ORC Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DC Switching Level	V_{ODC}	CC	100	125	200	mV	$V_{\mathrm{AIN}} \geq V_{\mathrm{AREF}} + V_{\mathrm{ODC}}$
Hysteresis	V_{OHYS}	CC	50	–	V_{ODC}	mV	
Detection Delay of a persistent Overvoltage	t_{ODD}	CC	55	–	450	ns	$V_{\mathrm{AIN}} \geq V_{\mathrm{AREF}}$ + 200 mV
			45	–	105	ns	$V_{\mathrm{AIN}} \geq V_{\mathrm{AREF}}$ + 400 mV
Always detected Overvoltage Pulse	t_{OPDD}	CC	440	–	–	ns	$V_{\mathrm{AIN}} \geq V_{\mathrm{AREF}}$ + 200 mV
			90	–	–	ns	$V_{\mathrm{AIN}} \geq V_{\mathrm{AREF}}$ + 400 mV
Never detected Overvoltage Pulse	t_{OPDN}	CC	–	–	49	ns	$V_{\mathrm{AIN}} \geq V_{\mathrm{AREF}}$ + 200 mV
			–	–	30	ns	$V_{\mathrm{AIN}} \geq V_{\mathrm{AREF}}$ + 400 mV
Release Delay	t_{ORD}	CC	65	–	105	ns	$V_{\mathrm{AIN}} \leq V_{\mathrm{AREF}}$
Enable Delay	t_{OED}	CC	–	100	200	ns	

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[1] Always the standard VADC reference, alternate references do not apply to the ORC.

Table 35 Power Sequencing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Positive Load Step Current	ΔI_{PLS} SR	-	–	50	mA	Load increase on V_{DDP} $\Delta t \leq$ 10 ns
Negative Load Step Current	ΔI_{NLS} SR	-	–	150	mA	Load decrease on V_{DDP} $\Delta t \leq$ 10 ns
V_{DDC} Voltage Over- / Undershoot from Load Step	ΔV_{LS} CC	-	–	±100	mV	For maximum positive or negative load step
Positive Load Step Settling Time	t_{PLSS} SR	50	–	-	µs	
Negative Load Step Settling Time	t_{NLSS} SR	100	–	-	µs	
External Buffer Capacitor on V_{DDC}	C_{EXT} SR	-	10	-	µF	In addition C = 100 nF capacitor on each V_{DDC} pin

Positive Load Step Examples

System assumptions:
$f_{CPU} = f_{SYS}$, target frequency f_{CPU} = 120 MHz, main PLL f_{VCO} = 480 MHz, stepping done by K2 divider, t_{PLSS} between individual steps:

24 MHz - 48 MHz - 68 MHz - 96 MHz - 120 MHz (K2 steps 20 - 10 - 7 - 5 - 4)
24 MHz - 68 MHz - 96 MHz - 120 MHz (K2 steps 20 - 7 - 5 - 4)
24 MHz - 68 MHz - 120 MHz (K2 steps 20 - 7 - 4)

3.3.5 Internal Clock Source Characteristics

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Fast Internal Clock Source

Table 37 Fast Internal Clock Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal frequency	f_{OFINC} CC	–	36.5	–	MHz	not calibrated
		–	24	–	MHz	calibrated
Accuracy	Δf_{OFI} CC	-0.5	–	0.5	%	automatic calibration[1][2]
		-15	–	15	%	factory calibration, V_{DDP} = 3.3 V
		-25	–	25	%	no calibration, V_{DDP} = 3.3 V
		-7	–	7	%	Variation over voltage range[3] 3.13 V $\leq V_{\mathrm{DDP}} \leq$ 3.63 V
Start-up time	t_{OFIS} CC	–	50	–	µs	

[1] Error in addition to the accuracy of the reference clock.

[2] Automatic calibration compensates variations of the temperature and in the V_{DDP} supply voltage.

[3] Deviations from the nominal V_{DDP} voltage induce an additional error to the uncalibrated and/or factory calibrated oscillator frequency.

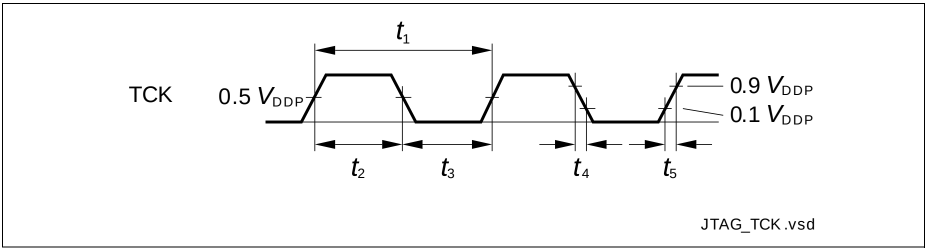


Figure 27 Test Clock Timing (TCK)

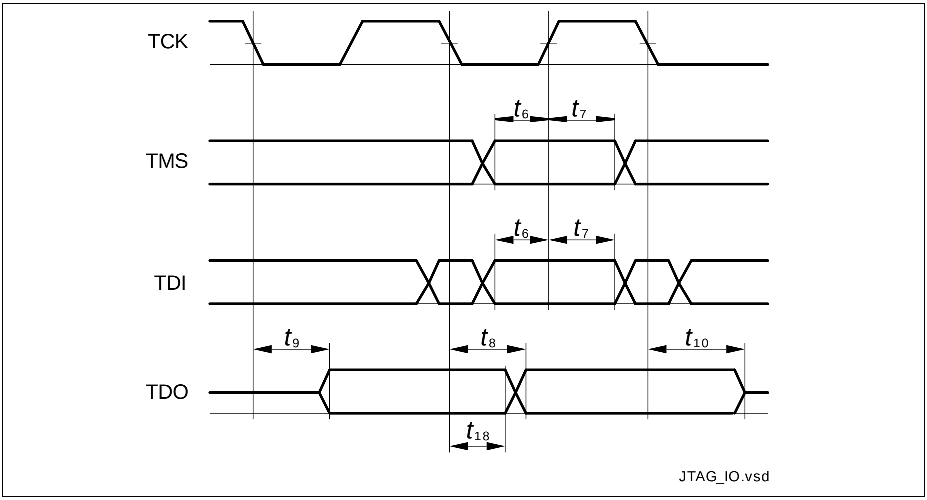


Figure 28 JTAG Timing

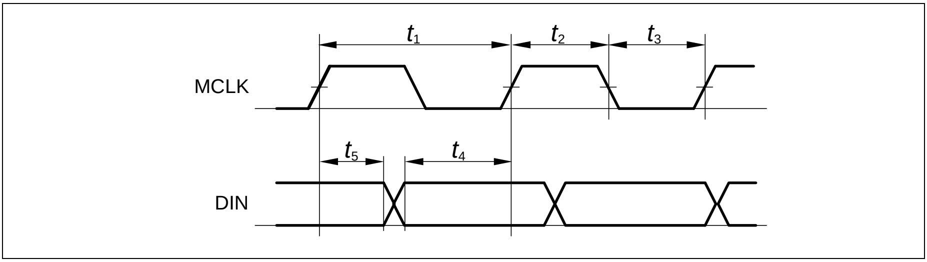


Figure 32 DSD Data Timing

3.3.9.2 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

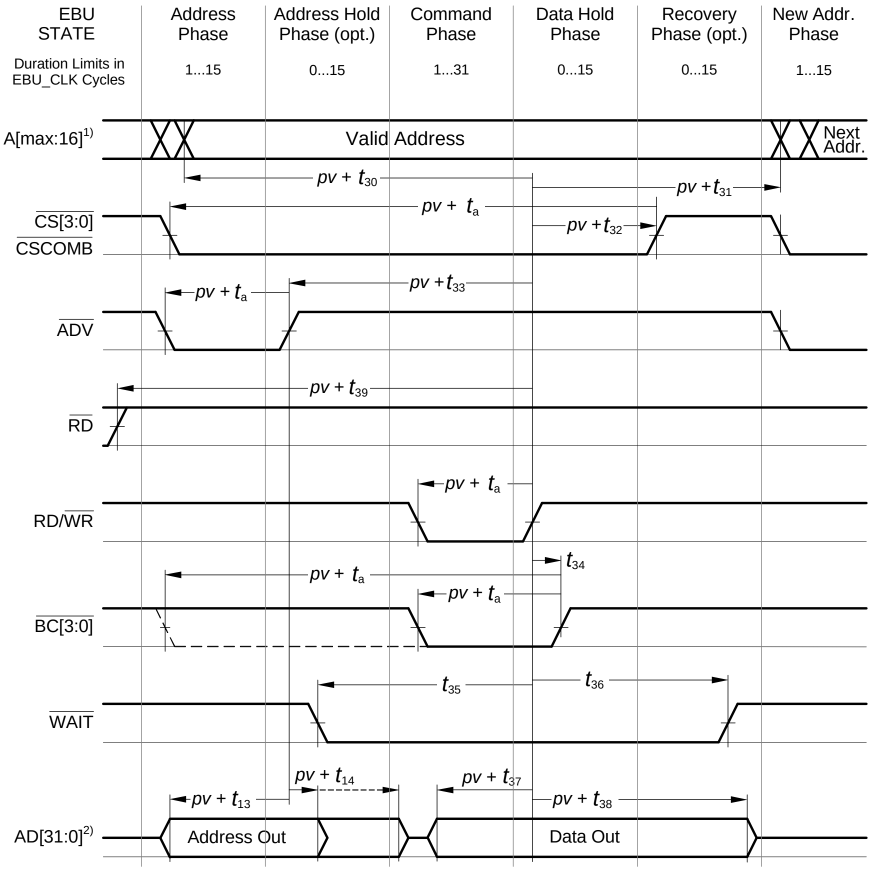
Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 43 USIC SSC Master Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
SCLKOUT master clock period	t_{CLK}	CC	33.3	–	–	ns	
Slave select output SELO active to first SCLKOUT transmit edge	t_1	CC	t_{PB} - 6.5[1]	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2	CC	t_{PB} - 8.5[1]	–	–	ns	
Data output DOUT[3:0] valid time	t_3	CC	-6	–	8	ns	
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	t_4	SR	23	–	–	ns	
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	t_5	SR	1	–	–	ns	

[1] $t_{PB} = 1 / f_{PB}$

Multiplexed Write Timing



[1] For 16-bit MUX and Twin 16-bit MUX only

*[2] * 16-bit MUX: - Address A[15:0], Data D[15:0] on pins AD[15:0] only*
** Twin 16-Bit MUX: - Address A[15:0] on pins AD[15:0] and AD[31:16] in parallel*
- Data D[31:0] on pins AD[31:0]
** 32-bit MUX: - Address A[24:0] on pins AD[24:0]*
- Data D[31:0] on pins AD[31:0]

pv = programmed value,
*T_{EBU_CLK} * sum (corresponding bitfield values)*

EBU_MuxWR_Async.vsd

Figure 43 Multiplexed Write Access

3.3.12.3 ETH MII Parameters

In the following, the parameters of the MII (Media Independent Interface) are described.

Table 62 ETH MII Signal Timing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period, 10 Mbps	t_7 SR	400	–	–	ns	C_L = 25 pF
Clock high time, 10 Mbps	t_8 SR	140	–	260	ns	
Clock low time, 10 Mbps	t_9 SR	140	–	260	ns	
Clock period, 100 Mbps	t_7 SR	40	–	–	ns	
Clock high time, 100 Mbps	t_8 SR	14	–	26	ns	
Clock low time, 100 Mbps	t_9 SR	14	–	26	ns	
Input setup time	t_{10} SR	10	–	–	ns	
Input hold time	t_{11} SR	10	–	–	ns	
Output valid time	t_{12} CC	0	–	25	ns	

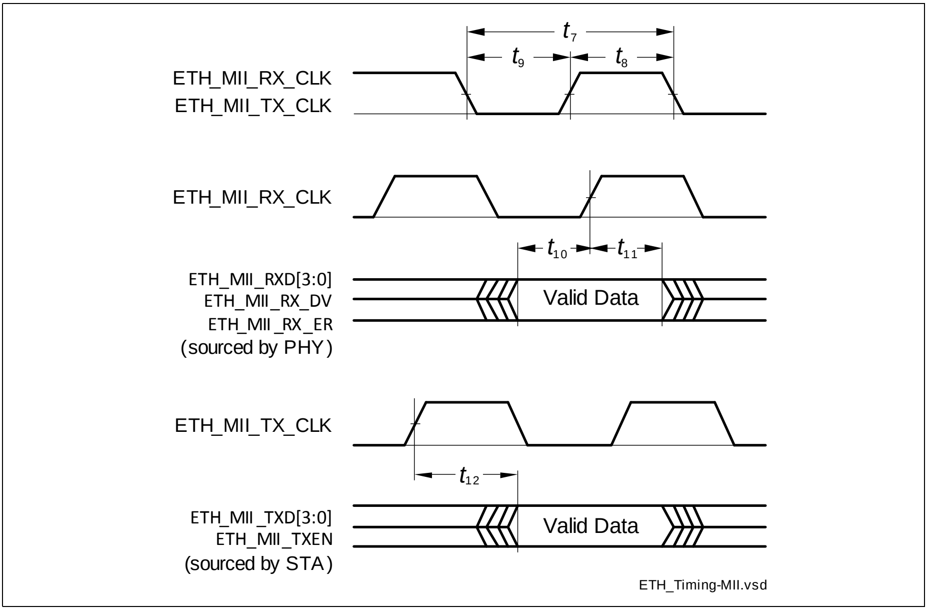
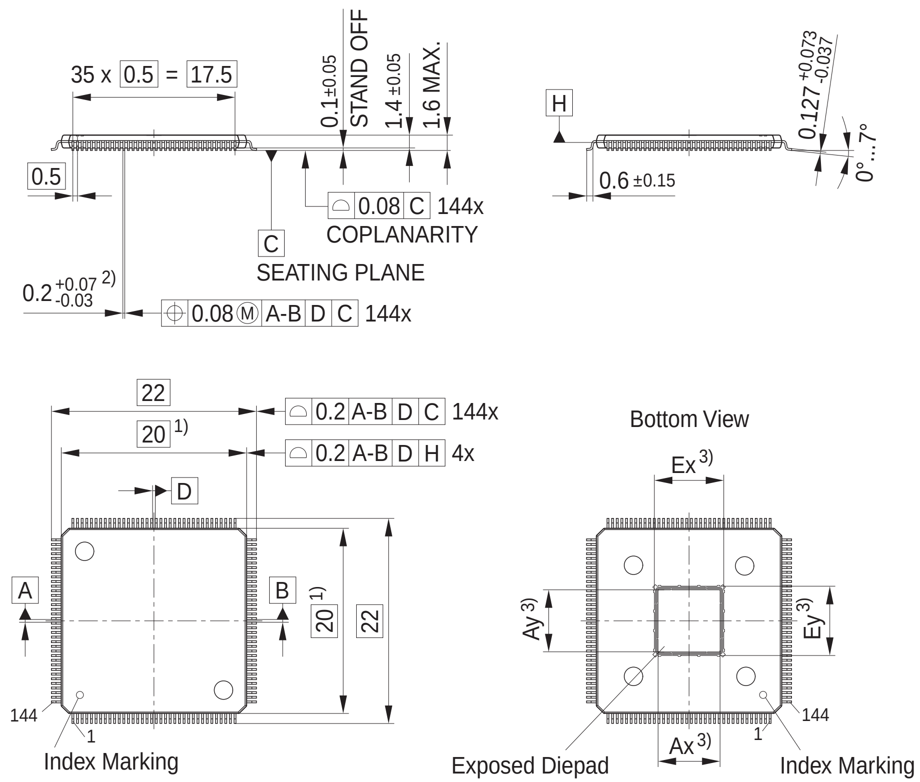


Figure 53 ETH MII Signal Timing



1) Does not include plastic or metal protrusion of 0.25 max. per side
2) Does not include dambar protrusion
3) Refer table for exposed pad dimension

PG-LQFP-144-22-PO V04

Figure 56 **PG-LQFP-144-24** (Plastic Green Low Profile Quad Flat Package)

4.3 Quality Declarations

The qualification of the XMC4500 is executed according to the JEDEC standard JESD47H.

Note: For automotive applications refer to the Infineon automotive microcontrollers.

Table 67 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation lifetime	t_{OP} CC	20	–	–	a	$T_J \leq 109°C$, device permanent on
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	–	–	2 000	V	EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM} SR	–	–	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	–	–	3	–	JEDEC J-STD-020D
Soldering temperature	T_{SDR} SR	–	–	260	°C	Profile according to JEDEC J-STD-020D