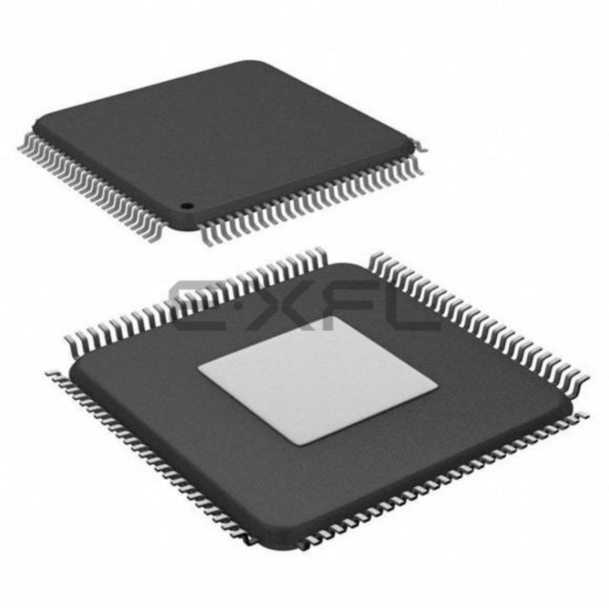

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Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, LED, POR, PWM, WDT
Number of I/O	55
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-11
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4504f100f512acxqma1

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XMC4500 Data Sheet

Revision History: V1.4 2016-01

Previous Versions:
V1.3, 2014-03
V1.2, 2013-07
V1.1, 2013-07
V1.0, 2013-01
V0.9, 2012-12
V0.8, 2012-11

Page	Subjects
43	Added information that $\overline{\text{PORST}}$ Pull-up is identical to the pull-up on standard I/O pins.
42	Added footnote explaining minimum V_{BAT} requirements to start the hibernate domain and/or oscillation of a crystal on RTC_XTAL.
59	Corrected parameter name of of USB pull device (upstream port receiving) definition according to USB standard (referenced to DM instead of DP)
61	Relaxed RTC_XTAL V_{PPX} parameter value and changed it to a system requirement.
115ff	Added PG-LQFP-100-25 and PG-LQFP-144-24 package information.
115	Added tables describing the differences between PG-LQFP-100-11 to PG-LQFP-100-25 as well as PG-LQFP-144-18 to PG-LQFP-144-24 packages.

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mcdocu.comments@infineon.com

Input/Output Lines

- Programmable port driver control module (PORTS)
- Individual bit addressability
- Tri-stated in input mode
- Push/pull or open drain output mode
- Boundary scan test support over JTAG interface

On-Chip Debug Support

- Full support for debug features: 8 breakpoints, CoreSight, trace
- Various interfaces: ARM-JTAG, SWD, single wire trace

1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code "XMC4<DDD>-<Z><PPP><T><FFFF>" identifies:

- <DDD> the derivatives function set
- <Z> the package variant
  - E: LFBGA
  - F: LQFP
  - Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
  - F: -40°C to 85°C
  - X: -40°C to 105°C
  - K: -40°C to 125°C
- <FFFF> the Flash memory size.

For ordering codes for the XMC4500 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC4500 series, some descriptions may not apply to a specific product.

For simplicity the term **XMC4500** is used for all derivatives throughout this document.

2.2.1 Package Pin Summary

The following general scheme is used to describe each pin:

Table 8 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type	Notes
Name	N	Ax	...	A2	

The table is sorted by the "Function" column, starting with the regular Port pins (Px.y), followed by the dedicated pins (i.e. $\overline{\text{PORST}}$) and supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The "Pad Type" indicates the employed pad type (A1, A1+, A2, special=special pad, In=input pad, AN/DIG_IN=analog and digital input, Power=power supply). Details about the pad properties are defined in the Electrical Parameters.

In the "Notes", special information to the respective pin/function is given, i.e. deviations from the default configuration after reset. Per default the regular Port pins are configured as direct input with no internal pull device active.

Table 9 Package Pin Mapping

Function	LQFP-144	LFBGA-144	LQFP-100	Pad Type	Notes
P0.0	2	C4	2	A1+	
P0.1	1	C3	1	A1+	
P0.2	144	A3	100	A2	
P0.3	143	A4	99	A2	
P0.4	142	B5	98	A2	
P0.5	141	A5	97	A2	
P0.6	140	A6	96	A2	
P0.7	128	B7	89	A2	After a system reset, via HWSEL this pin selects the DB.TDI function.
P0.8	127	A8	88	A2	After a system reset, via HWSEL this pin selects the DB.$\overline{\text{TRST}}$ function, with a weak pull-down active.
P0.9	4	D4	4	A2	
P0.10	3	B4	3	A1+	

2.2.2.1 Port I/O Function Table

Table 11 Port I/O Functions

Function	Outputs						Inputs									
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P0.0		CAN.N0_TXD	CCU80.OUT21	LEDTS0.COL2					U1C1.DX0D	ETH0.CLK_RMIIB	ERU0.0B0					ETH0.CLKRXB
P0.1	USB.DRIVEVBUS	U1C1.DOUT0	CCU80.OUT11	LEDTS0.COL3						ETH0.CRS_DVB	ERU0.0A0					ETH0.RXDVB
P0.2		U1C1.SELO1	CCU80.OUT01		U1C0.DOUT3	EBU.AD0	U1C0.HWIN3	EBU.D0	ETH0.RXD0B		ERU0.3B3					
P0.3			CCU80.OUT20		U1C0.DOUT2	EBU.AD1	U1C0.HWIN2	EBU.D1	ETH0.RXD1B			ERU1.3B0				
P0.4	ETH0.TX_EN		CCU80.OUT10		U1C0.DOUT1	EBU.AD2	U1C0.HWIN1	EBU.D2		U1C0.DX0A	ERU0.2B3					
P0.5	ETH0.TXD0	U1C0.DOUT0	CCU80.OUT00		U1C0.DOUT0	EBU.AD3	U1C0.HWIN0	EBU.D3		U1C0.DX0B		ERU1.3A0				
P0.6	ETH0.TXD1	U1C0.SELO0	CCU80.OUT30			EBU.$\overline{\text{ADV}}$				U1C0.DX2A	ERU0.3B2		CCU80.IN2B			
P0.7	WWDT.SERVICE_OUT	U0C0.SELO0				EBU.AD6	DB.TDI	EBU.D6	U0C0.DX2B	DSD.DIN1A	ERU0.2B1		CCU80.IN0A	CCU80.IN1A	CCU80.IN2A	CCU80.IN3A
P0.8	SCU.EXTCLK	U0C0.SCLKOUT				EBU.AD7	DB.$\overline{\text{TRST}}$	EBU.D7	U0C0.DX1B	DSD.DIN0A	ERU0.2A1		CCU80.IN1B			
P0.9		U1C1.SELO0	CCU80.OUT12	LEDTS0.COL0	ETH0.MDO	EBU.$\overline{\text{CS1}}$	ETH0.MDIA		U1C1.DX2A	USB.ID	ERU0.1B0					
P0.10	ETH0.MDC	U1C1.SCLKOUT	CCU80.OUT02	LEDTS0.COL1					U1C1.DX1A		ERU0.1A0					
P0.11		U1C0.SCLKOUT	CCU80.OUT31		SDMMC.$\overline{\text{RST}}$	EBU.$\overline{\text{BREQ}}$			ETH0.RXERB	U1C0.DX1A	ERU0.3A2					
P0.12		U1C1.SELO0	CCU40.OUT3			EBU.$\overline{\text{HLDA}}$		EBU.$\overline{\text{HLDA}}$		U1C1.DX2B	ERU0.2B2					
P0.13		U1C1.SCLKOUT	CCU40.OUT2							U1C1.DX1B	ERU0.2A2					
P0.14		U1C0.SELO1	CCU40.OUT1		U1C1.DOUT3		U1C1.HWIN3						CCU42.IN3C			
P0.15		U1C0.SELO2	CCU40.OUT0		U1C1.DOUT2		U1C1.HWIN2						CCU42.IN2C			
P1.0	DSD.CGPWMN	U0C0.SELO0	CCU40.OUT3	ERU1.PDOUT3					U0C0.DX2A		ERU0.3B0		CCU40.IN3A			
P1.1	DSD.CGPWMP	U0C0.SCLKOUT	CCU40.OUT2	ERU1.PDOUT2			SDMMC.SDWC		U0C0.DX1A	POSIF0.IN2A	ERU0.3A0		CCU40.IN2A			
P1.2			CCU40.OUT1	ERU1.PDOUT1	U0C0.DOUT3	EBU.AD14	U0C0.HWIN3	EBU.D14		POSIF0.IN1A		ERU1.2B0	CCU40.IN1A			
P1.3		U0C0.MCLKOUT	CCU40.OUT0	ERU1.PDOUT0	U0C0.DOUT2	EBU.AD15	U0C0.HWIN2	EBU.D15		POSIF0.IN0A		ERU1.2A0	CCU40.IN0A			
P1.4	WWDT.SERVICE_OUT	CAN.N0_TXD	CCU80.OUT33	CCU81.OUT20	U0C0.DOUT1		U0C0.HWIN1		U0C0.DX0B	CAN.N1_RXDD	ERU0.2B0		CCU41.IN0C			

Table 11 Port I/O Functions (cont'd)

Function	Outputs						Inputs									
	ALT1	**ALT2**	**ALT3**	**ALT4**	**HWO0**	**HWO1**	**HWI0**	**HWI1**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**
P1.5	CAN.N1_TXD	U0C0.DOUT0	CCU80.OUT23	CCU81.OUT10	U0C0.DOUT0		U0C0.HWIN0		U0C0.DX0A	CAN.N0_RXDA	ERU0.2A0	ERU1.0A0	CCU41.IN1C	DSD.DIN2B		
P1.6		U0C0.SCLKOUT			SDMMC.DATA1_OUT	EBU.AD10	SDMMC.DATA1_IN	EBU.D10	DSD.DIN2A							
P1.7		U0C0.DOUT0	DSD.MCLK2		SDMMC.DATA2_OUT	EBU.AD11	SDMMC.DATA2_IN	EBU.D11		DSD.MCLK2A						
P1.8		U0C0.SELO1	DSD.MCLK1		SDMMC.DATA4_OUT	EBU.AD12	SDMMC.DATA4_IN	EBU.D12	CAN.N2_RXDA	DSD.MCLK1A						
P1.9		CAN.N2_TXD			SDMMC.DATA5_OUT	EBU.AD13	SDMMC.DATA5_IN	EBU.D13		DSD.MCLK0A						
P1.10	ETH0.MDC	U0C0.SCLKOUT	CCU81.OUT21				$\overline{\text{SDMMC.SDCD}}$						CCU41.IN2C			
P1.11		U0C0.SELO0	CCU81.OUT11		ETH0.MDO		ETH0.MDIC						CCU41.IN3C			
P1.12	ETH0.TX_EN	CAN.N1_TXD	CCU81.OUT01		SDMMC.DATA6_OUT	EBU.AD16	SDMMC.DATA6_IN	EBU.D16								
P1.13	ETH0.TXD0	U0C1.SELO3	CCU81.OUT20		SDMMC.DATA7_OUT	EBU.AD17	SDMMC.DATA7_IN	EBU.D17	CAN.N1_RXDC							
P1.14	ETH0.TXD1	U0C1.SELO2	CCU81.OUT10			EBU.AD18		EBU.D18								
P1.15	SCU.EXTCLK	DSD.MCLK2	CCU81.OUT00			EBU.AD19		EBU.D19		DSD.MCLK2B		ERU1.1A0				
P2.0		CCU81.OUT21	DSD.CGPWMN	LEDTS0.COL1	ETH0.MDO	EBU.AD20	ETH0.MDIB	EBU.D20			ERU0.0B3		CCU40.IN1C			
P2.1		CCU81.OUT11	DSD.CGPWMP	LEDTS0.COL0	DB.TDO/TRACESWO	EBU.AD21		EBU.D21	ETH0.CLK_RMIIA			ERU1.0B0	CCU40.IN0C			ETH0.CLKRXA
P2.2	VADC.EMUX00	CCU81.OUT01	CCU41.OUT3	LEDTS0.LINE0	LEDTS0.EXTENDED0	EBU.AD22	LEDTS0.TSIN0A	EBU.D22	ETH0.RXD0A	U0C1.DX0A	ERU0.1B2		CCU41.IN3A			
P2.3	VADC.EMUX01	U0C1.SELO0	CCU41.OUT2	LEDTS0.LINE1	LEDTS0.EXTENDED1	EBU.AD23	LEDTS0.TSIN1A	EBU.D23	ETH0.RXD1A	U0C1.DX2A	ERU0.1A2	POSIF1.IN2A	CCU41.IN2A			
P2.4	VADC.EMUX02	U0C1.SCLKOUT	CCU41.OUT1	LEDTS0.LINE2	LEDTS0.EXTENDED2	EBU.AD24	LEDTS0.TSIN2A	EBU.D24	ETH0.RXERA	U0C1.DX1A	ERU0.0B2	POSIF1.IN1A	CCU41.IN1A			
P2.5	ETH0.TX_EN	U0C1.DOUT0	CCU41.OUT0	LEDTS0.LINE3	LEDTS0.EXTENDED3	EBU.AD25	LEDTS0.TSIN3A	EBU.D25	ETH0.RXDVA	U0C1.DX0B	ERU0.0A2	POSIF1.IN0A	CCU41.IN0A			ETH0.CRS_DVA
P2.6	U2C0.SELO4		CCU80.OUT13	LEDTS0.COL3	U2C0.DOUT3		U2C0.HWIN3		DSD.DIN1B	CAN.N1_RXDA	ERU0.1B3		CCU40.IN3C			
P2.7	ETH0.MDC	CAN.N1_TXD	CCU80.OUT03	LEDTS0.COL2					DSD.DIN0B			ERU1.1B0	CCU40.IN2C			
P2.8	ETH0.TXD0		CCU80.OUT32	LEDTS0.LINE4	LEDTS0.EXTENDED4	EBU.AD26	LEDTS0.TSIN4A	EBU.D26	DAC.TRIGGER5				CCU40.IN0B	CCU40.IN1B	CCU40.IN2B	CCU40.IN3B
P2.9	ETH0.TXD1		CCU80.OUT22	LEDTS0.LINE5	LEDTS0.EXTENDED5	EBU.AD27	LEDTS0.TSIN5A	EBU.D27	DAC.TRIGGER4				CCU41.IN0B	CCU41.IN1B	CCU41.IN2B	CCU41.IN3B
P2.10	VADC.EMUX10				DB.ETM_TRACEDATA3	EBU.AD28		EBU.D28								
P2.11	ETH0.TXER		CCU80.OUT22		DB.ETM_TRACEDATA2	EBU.AD29		EBU.D29								

Table 11 Port I/O Functions (cont'd)

Function	Outputs						Inputs									
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P15.12												VADC. G3CH4				
P15.13												VADC. G3CH5				
P15.14												VADC. G3CH6				
P15.15												VADC. G3CH7				
USB_DP																
USB_DM																
HIB_IO_0	HIBOUT	WWDT. SERVICE_OUT							WAKEUPA							
HIB_IO_1	HIBOUT	WWDT. SERVICE_OUT							WAKEUPB							
TCK							DB.TCK/ SWCLK									
TMS					DB.TMS/ SWDIO											
$\overline{\text{PORST}}$																
XTAL1									U0C0. DX0F	U0C1. DX0F	U1C0. DX0F	U1C1. DX0F	U2C0. DX0F	U2C1. DX0F		
XTAL2																
RTC_XTAL1											ERU0. 1B1					
RTC_XTAL2																

3.1.4 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and their basic characteristics.

Table 17 Pad Driver and Pad Classes Overview

Class	Power Supply	Type	Sub-Class	Speed Grade	Load	Termination
A	3.3 V	LVTTL I/O	**A1** (e.g. GPIO)	6 MHz	100 pF	No
			A1+ (e.g. serial I/Os)	25 MHz	50 pF	Series termination recommended
			A2 (e.g. ext. Bus)	80 MHz	15 pF	Series termination recommended

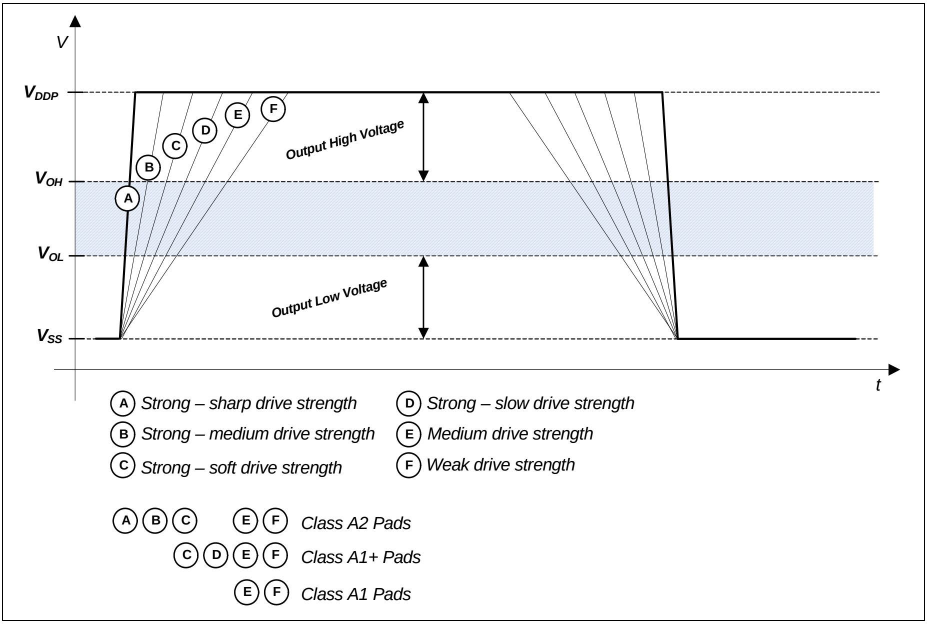


Figure 12 Output Slopes with different Pad Driver Modes

Figure 12 is a qualitative display of the resulting output slope performance with different output driver modes. The detailed input and output characteristics are listed in **Section 3.2.1**.

Table 22 Standard Pads Class_A2

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Fall time	t_{FA2} CC	–		150	ns	C_L = 20 pF; POD = weak
		–		50	ns	C_L = 50 pF; POD = medium
		–		3.7	ns	C_L = 50 pF; POD = strong; edge = sharp
		–		7	ns	C_L = 50 pF; POD = strong; edge = medium
		–		16	ns	C_L = 50 pF; POD = strong; edge = soft
Rise time	t_{RA2} CC	–		150	ns	C_L = 20 pF; POD = weak
		–		50	ns	C_L = 50 pF; POD = medium
		–		3.7	ns	C_L = 50 pF; POD = strong; edge = sharp
		–		7.0	ns	C_L = 50 pF; POD = strong; edge = medium
		–		16	ns	C_L = 50 pF; POD = strong; edge = soft

Table 23 VADC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Total Unadjusted Error	*TUE* CC	-4	–	4	LSB	12-bit resolution; V_{DDA} = 3.3 V; $V_{AREF} = V_{DDA}$ 7)
Differential Non-Linearity Error[8)]	EA_{DNL} CC	-3	–	3	LSB	
Gain Error[8)]	EA_{GAIN} CC	-4	–	4	LSB	
Integral Non-Linearity[8)]	EA_{INL} CC	-3	–	3	LSB	
Offset Error[8)]	EA_{OFF} CC	-4	–	4	LSB	
Worst case ADC V_{DDA} power supply current per active converter	I_{DDAA} CC	–	1.5	2	mA	during conversion V_{DDP} = 3.6 V, T_J = 150 °C
Charge consumption on V_{AREF} per conversion[5)]	Q_{CONV} CC	–	30	–	pC	0 V ≤ V_{AREF} ≤ V_{DDA} 9)
ON resistance of the analog input path	R_{AIN} CC	–	700	1 700	Ohm	
ON resistance for the ADC test (pull down for AIN7)	R_{AIN7T} CC	180	550	900	Ohm	
Resistance of the reference voltage input path	R_{AREF} CC	–	700	1 700	Ohm	

1) A running conversion may become imprecise in case the normal conditions are violated (voltage overshoot).

2) If the analog reference voltage is below V_{DDA}, then the ADC converter errors increase. If the reference voltage is reduced by the factor k (k<1), TUE, DNL, INL, Gain, and Offset errors increase also by the factor 1/k.

3) The leakage current definition is a continuous function, as shown in figure ADCx Analog Inputs Leakage. The numerical values defined determine the characteristic points of the given continuous linear approximation - they do not define step function (see **Figure 16**).

4) The sampling capacity of the conversion C-network is pre-charged to $V_{AREF}/2$ before the sampling moment. Because of the parasitic elements, the voltage measured at AINx can deviate from $V_{AREF}/2$.

5) Applies to AINx, when used as alternate reference input.

6) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead, smaller capacitances are successively switched to the reference voltage.

7) For 10-bit conversions, the errors are reduced to 1/4; for 8-bit conversions, the errors are reduced to 1/16. Never less than ±1 LSB.

8) The sum of DNL/INL/GAIN/OFF errors does not exceed the related total unadjusted error TUE.

9) The resulting current for a conversion can be calculated with $I_{AREF} = Q_{CONV} / t_c$.
The fastest 12-bit post-calibrated conversion of t_c = 550 ns results in a typical average current of I_{AREF} = 54.5 µA.

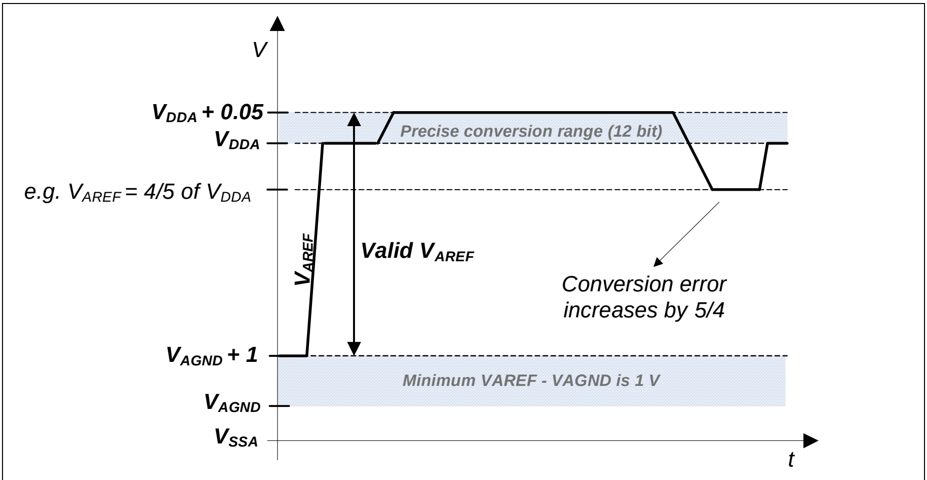


Figure 14 VADC Reference Voltage Range

The power-up calibration of the VADC requires a maximum number of 4 352 f_{ADCI} cycles.

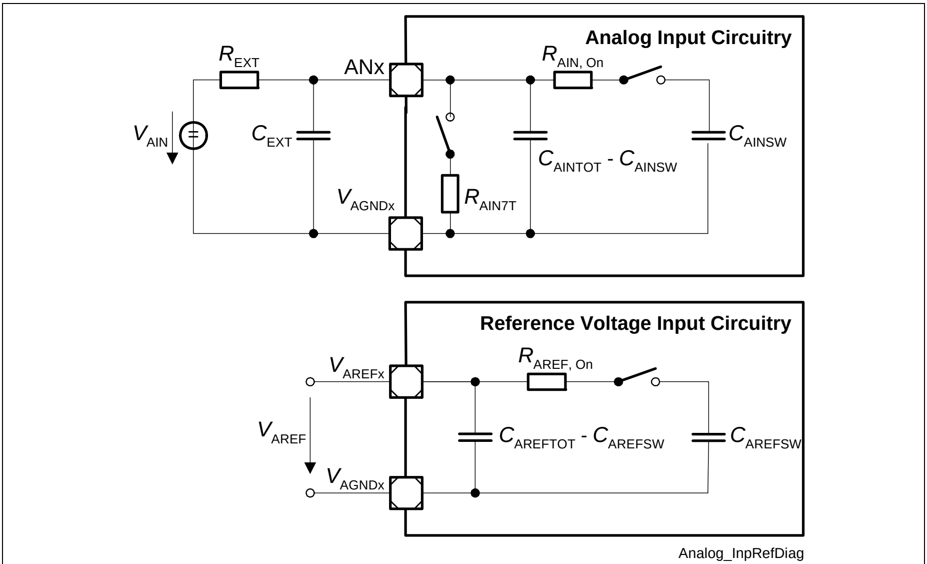


Figure 15 VADC Input Circuits

Table 29 **USB OTG Data Line (USB_DP, USB_DM) Parameters** (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Input low voltage	V_{IL}	SR	–	–	0.8	V	
Input high voltage (driven)	V_{IH}	SR	2.0	–	–	V	
Input high voltage (floating) [1)]	V_{IHZ}	SR	2.7	–	3.6	V	
Differential input sensitivity	V_{DIS}	CC	0.2	–	–	V	
Differential common mode range	V_{CM}	CC	0.8	–	2.5	V	
Output low voltage	V_{OL}	CC	0.0	–	0.3	V	1.5 kOhm pull-up to 3.6 V
Output high voltage	V_{OH}	CC	2.8	–	3.6	V	15 kOhm pull-down to 0 V
DP pull-up resistor (idle bus)	R_{PUI}	CC	900	–	1 575	Ohm	
DP pull-up resistor (upstream port receiving)	R_{PUA}	CC	1 425	–	3 090	Ohm	
DP, DM pull-down resistor	R_{PD}	CC	14.25	–	24.8	kOhm	
Input impedance DP, DM	Z_{INP}	CC	300	–	–	kOhm	$0\ V \leq V_{IN} \leq V_{DDP}$
Driver output resistance DP, DM	Z_{DRV}	CC	28	–	44	Ohm	

1) Measured at A-connector with 1.5 kOhm ± 5% to 3.3 V ± 0.3 V connected to USB_DP or USB_DM and at B-connector with 15 kOhm ± 5% to ground connected to USB_DP and USB_DM.

Table 35 Power Sequencing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Positive Load Step Current	ΔI_{PLS} SR	-	–	50	mA	Load increase on V_{DDP} $\Delta t \leq$ 10 ns
Negative Load Step Current	ΔI_{NLS} SR	-	–	150	mA	Load decrease on V_{DDP} $\Delta t \leq$ 10 ns
V_{DDC} Voltage Over- / Undershoot from Load Step	ΔV_{LS} CC	-	–	±100	mV	For maximum positive or negative load step
Positive Load Step Settling Time	t_{PLSS} SR	50	–	-	µs	
Negative Load Step Settling Time	t_{NLSS} SR	100	–	-	µs	
External Buffer Capacitor on V_{DDC}	C_{EXT} SR	-	10	-	µF	In addition C = 100 nF capacitor on each V_{DDC} pin

Positive Load Step Examples

System assumptions:
$f_{CPU} = f_{SYS}$, target frequency f_{CPU} = 120 MHz, main PLL f_{VCO} = 480 MHz, stepping done by K2 divider, t_{PLSS} between individual steps:

24 MHz - 48 MHz - 68 MHz - 96 MHz - 120 MHz (K2 steps 20 - 10 - 7 - 5 - 4)
24 MHz - 68 MHz - 96 MHz - 120 MHz (K2 steps 20 - 7 - 5 - 4)
24 MHz - 68 MHz - 120 MHz (K2 steps 20 - 7 - 4)

3.3.5 Internal Clock Source Characteristics

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Fast Internal Clock Source

Table 37 Fast Internal Clock Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal frequency	f_{OFINC} CC	–	36.5	–	MHz	not calibrated
		–	24	–	MHz	calibrated
Accuracy	Δf_{OFI} CC	-0.5	–	0.5	%	automatic calibration[1)2)]
		-15	–	15	%	factory calibration, V_{DDP} = 3.3 V
		-25	–	25	%	no calibration, V_{DDP} = 3.3 V
		-7	–	7	%	Variation over voltage range[3)] 3.13 V $\leq V_{DDP} \leq$ 3.63 V
Start-up time	t_{OFIS} CC	–	50	–	µs	

1) Error in addition to the accuracy of the reference clock.

2) Automatic calibration compensates variations of the temperature and in the V_{DDP} supply voltage.

3) Deviations from the nominal V_{DDP} voltage induce an additional error to the uncalibrated and/or factory calibrated oscillator frequency.

3.3.9.5 SDMMC Interface Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply, total external capacitive load C_L = 40 pF.

AC Timing Specifications (Full-Speed Mode)

Table 49 SDMMC Timing for Full-Speed Mode

Parameter	Symbol		Values		Unit	Note/ Test Condition
			Min.	Max.		
Clock frequency in full speed transfer mode ($1/t_{pp}$)	f_{pp}	CC	0	24	MHz	
Clock cycle in full speed transfer mode	t_{pp}	CC	40	–	ns	
Clock low time	t_{WL}	CC	10	–	ns	
Clock high time	t_{WH}	CC	10	–	ns	
Clock rise time	t_{TLH}	CC	–	10	ns	
Clock fall time	t_{THL}	CC	–	10	ns	
Inputs setup to clock rising edge	t_{ISU_F}	SR	2	–	ns	
Inputs hold after clock rising edge	t_{IH_F}	SR	2	–	ns	
Outputs valid time in full speed mode	t_{ODLY_F}	CC	–	10	ns	
Outputs hold time in full speed mode	t_{OH_F}	CC	0	–	ns	

Table 50 SD Card Bus Timing for Full-Speed Mode[1)]

Parameter	Symbol	Values		Unit	Note/ Test Condition
		Min.	Max.		
SD card input setup time	t_{ISU}	5	–	ns	
SD card input hold time	t_{IH}	5	–	ns	

Table 50 SD Card Bus Timing for Full-Speed Mode[1] (cont'd)

Parameter	Symbol	Values		Unit	Note/ Test Condition
		Min.	Max.		
SD card output valid time	t_{ODLY}	–	14	ns	
SD card output hold time	t_{OH}	0	–	ns	

1) Reference card timing values for calculation examples. Not subject to production test and not characterized.

Full-Speed Output Path (Write)

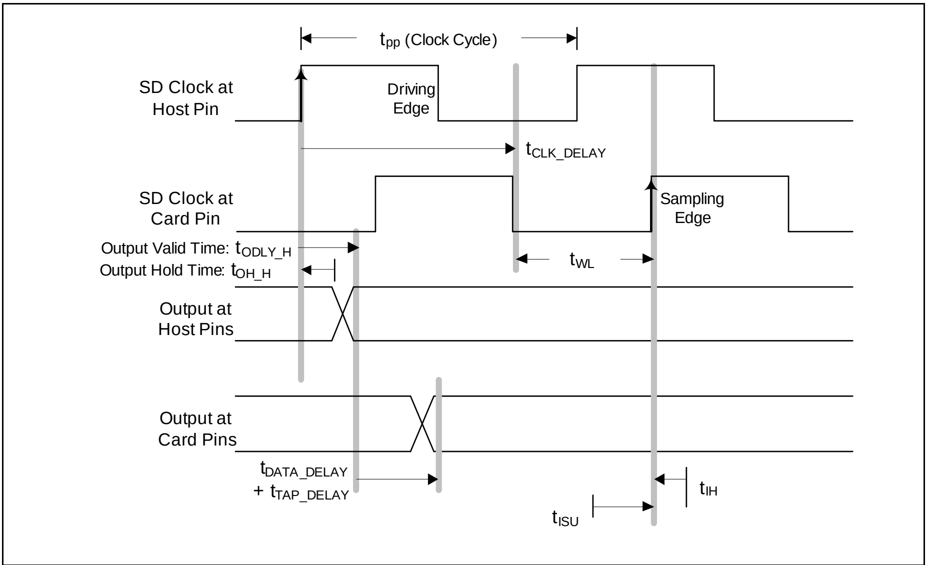


Figure 37 Full-Speed Output Path

Full-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

No clock delay:

(1)

$$t_{ODLY\_F} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ISU} < t_{WL}$$

High-Speed Read Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

(12)

$$t_{CLK\_DELAY} + t_{OH} + t_{DATA\_DELAY} + t_{TAP\_DELAY} > t_{IH\_H}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} > t_{IH\_H} - t_{OH} - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} > 2 - 2{,}5 - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} > -0{,}5 - t_{TAP\_DELAY}$$

The data + clock delay must be greater than -0.5 ns for a 20 ns clock cycle. This is always fulfilled.

3.3.10 EBU Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply, with Class A2 pins and C_L = 16 pF.

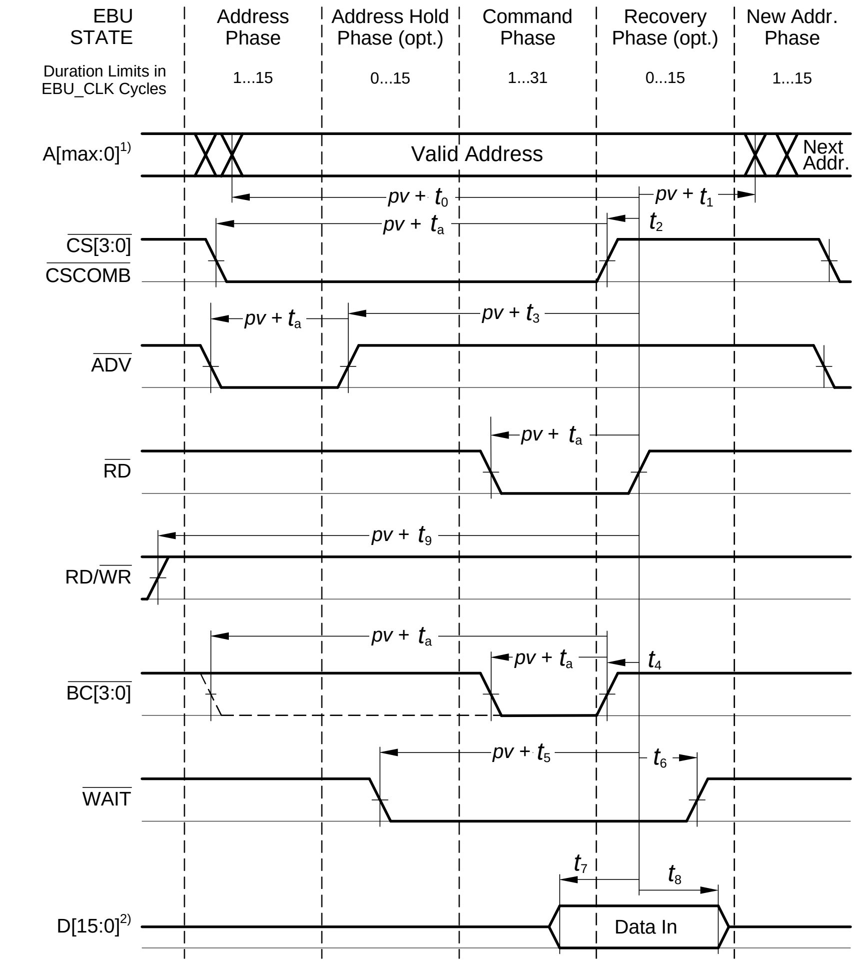
3.3.10.1 EBU Asynchronous Timing

Note: For each timing, the accumulated PLL jitter must be added separately.

Table 53 Common Timing Parameters for all Asynchronous Timings

Parameter			Symbol	Limit Values		Unit	Edge Setting
				Min.	Max.		
Pulse width deviation from the ideal programmed width due to the A2 pad asymmetry, strong driver mode, rise delay - fall delay. C_L = 16 pF.		CC	t_a	-1	1.5	ns	sharp
				-2	1		medium
AD(24:16) output delay	to $\overline{ADV}$ rising edge, multiplexed read / write	CC	t_{13}	-5.5	2		–
AD(24:16) output delay		CC	t_{14}	-5.5	2		–

Demultiplexed Read Timing



1) Address A[max:16] on pins A[max:16], Address A[15:0] on pins AD[31:16]
2) Data D[15:0] on pins AD[15:0]

pv = programmed value,
*T_{EBU_CLK} * sum (corresponding bitfield values)*

EBU_DeMuxRD_Async.vsd

Figure 42 Demultiplexed Read Access

3.3.10.4 EBU SDRAM Access Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply, with Class A2 pins and C_L = 16 pF.

Table 58 EBU SDRAM Access SDCLKO Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Con dition
			Min.	Typ.	Max.		
SDCLKO period	t_1	CC	12.5	–	–	ns	–
SDCLKO high time	t_2	SR	5.5	–	–	ns	–
SDCLKO low time	t_3	SR	3.75	–	–	ns	–
SDCLKO rise time	t_4	SR	–	–	3.0	ns	–
SDCLKO fall time	t_5	SR	–	–	3.0	ns	–

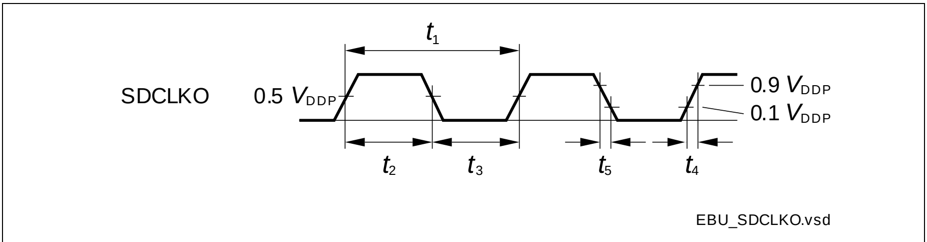


Figure 47 EBU SDRAM Access CLKOUT Timing

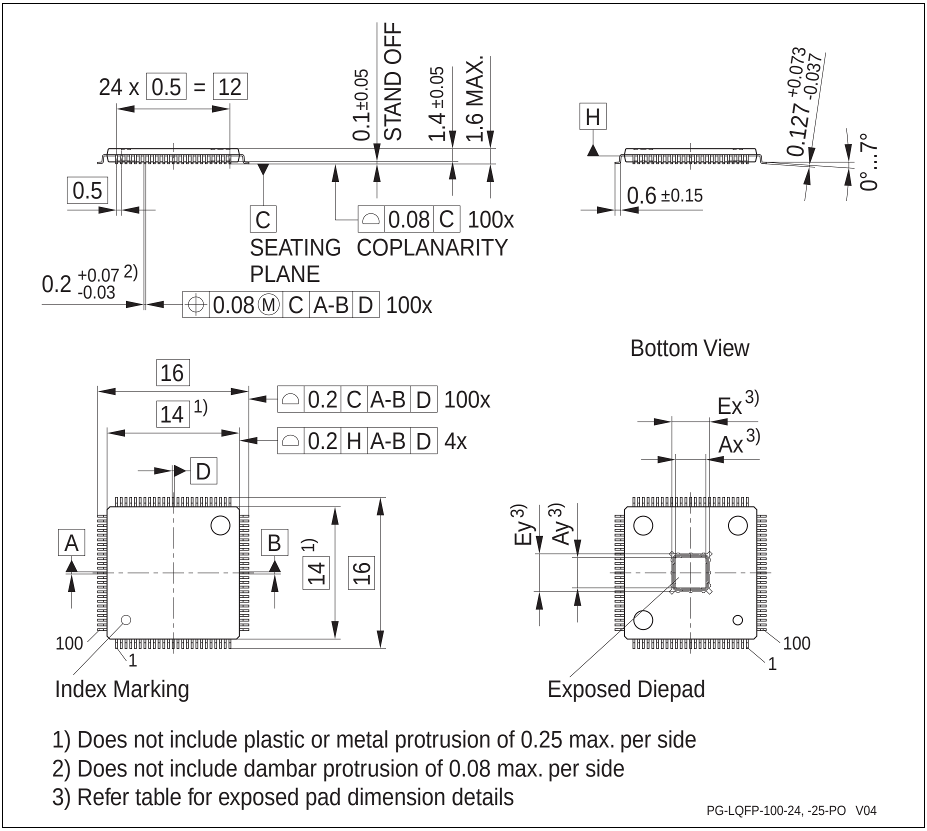


Figure 58 **PG-LQFP-100-25** (Plastic Green Low Profile Quad Flat Package)