Infineon Technologies - XMC4504F144F512ABXQMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, LED, POR, PWM, WDT
Number of I/O	91
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-18
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4504f144f512abxqma1

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Table 4 Flash Memory Ranges (cont'd)

Total Flash Size	Cached Range	Uncached Range
768 Kbytes	$0800\ 0000_H$ – $080B\ FFFF_H$	$0C00\ 0000_H$ – $0C0B\ FFFF_H$
1,024 Kbytes	$0800\ 0000_H$ – $080F\ FFFF_H$	$0C00\ 0000_H$ – $0C0F\ FFFF_H$

Table 5 SRAM Memory Ranges

Total SRAM Size	Program SRAM	System Data SRAM	Communication Data SRAM
128 Kbytes	$1000\ 0000_H$ – $1000\ FFFF_H$	$2000\ 0000_H$ – $2000\ FFFF_H$	–
160 Kbytes	$1000\ 0000_H$ – $1000\ FFFF_H$	$2000\ 0000_H$ – $2000\ FFFF_H$	$3000\ 0000_H$ – $3000\ 7FFF_H$

Table 6 ADC Channels[1)]

Package	VADC G0	VADC G1	VADC G2	VADC G3
PG-LQFP-144 PG-LFBGA-144	CH0..CH7	CH0..CH7	CH0..CH7	CH0..CH7
PG-LQFP-100	CH0..CH7	CH0..CH7	CH0..CH3	CH0..CH3

1) Some pins in a package may be connected to more than one channel. For the detailed mapping see the Port I/O Function table.

1.5 Identification Registers

The identification registers allow software to identify the marking.

Table 7 XMC4500 Identification Registers

Register Name	Value	Marking
SCU_IDCHIP	$0004\ 5002_H$	EES-AA, ES-AA
SCU_IDCHIP	$0004\ 5003_H$	ES-AB, AB
SCU_IDCHIP	$0004\ 5004_H$	AC
JTAG IDCODE	$101D\ B083_H$	EES-AA, ES-AA
JTAG IDCODE	$101D\ B083_H$	ES-AB, AB
JTAG IDCODE	$401D\ B083_H$	AC

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

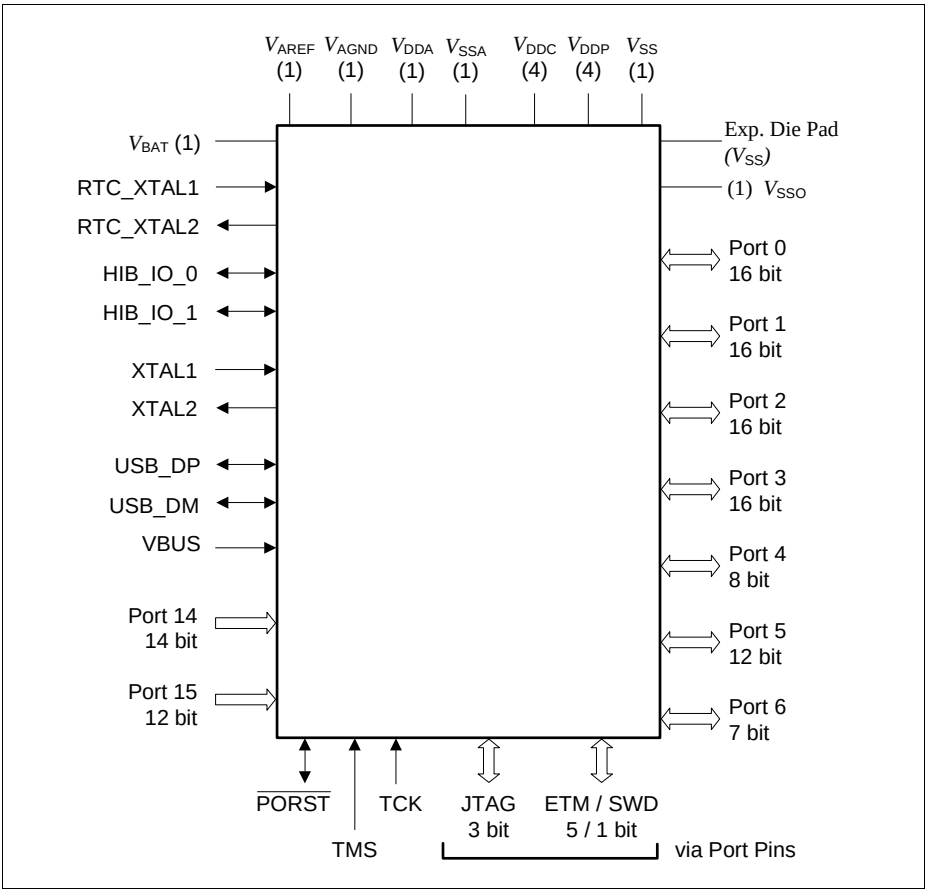

Figure 2 XMC4500 Logic Symbol PG-LQFP-144

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the four sides of the different packages.

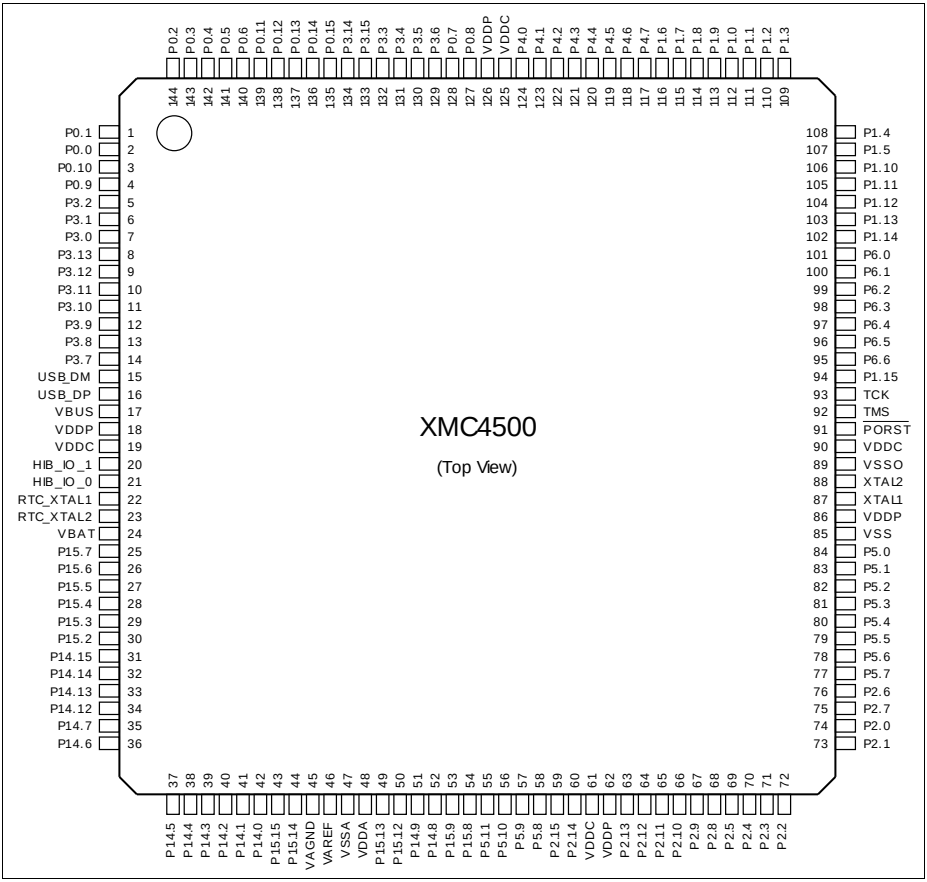

Figure 5 XMC4500 PG-LQFP-144 Pin Configuration (top view)

Table 9 Package Pin Mapping (cont'd)

Function	LQFP-144	LFBGA-144	LQFP-100	Pad Type	Notes
P0.11	139	E5	95	A1+	
P0.12	138	D5	94	A1+	
P0.13	137	C5	-	A1+	
P0.14	136	E6	-	A1+	
P0.15	135	C6	-	A1+	
P1.0	112	D9	79	A1+	
P1.1	111	E9	78	A1+	
P1.2	110	C11	77	A2	
P1.3	109	C12	76	A2	
P1.4	108	C10	75	A1+	
P1.5	107	D10	74	A1+	
P1.6	116	B9	83	A2	
P1.7	115	B10	82	A2	
P1.8	114	A10	81	A2	
P1.9	113	B11	80	A2	
P1.10	106	D12	73	A1+	
P1.11	105	D11	72	A1+	
P1.12	104	E11	71	A2	
P1.13	103	E12	70	A2	
P1.14	102	E10	69	A2	
P1.15	94	G12	68	A2	
P2.0	74	J11	52	A2	
P2.1	73	K12	51	A2	After a system reset, via HWSEL this pin selects the DB.TDO function.
P2.2	72	K11	50	A2	
P2.3	71	L11	49	A2	
P2.4	70	L10	48	A2	
P2.5	69	M10	47	A2	
P2.6	76	J9	54	A1+	
P2.7	75	K9	53	A1+	
P2.8	68	L9	46	A2	
P2.9	67	M9	45	A2	

Table 9 Package Pin Mapping (cont'd)

Function	LQFP-144	LFBGA-144	LQFP-100	Pad Type	Notes
P5.3	81	J10	-	A2	
P5.4	80	K10	-	A2	
P5.5	79	J8	-	A2	
P5.6	78	K8	-	A2	
P5.7	77	J7	55	A1+	
P5.8	58	H6	-	A2	
P5.9	57	K6	-	A2	
P5.10	56	H5	-	A1+	
P5.11	55	J5	-	A1+	
P6.0	101	G10	-	A2	
P6.1	100	F9	-	A2	
P6.2	99	H10	-	A2	
P6.3	98	G9	-	A1+	
P6.4	97	F10	-	A2	
P6.5	96	F11	-	A2	
P6.6	95	F12	-	A2	
P14.0	42	L3	31	AN/DIG_IN	
P14.1	41	L2	30	AN/DIG_IN	
P14.2	40	K3	29	AN/DIG_IN	
P14.3	39	J4	28	AN/DIG_IN	
P14.4	38	K1	27	AN/DIG_IN	
P14.5	37	K2	26	AN/DIG_IN	
P14.6	36	J3	25	AN/DIG_IN	
P14.7	35	J2	24	AN/DIG_IN	
P14.8	52	M5	37	AN/DAC/DIG_IN	
P14.9	51	L5	36	AN/DAC/DIG_IN	
P14.12	34	J1	23	AN/DIG_IN	
P14.13	33	H4	22	AN/DIG_IN	
P14.14	32	H3	21	AN/DIG_IN	
P14.15	31	H2	20	AN/DIG_IN	
P15.2	30	H1	19	AN/DIG_IN	

Table 9 Package Pin Mapping (cont'd)

Function	LQFP-144	LFBGA-144	LQFP-100	Pad Type	Notes
VSSO	89	J12	63	Power	
VSS	Exp. Pad	-	Exp. Pad	Power	**Exposed Die Pad** The exposed die pad is connected internally to VSS. For proper operation, it is mandatory to connect the exposed pad directly to the common ground on the board. For thermal aspects, please refer to the Data Sheet. Board layout examples are given in an application note.

Table 11 Port I/O Functions (cont'd)

Function	Outputs						Inputs									
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P1.5	CAN. N1_TXD	U0C0. DOUT0	CCU80. OUT23	CCU81. OUT10	U0C0. DOUT0		U0C0. HWIN0		U0C0. DX0A	CAN. N0_RXDA	ERU0. 2A0	ERU1. 0A0	CCU41. IN1C	DSD. DIN2B		
P1.6		U0C0. SCLKOUT			SDMMC. DATA1_OUT	EBU. AD10	SDMMC. DATA1_IN	EBU. D10	DSD. DIN2A							
P1.7		U0C0. DOUT0	DSD. MCLK2		SDMMC. DATA2_OUT	EBU. AD11	SDMMC. DATA2_IN	EBU. D11		DSD. MCLK2A						
P1.8		U0C0. SELO1	DSD. MCLK1		SDMMC. DATA4_OUT	EBU. AD12	SDMMC. DATA4_IN	EBU. D12	CAN. N2_RXDA	DSD. MCLK1A						
P1.9		CAN. N2_TXD			SDMMC. DATA5_OUT	EBU. AD13	SDMMC. DATA5_IN	EBU. D13		DSD. MCLK0A						
P1.10	ETH0. MDC	U0C0. SCLKOUT	CCU81. OUT21				SDMMC. SDCD						CCU41. IN2C			
P1.11		U0C0. SELO0	CCU81. OUT11		ETH0. MDO		ETH0. MDIC						CCU41. IN3C			
P1.12	ETH0. TX_EN	CAN. N1_TXD	CCU81. OUT01		SDMMC. DATA6_OUT	EBU. AD16	SDMMC. DATA6_IN	EBU. D16								
P1.13	ETH0. TXD0	U0C1. SELO3	CCU81. OUT20		SDMMC. DATA7_OUT	EBU. AD17	SDMMC. DATA7_IN	EBU. D17	CAN. N1_RXDC							
P1.14	ETH0. TXD1	U0C1. SELO2	CCU81. OUT10			EBU. AD18		EBU. D18								
P1.15	SCU. EXTCLK	DSD. MCLK2	CCU81. OUT00			EBU. AD19		EBU. D19		DSD. MCLK2B		ERU1. 1A0				
P2.0		CCU81. OUT21	DSD. CGPWMN	LEDTS0. COL1	ETH0. MDO	EBU. AD20	ETH0. MDIB	EBU. D20			ERU0. 0B3		CCU40. IN1C			
P2.1		CCU81. OUT11	DSD. CGPWMP	LEDTS0. COL0	DB.TDO/ TRACESWO	EBU. AD21		EBU. D21	ETH0. CLK_RMIIA			ERU1. 0B0	CCU40. IN0C			ETH0. CLKRXA
P2.2	VADC. EMUX00	CCU81. OUT01	CCU41. OUT3	LEDTS0. LINE0	LEDTS0. EXTENDED0	EBU. AD22	LEDTS0. TSIN0A	EBU. D22	ETH0. RXD0A	U0C1. DX0A	ERU0. 1B2		CCU41. IN3A			
P2.3	VADC. EMUX01	U0C1. SELO0	CCU41. OUT2	LEDTS0. LINE1	LEDTS0. EXTENDED1	EBU. AD23	LEDTS0. TSIN1A	EBU. D23	ETH0. RXD1A	U0C1. DX2A	ERU0. 1A2	POSIF1. IN2A	CCU41. IN2A			
P2.4	VADC. EMUX02	U0C1. SCLKOUT	CCU41. OUT1	LEDTS0. LINE2	LEDTS0. EXTENDED2	EBU. AD24	LEDTS0. TSIN2A	EBU. D24	ETH0. RXERA	U0C1. DX1A	ERU0. 0B2	POSIF1. IN1A	CCU41. IN1A			
P2.5	ETH0. TX_EN	U0C1. DOUT0	CCU41. OUT0	LEDTS0. LINE3	LEDTS0. EXTENDED3	EBU. AD25	LEDTS0. TSIN3A	EBU. D25	ETH0. RXDVA	U0C1. DX0B	ERU0. 0A2	POSIF1. IN0A	CCU41. IN0A			ETH0. CRS_DVA
P2.6	U2C0. SELO4		CCU80. OUT13	LEDTS0. COL3	U2C0. DOUT3		U2C0. HWIN3		DSD. DIN1B	CAN. N1_RXDA	ERU0. 1B3		CCU40. IN3C			
P2.7	ETH0. MDC	CAN. N1_TXD	CCU80. OUT03	LEDTS0. COL2					DSD. DIN0B			ERU1. 1B0	CCU40. IN2C			
P2.8	ETH0. TXD0		CCU80. OUT32	LEDTS0. LINE4	LEDTS0. EXTENDED4	EBU. AD26	LEDTS0. TSIN4A	EBU. D26	DAC. TRIGGER5				CCU40. IN0B	CCU40. IN1B	CCU40. IN2B	CCU40. IN3B
P2.9	ETH0. TXD1		CCU80. OUT22	LEDTS0. LINE5	LEDTS0. EXTENDED5	EBU. AD27	LEDTS0. TSIN5A	EBU. D27	DAC. TRIGGER4				CCU41. IN0B	CCU41. IN1B	CCU41. IN2B	CCU41. IN3B
P2.10	VADC. EMUX10				DB. ETM_TRACEDATA3	EBU. AD28		EBU. D28								
P2.11	ETH0. TXER		CCU80. OUT22		DB. ETM_TRACEDATA2	EBU. AD29		EBU. D29								

3 Electrical Parameters

3.1 General Parameters

3.1.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the XMC4500 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with a two-letter abbreviation in column “Symbol”:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics, which are a distinctive feature of the XMC4500 and must be regarded for system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC4500 is designed in.

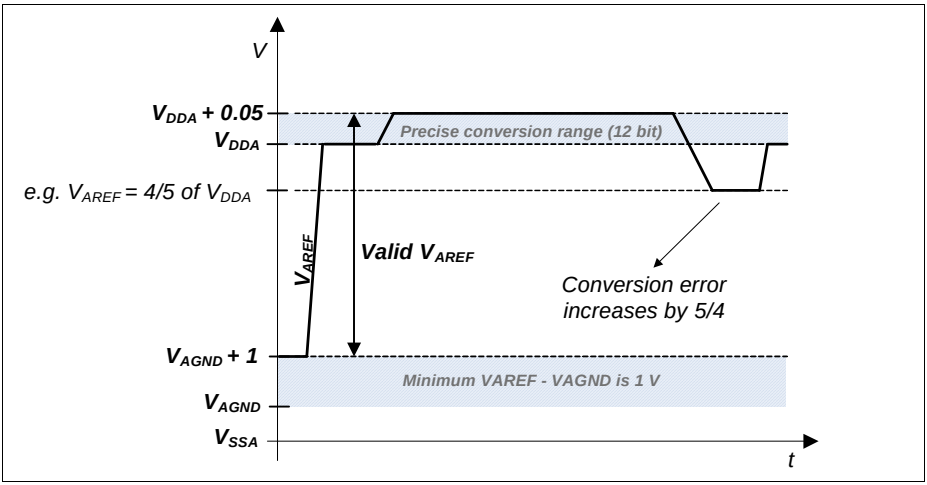

Figure 14 VADC Reference Voltage Range

The power-up calibration of the VADC requires a maximum number of 4 352 f_{ADCI} cycles.

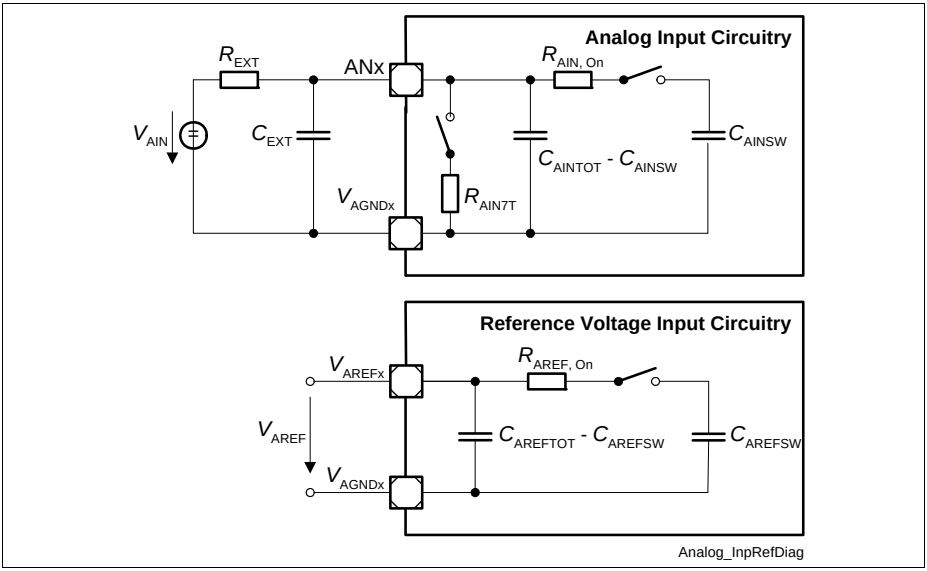

Figure 15 VADC Input Circuits

3.2.6 USB OTG Interface DC Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification and the OTG Specification Rev. 1.3. High-Speed Mode is not supported.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 28 USB OTG VBUS and ID Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VBUS input voltage range	V_{IN} CC	0.0	–	5.25	V	
A-device VBUS valid threshold	V_{B1} CC	4.4	–	–	V	
A-device session valid threshold	V_{B2} CC	0.8	–	2.0	V	
B-device session valid threshold	V_{B3} CC	0.8	–	4.0	V	
B-device session end threshold	V_{B4} CC	0.2	–	0.8	V	
VBUS input resistance to ground	R_{VBUS_IN} CC	40	–	100	kOhm	
B-device VBUS pull-up resistor	R_{VBUS_PU} CC	281	–	–	Ohm	Pull-up voltage = 3.0 V
B-device VBUS pull-down resistor	R_{VBUS_PD} CC	656	–	–	Ohm	
USB.ID pull-up resistor	R_{UID_PU} CC	14	–	25	kOhm	
VBUS input current	I_{VBUS_IN} CC	–	–	150	µA	$0\ V \le V_{IN} \le 5.25\ V$: T_{AVG} = 1 ms

Table 32 Power Supply Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Sleep supply current[4] Peripherals disabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPS}	CC	–	110	–	mA	120 / 120 / 120
			–	100	–		120 / 60 / 60
			–	77	–		60 / 60 / 120
			–	59	–		24 / 24 / 24
			–	48	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz			–	46	–		100 / 100 / 100
Deep Sleep supply current[5] Flash in Sleep mode Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPD}	CC	–	20	–	mA	24 / 24 / 24
			–	12	–		4 / 4 / 4
			–	10	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz			–	6	–		100 / 100 / 100 [6]
Hibernate supply current RTC on[7]	I_{DDPH}	CC	–	10	–	µA	V_{BAT} = 3.3 V
			–	7.5	–		V_{BAT} = 2.4 V
			–	6.2	–		V_{BAT} = 2.0 V
Hibernate supply current RTC off[8]	I_{DDPH}	CC	–	9.2	–	µA	V_{BAT} = 3.3 V
			–	6.7	–		V_{BAT} = 2.4 V
			–	5.6	–		V_{BAT} = 2.0 V
Worst case active supply current[9]	I_{DDPA}	CC	–	–	180 [10]	mA	V_{DDP} = 3.6 V, T_J = 150 °C
V_{DDA} power supply current	I_{DDA}	CC	–	–	–[11]	mA	
I_{DDP} current at $\overline{\text{PORST}}$ Low	I_{DDP_PORST}	CC	–	–	16	mA	V_{DDP} = 3.6 V, T_J = 150 °C
Power Dissipation	P_{DISS}	CC	–	–	1	W	V_{DDP} = 3.6 V, T_J = 150 °C
Wake-up time from Sleep to Active mode	t_{SSA}	CC	–	6	–	cycles	

3.3.9.3 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 45 USIC IIC Standard Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	-	-	1000	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	250	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	4.0	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	4.0	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

With clock delay:

(2)

$$t_{ODLY\_F} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ISU} < t_{WL} + t_{CLK\_DELAY}$$

(3)

$$t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{WL} < t_{PP} + t_{CLK\_DELAY} - t_{ISU} - t_{ODLY\_F}$$

$$t_{DATA\_DELAY} + t_{TAP\_DELAY} + 20 < 40 + t_{CLK\_DELAY} - 5 - 10$$

$$t_{DATA\_DELAY} < 5 + t_{CLK\_DELAY} - t_{TAP\_DELAY}$$

The data can be delayed versus clock up to 5 ns in ideal case of t_{WL}= 20 ns.

Full-Speed Write Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

(4)

$$t_{CLK\_DELAY} < t_{WL} + t_{OH\_F} + t_{DATA\_DELAY} + t_{TAP\_DELAY} - t_{IH}$$

$$t_{CLK\_DELAY} < 20 + t_{DATA\_DELAY} + t_{TAP\_DELAY} - 5$$

$$t_{DATA\_DELAY} < 15 + t_{CLK\_DELAY} + t_{TAP\_DELAY}$$

The clock can be delayed versus data up to 18.2 ns (external delay line) in ideal case of t_{WL}= 20 ns, with maximum t_{TAP_DELAY} = 3.2 ns programmed.

Full-Speed Input Path (Read)

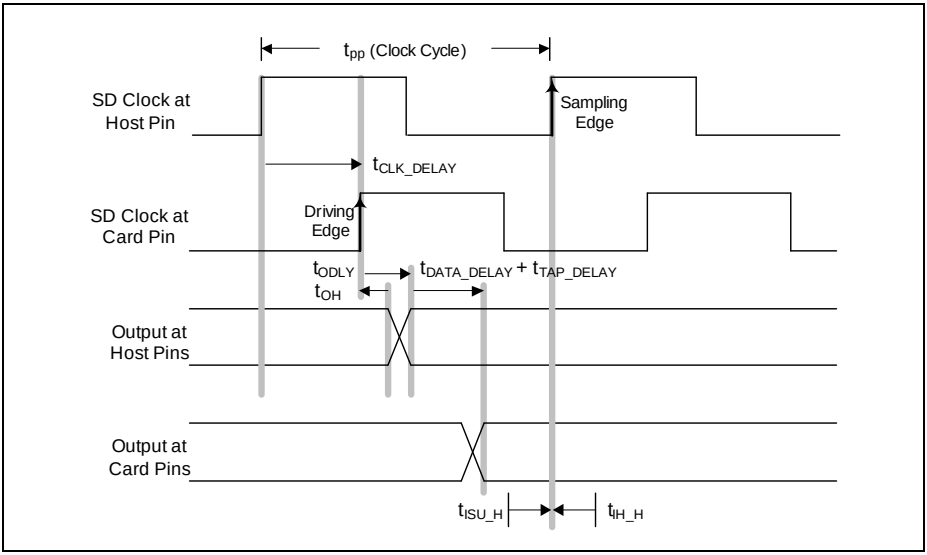

Figure 38 Full-Speed Input Path

Full-Speed Read Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

(5)

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ODLY} + t_{ISU\_F} < 0{,}5 \times t_{pp}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < 0{,}5 \times t_{pp} - t_{ODLY} - t_{ISU\_F} - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < 20 - 14 - 2 - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < 4 - t_{TAP\_DELAY}$$

The data + clock delay can be up to 4 ns for a 40 ns clock cycle.

Full-Speed Read Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

(6)

$$t_{CLK\_DELAY} + t_{OH} + t_{DATA\_DELAY} + t_{TAP\_DELAY} > t_{IH\_F}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} > t_{IH\_F} - t_{OH} - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} > 2 - t_{TAP\_DELAY}$$

The data + clock delay must be greater than 2 ns if t_{TAP_DELAY} is not used.

If the t_{TAP_DELAY} is programmed to at least 2 ns, the data + clock delay must be greater than 0 ns (or less). This is always fulfilled.

AC Timing Specifications (High-Speed Mode)

Table 51 SDMMC Timing for High-Speed Mode

Parameter	Symbol		Values		Unit	Note/ Test Condition
			Min.	Max.		
Clock frequency in high speed transfer mode ($1/t_{pp}$)	f_{pp}	CC	0	48	MHz	
Clock cycle in high speed transfer mode	t_{pp}	CC	20	–	ns	
Clock low time	t_{WL}	CC	7	–	ns	
Clock high time	t_{WH}	CC	7	–	ns	
Clock rise time	t_{TLH}	CC	–	3	ns	
Clock fall time	t_{THL}	CC	–	3	ns	
Inputs setup to clock rising edge	t_{ISU_H}	SR	2	–	ns	
Inputs hold after clock rising edge	t_{IH_H}	SR	2	–	ns	
Outputs valid time in high speed mode	t_{ODLY_H}	CC	–	14	ns	
Outputs hold time in high speed mode	t_{OH_H}	CC	2	–	ns	

Table 52 SD Card Bus Timing for High-Speed Mode[1)]

Parameter	Symbol	Values		Unit	Note/ Test Condition
		Min.	Max.		
SD card input setup time	t_{ISU}	6	–	ns	
SD card input hold time	t_{IH}	2	–	ns	
SD card output valid time	t_{ODLY}	–	14	ns	
SD card output hold time	t_{OH}	2.5	–	ns	

1) Reference card timing values for calculation examples. Not subject to production test and not characterized.

High-Speed Output Path (Write)

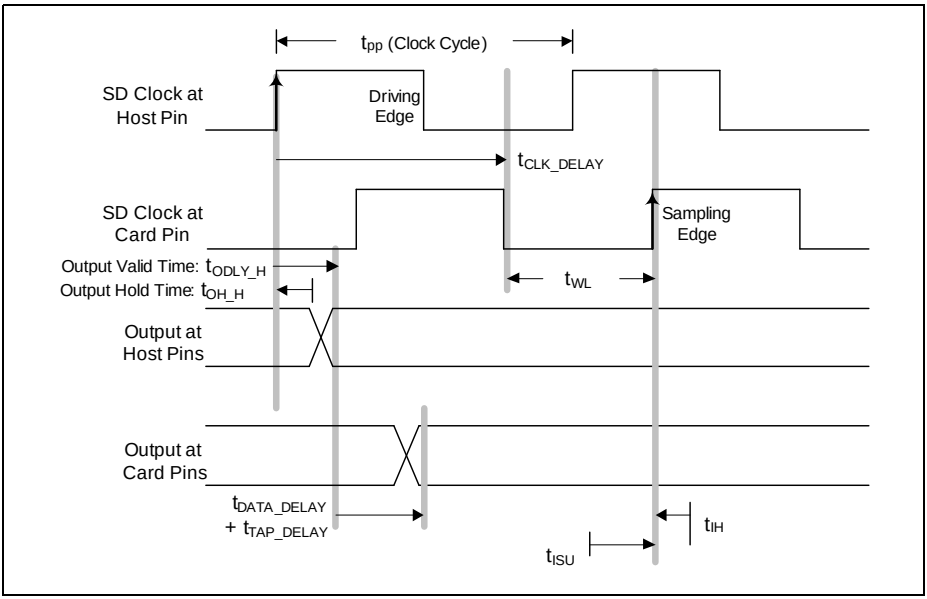

Figure 39 High-Speed Output Path

High-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

Multiplexed Write Timing

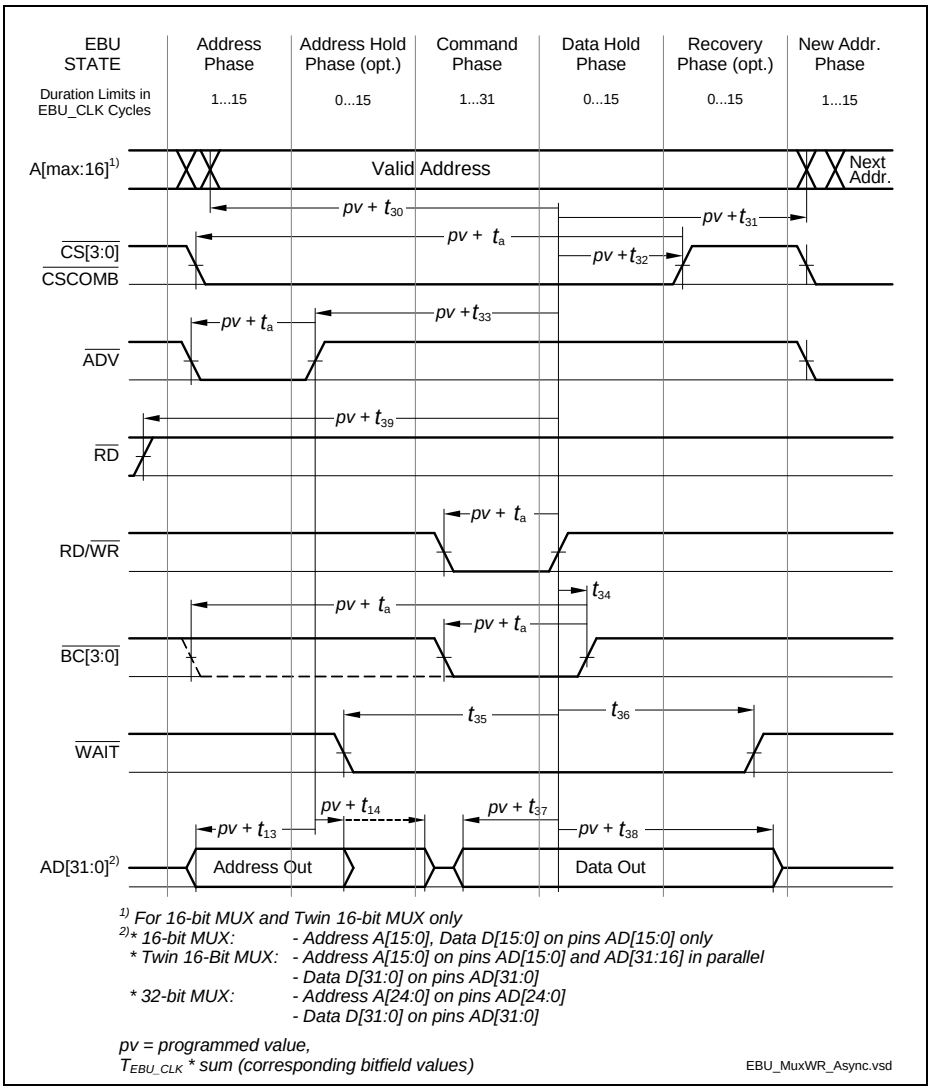

Figure 43 Multiplexed Write Access

3.3.12.2 ETH Management Signal Parameters (ETH_MDC, ETH_MDIO)

Table 61 ETH Management Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
ETH_MDC period	t_1	CC	400	–	–	ns	C_L = 25 pF
ETH_MDC high time	t_2	CC	160	–	–	ns	
ETH_MDC low time	t_3	CC	160	–	–	ns	
ETH_MDIO setup time (output)	t_4	CC	10	–	–	ns	
ETH_MDIO hold time (output)	t_5	CC	10	–	–	ns	
ETH_MDIO data valid (input)	t_6	SR	0	–	300	ns	

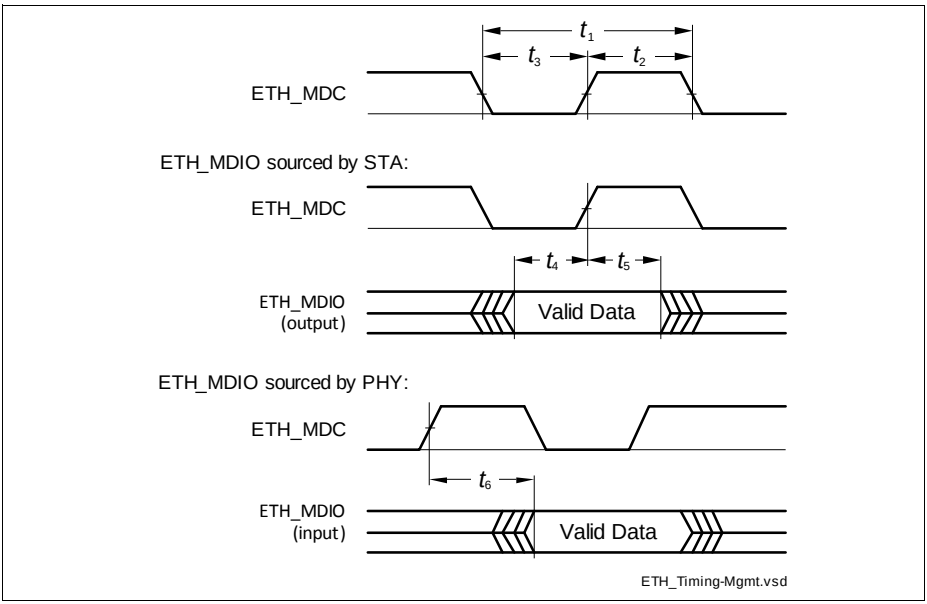

Figure 52 ETH Management Signal Timing