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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, LED, POR, PWM, WDT
Number of I/O	91
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	PG-LQFP-144-10
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4504f144f512acxqma1

Input/Output Lines

- Programmable port driver control module (PORTS)
- Individual bit addressability
- Tri-stated in input mode
- Push/pull or open drain output mode
- Boundary scan test support over JTAG interface

On-Chip Debug Support

- Full support for debug features: 8 breakpoints, CoreSight, trace
- Various interfaces: ARM-JTAG, SWD, single wire trace

1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code “XMC4<DDD>-<Z><PPP><T><FFFF>” identifies:

- <DDD> the derivatives function set
- <Z> the package variant
  – E: LFBGA
  – F: LQFP
  – Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
  – F: -40°C to 85°C
  – X: -40°C to 105°C
  – K: -40°C to 125°C
- <FFFF> the Flash memory size.

For ordering codes for the XMC4500 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC4500 series, some descriptions may not apply to a specific product.

For simplicity the term **XMC4500** is used for all derivatives throughout this document.

Table 9 Package Pin Mapping (cont'd)

Function	LQFP-144	LFBGA-144	LQFP-100	Pad Type	Notes
P15.3	29	G2	18	AN/DIG_IN	
P15.4	28	G4	-	AN/DIG_IN	
P15.5	27	G3	-	AN/DIG_IN	
P15.6	26	G5	-	AN/DIG_IN	
P15.7	25	G6	-	AN/DIG_IN	
P15.8	54	M6	39	AN/DIG_IN	
P15.9	53	L6	38	AN/DIG_IN	
P15.12	50	K5	-	AN/DIG_IN	
P15.13	49	M4	-	AN/DIG_IN	
P15.14	44	L4	-	AN/DIG_IN	
P15.15	43	K4	-	AN/DIG_IN	
USB_DP	16	E1	9	special	
USB_DM	15	D1	8	special	
HIB_IO_0	21	F4	14	A1 special	At the first power-up and with every reset of the hibernate domain this pin is configured as open-drain output and drives "0". As output the medium driver mode is active.
HIB_IO_1	20	F3	13	A1 special	At the first power-up and with every reset of the hibernate domain this pin is configured as input with no pull device active. As output the medium driver mode is active.
TCK	93	G8	67	A1	Weak pull-down active.
TMS	92	G7	66	A1+	Weak pull-up active. As output the strong-soft driver mode is active.
$\overline{\text{PORST}}$	91	G11	65	special	Weak pull-up permanently active, strong pull-down controlled by EVR.
XTAL1	87	H11	61	clock_IN	
XTAL2	88	H12	62	clock_O	

2.2.2.1 Port I/O Function Table

Table 11 Port I/O Functions

Function	Outputs						Inputs									
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P0.0		CAN.N0_TXD	CCU80.OUT21	LEDTS0.COL2					U1C1.DX0D	ETH0.CLK_RMIIB	ERU0.0B0					ETH0.CLKRXB
P0.1	USB.DRIVEVBUS	U1C1.DOUT0	CCU80.OUT11	LEDTS0.COL3						ETH0.CRS_DVB	ERU0.0A0					ETH0.RXDVB
P0.2		U1C1.SELO1	CCU80.OUT01		U1C0.DOUT3	EBU.AD0	U1C0.HWIN3	EBU.D0	ETH0.RXD0B		ERU0.3B3					
P0.3			CCU80.OUT20		U1C0.DOUT2	EBU.AD1	U1C0.HWIN2	EBU.D1	ETH0.RXD1B			ERU1.3B0				
P0.4	ETH0.TX_EN		CCU80.OUT10		U1C0.DOUT1	EBU.AD2	U1C0.HWIN1	EBU.D2		U1C0.DX0A	ERU0.2B3					
P0.5	ETH0.TXD0	U1C0.DOUT0	CCU80.OUT00		U1C0.DOUT0	EBU.AD3	U1C0.HWIN0	EBU.D3		U1C0.DX0B		ERU1.3A0				
P0.6	ETH0.TXD1	U1C0.SELO0	CCU80.OUT30			EBU.$\overline{\text{ADV}}$				U1C0.DX2A	ERU0.3B2		CCU80.IN2B			
P0.7	WWDT.SERVICE_OUT	U0C0.SELO0				EBU.AD6	DB.TDI	EBU.D6	U0C0.DX2B	DSD.DIN1A	ERU0.2B1		CCU80.IN0A	CCU80.IN1A	CCU80.IN2A	CCU80.IN3A
P0.8	SCU.EXTCLK	U0C0.SCLKOUT				EBU.AD7	DB.$\overline{\text{TRST}}$	EBU.D7	U0C0.DX1B	DSD.DIN0A	ERU0.2A1		CCU80.IN1B			
P0.9		U1C1.SELO0	CCU80.OUT12	LEDTS0.COL0	ETH0.MDO	EBU.$\overline{\text{CS1}}$	ETH0.MDIA		U1C1.DX2A	USB.ID	ERU0.1B0					
P0.10	ETH0.MDC	U1C1.SCLKOUT	CCU80.OUT02	LEDTS0.COL1					U1C1.DX1A		ERU0.1A0					
P0.11		U1C0.SCLKOUT	CCU80.OUT31		SDMMC.$\overline{\text{RST}}$	EBU.$\overline{\text{BREQ}}$			ETH0.RXERB	U1C0.DX1A	ERU0.3A2					
P0.12		U1C1.SELO0	CCU40.OUT3			EBU.$\overline{\text{HLDA}}$		EBU.$\overline{\text{HLDA}}$		U1C1.DX2B	ERU0.2B2					
P0.13		U1C1.SCLKOUT	CCU40.OUT2							U1C1.DX1B	ERU0.2A2					
P0.14		U1C0.SELO1	CCU40.OUT1		U1C1.DOUT3		U1C1.HWIN3						CCU42.IN3C			
P0.15		U1C0.SELO2	CCU40.OUT0		U1C1.DOUT2		U1C1.HWIN2						CCU42.IN2C			
P1.0	DSD.CGPWMN	U0C0.SELO0	CCU40.OUT3	ERU1.PDOUT3					U0C0.DX2A		ERU0.3B0		CCU40.IN3A			
P1.1	DSD.CGPWMP	U0C0.SCLKOUT	CCU40.OUT2	ERU1.PDOUT2			SDMMC.SDWC		U0C0.DX1A	POSIF0.IN2A	ERU0.3A0		CCU40.IN2A			
P1.2			CCU40.OUT1	ERU1.PDOUT1	U0C0.DOUT3	EBU.AD14	U0C0.HWIN3	EBU.D14		POSIF0.IN1A		ERU1.2B0	CCU40.IN1A			
P1.3		U0C0.MCLKOUT	CCU40.OUT0	ERU1.PDOUT0	U0C0.DOUT2	EBU.AD15	U0C0.HWIN2	EBU.D15		POSIF0.IN0A		ERU1.2A0	CCU40.IN0A			
P1.4	WWDT.SERVICE_OUT	CAN.N0_TXD	CCU80.OUT33	CCU81.OUT20	U0C0.DOUT1		U0C0.HWIN1		U0C0.DX0B	CAN.N1_RXDD	ERU0.2B0		CCU41.IN0C			

Table 11 Port I/O Functions (cont'd)

Function	Outputs						Inputs									
	ALT1	**ALT2**	**ALT3**	**ALT4**	**HWO0**	**HWO1**	**HWI0**	**HWI1**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**
P6.6			DSD.MCLK3		DB.ETM_TRACEDATA0	EBU.$\overline{\text{BC3}}$			DSD.MCLK3A	ETH0.CLK_TXB						
P14.0									VADC.G0CH0							
P14.1									VADC.G0CH1							
P14.2									VADC.G0CH2	VADC.G1CH2						
P14.3									VADC.G0CH3	VADC.G1CH3			CAN.N0_RXDB			
P14.4									VADC.G0CH4		VADC.G2CH0					
P14.5									VADC.G0CH5		VADC.G2CH1		POSIF0.IN2B			
P14.6									VADC.G0CH6				POSIF0.IN1B		G0ORC6	
P14.7									VADC.G0CH7				POSIF0.IN0B		G0ORC7	
P14.8					DAC.OUT_0					VADC.G1CH0		VADC.G3CH2	ETH0.RXD0C			
P14.9					DAC.OUT_1					VADC.G1CH1		VADC.G3CH3	ETH0.RXD1C			
P14.12										VADC.G1CH4						
P14.13										VADC.G1CH5						
P14.14										VADC.G1CH6					G1ORC6	
P14.15										VADC.G1CH7					G1ORC7	
P15.2											VADC.G2CH2					
P15.3											VADC.G2CH3					
P15.4											VADC.G2CH4					
P15.5											VADC.G2CH5					
P15.6											VADC.G2CH6					
P15.7											VADC.G2CH7					
P15.8												VADC.G3CH0	ETH0.CLK_RMIIC			ETH0.CLKRXC
P15.9												VADC.G3CH1	ETH0.CRS_DVC			ETH0.RXDVC

Table 13 Overload Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current on any port pin during overload condition	I_{OV} SR	-5	–	5	mA	
Absolute sum of all input circuit currents for one port group during overload condition[1]	I_{OVG} SR	–	–	20	mA	$\Sigma\lvert I_{OVx}\rvert$, for all $I_{OVx} < 0$ mA
		–	–	20	mA	$\Sigma\lvert I_{OVx}\rvert$, for all $I_{OVx} > 0$ mA
Absolute sum of all input circuit currents during overload condition	I_{OVS} SR	–	–	80	mA	ΣI_{OVG}

1) The port groups are defined in **Table 16**.

Figure 11 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DDP} and ground are a simplified representation of these ESD protection structures.

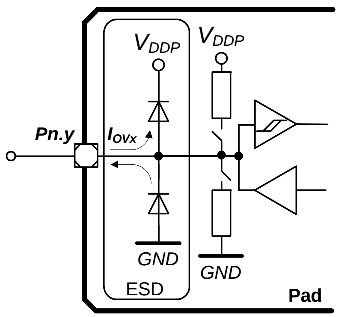

Figure 11 Input Overload Current via ESD structures

Table 14 and **Table 15** list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the **Absolute Maximum Ratings** must not be exceeded during overload.

3.1.5 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC4500. All parameters specified in the following sections refer to these operating conditions, unless noted otherwise.

Table 18 Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ambient Temperature	T_A SR	-40	–	85	°C	Temp. Range F
		-40	–	105	°C	Temp. Range X
		-40	–	125	°C	Temp. Range K
Digital supply voltage	V_{DDP} SR	3.13[1)]	3.3	3.63 [2)]	V	
Core Supply Voltage	V_{DDC} CC	–[1)]	1.3	–	V	Generated internally
Digital ground voltage	V_{SS} SR	0	–	–	V	
Analog supply voltage	V_{DDA} SR	3.0	3.3	3.6[2)]	V	
Analog ground voltage for V_{DDA}	V_{SSA} SR	-0.1	0	0.1	V	
Battery Supply Voltage for Hibernate Domain	V_{BAT} SR	1.95[3)]	–	3.63	V	When V_{DDP} is supplied V_{BAT} has to be supplied as well.
System Frequency	f_{SYS} SR	–	–	120	MHz	
Short circuit current of digital outputs	I_{SC} SR	-5	–	5	mA	
Absolute sum of short circuit currents per pin group[4)]	ΣI_{SC_PG} SR	–	–	20	mA	
Absolute sum of short circuit currents of the device	ΣI_{SC_D} SR	–	–	100	mA	

1) See also the Supply Monitoring thresholds, **Section 3.3.2**.

2) Voltage overshoot to 4.0 V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h over lifetime.

3) To start the hibernate domain it is required that $V_{BAT} \geq 2.1$ V, for a reliable start of the oscillation of RTC_XTAL in crystal mode it is required that $V_{BAT} \geq 3.0$ V.

4) The port groups are defined in **Table 16**.

Table 21 Standard Pads Class_A1+

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Output high voltage, POD[1] = weak	V_{OHA1+} CC	V_{DDP} - 0.4		–	V	$I_{OH} \geq$ -400 µA
		2.4		–	V	$I_{OH} \geq$ -500 µA
Output high voltage, POD[1] = medium		V_{DDP} - 0.4		–	V	$I_{OH} \geq$ -1.4 mA
		2.4		–	V	$I_{OH} \geq$ -2 mA
Output high voltage, POD[1] = strong		V_{DDP} - 0.4		–	V	$I_{OH} \geq$ -1.4 mA
		2.4		–	V	$I_{OH} \geq$ -2 mA
Output low voltage	V_{OLA1+} CC	–		0.4	V	$I_{OL} \leq$ 500 µA; POD[1] = weak
		–		0.4	V	$I_{OL} \leq$ 2 mA; POD[1] = medium
		–		0.4	V	$I_{OL} \leq$ 2 mA; POD[1] = strong
Fall time	t_{FA1+} CC	–		150	ns	C_L = 20 pF; POD[1] = weak
		–		50	ns	C_L = 50 pF; POD[1] = medium
		–		28	ns	C_L = 50 pF; POD[1] = strong; edge = slow
		–		16	ns	C_L = 50 pF; POD[1] = strong; edge = soft;
Rise time	t_{RA1+} CC	–		150	ns	C_L = 20 pF; POD[1] = weak
		–		50	ns	C_L = 50 pF; POD[1] = medium
		–		28	ns	C_L = 50 pF; POD[1] = strong; edge = slow
		–		16	ns	C_L = 50 pF; POD[1] = strong; edge = soft

1) POD = Pin Out Driver

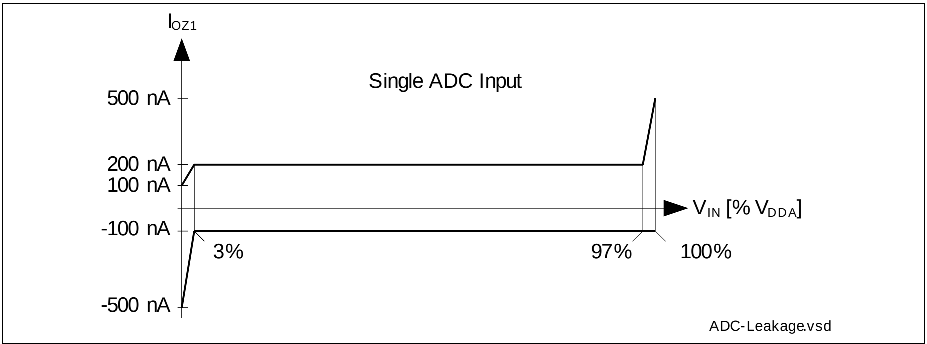

Figure 16 VADC Analog Input Leakage Current

Conversion Time

Table 24 Conversion Time (Operating Conditions apply)

Parameter	Symbol		Values	Unit	Note
Conversion time	t_C	CC	$2 \times T_{ADC}$ + (2 + N + STC + PC +DM) $\times$ T_{ADCI}	µs	N = 8, 10, 12 for N-bit conversion $T_{ADC} = 1 / f_{PERIPH}$ $T_{ADCI} = 1 / f_{ADCI}$

- STC defines additional clock cycles to extend the sample time
- PC adds two cycles if post-calibration is enabled
- DM adds one cycle for an extended conversion time of the MSB

Conversion Time Examples

System assumptions:
f_{ADC} = 120 MHz i.e. t_{ADC} = 8.33 ns, DIVA = 3, f_{ADCI} = 30 MHz i.e. t_{ADCI} = 33.3 ns

According to the given formulas the following minimum conversion times can be achieved (STC = 0, DM = 0):

12-bit post-calibrated conversion (PC = 2):
$t_{CN12C} = (2 + 12 + 2) \times t_{ADCI} + 2 \times t_{ADC} = 16 \times 33.3\ \text{ns} + 2 \times 8.33\ \text{ns} = 550\ \text{ns}$

12-bit uncalibrated conversion:
$t_{CN12} = (2 + 12) \times t_{ADCI} + 2 \times t_{ADC} = 14 \times 33.3\ \text{ns} + 2 \times 8.33\ \text{ns} = 483\ \text{ns}$

10-bit uncalibrated conversion:
$t_{CN10} = (2 + 10) \times t_{ADCI} + 2 \times t_{ADC} = 12 \times 33.3\ \text{ns} + 2 \times 8.33\ \text{ns} = 417\ \text{ns}$

8-bit uncalibrated:
$t_{CN8} = (2 + 8) \times t_{ADCI} + 2 \times t_{ADC} = 10 \times 33.3\ \text{ns} + 2 \times 8.33\ \text{ns} = 350\ \text{ns}$

Table 29 USB OTG Data Line (USB_DP, USB_DM) Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Input low voltage	V_{IL}	SR	–	–	0.8	V	
Input high voltage (driven)	V_{IH}	SR	2.0	–	–	V	
Input high voltage (floating) [1]	V_{IHZ}	SR	2.7	–	3.6	V	
Differential input sensitivity	V_{DIS}	CC	0.2	–	–	V	
Differential common mode range	V_{CM}	CC	0.8	–	2.5	V	
Output low voltage	V_{OL}	CC	0.0	–	0.3	V	1.5 kOhm pull-up to 3.6 V
Output high voltage	V_{OH}	CC	2.8	–	3.6	V	15 kOhm pull-down to 0 V
DP pull-up resistor (idle bus)	R_{PUI}	CC	900	–	1 575	Ohm	
DP pull-up resistor (upstream port receiving)	R_{PUA}	CC	1 425	–	3 090	Ohm	
DP, DM pull-down resistor	R_{PD}	CC	14.25	–	24.8	kOhm	
Input impedance DP, DM	Z_{INP}	CC	300	–	–	kOhm	$0\ V \leq V_{IN} \leq V_{DDP}$
Driver output resistance DP, DM	Z_{DRV}	CC	28	–	44	Ohm	

1) Measured at A-connector with 1.5 kOhm ± 5% to 3.3 V ± 0.3 V connected to USB_DP or USB_DM and at B-connector with 15 kOhm ± 5% to ground connected to USB_DP and USB_DM.

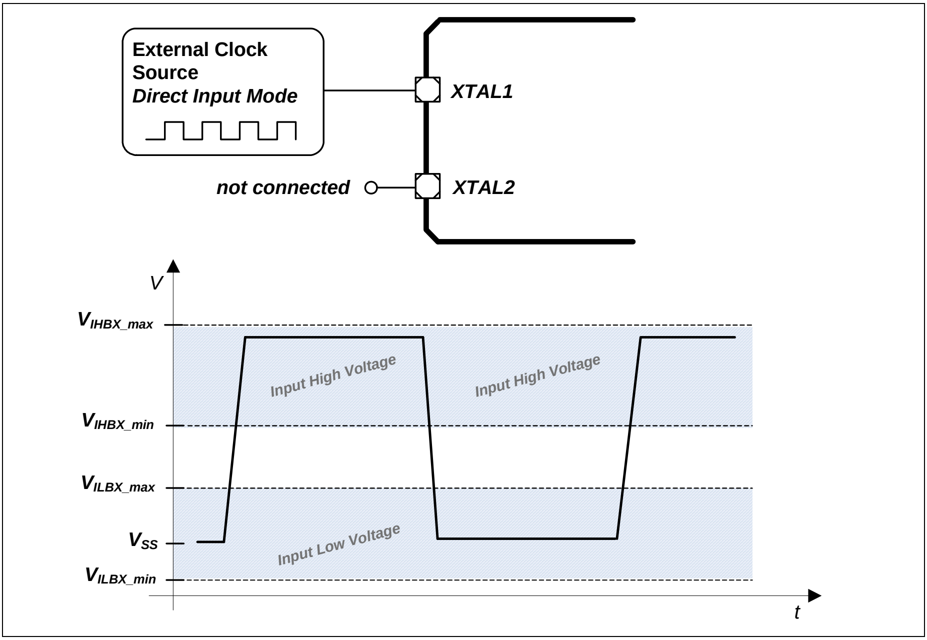

Figure 21 Oscillator in Direct Input Mode

Table 32 Power Supply Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sleep supply current[4)] Peripherals disabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPS} CC	–	110	–	mA	120 / 120 / 120
		–	100	–		120 / 60 / 60
		–	77	–		60 / 60 / 120
		–	59	–		24 / 24 / 24
		–	48	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	46	–		100 / 100 / 100
Deep Sleep supply current[5)] Flash in Sleep mode Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPD} CC	–	20	–	mA	24 / 24 / 24
		–	12	–		4 / 4 / 4
		–	10	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	6	–		100 / 100 / 100 [6)]
Hibernate supply current RTC on[7)]	I_{DDPH} CC	–	10	–	µA	V_{BAT} = 3.3 V
		–	7.5	–		V_{BAT} = 2.4 V
		–	6.2	–		V_{BAT} = 2.0 V
Hibernate supply current RTC off[8)]	I_{DDPH} CC	–	9.2	–	µA	V_{BAT} = 3.3 V
		–	6.7	–		V_{BAT} = 2.4 V
		–	5.6	–		V_{BAT} = 2.0 V
Worst case active supply current[9)]	I_{DDPA} CC	–	–	180 [10)]	mA	V_{DDP} = 3.6 V, T_J = 150 °C
V_{DDA} power supply current	I_{DDA} CC	–	–	–[11)]	mA	
I_{DDP} current at $\overline{\text{PORST}}$ Low	I_{DDP_PORST} CC	–	–	16	mA	V_{DDP} = 3.6 V, T_J = 150 °C
Power Dissipation	P_{DISS} CC	–	–	1	W	V_{DDP} = 3.6 V, T_J = 150 °C
Wake-up time from Sleep to Active mode	t_{SSA} CC	–	6	–	cycles	

3.2.9 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 33 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Erase Time per 256 Kbyte Sector	t_{ERP} CC	–	5	5.5	s	
Erase Time per 64 Kbyte Sector	t_{ERP} CC	–	1.2	1.4	s	
Erase Time per 16 Kbyte Logical Sector	t_{ERP} CC	–	0.3	0.4	s	
Program time per page[1]	t_{PRP} CC	–	5.5	11	ms	
Erase suspend delay	t_{FL_ErSusp} CC	–	–	15	ms	
Wait time after margin change	$t_{FL\_MarginDel}$ CC	10	–	–	µs	
Wake-up time	t_{WU} CC	–	–	270	µs	
Read access time	t_a CC	22	–	–	ns	For operation with $1 / f_{CPU} < t_a$ wait states must be configured[2]
Data Retention Time, Physical Sector[3)4)]	t_{RET} CC	20	–	–	years	Max. 1000 erase/program cycles
Data Retention Time, Logical Sector[3)4)]	t_{RETL} CC	20	–	–	years	Max. 100 erase/program cycles
Data Retention Time, User Configuration Block (UCB)[3)4)]	t_{RTU} CC	20	–	–	years	Max. 4 erase/program cycles per UCB

1) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes an additional time of 5.5 ms.

2) The following formula applies to the wait state configuration: FCON.WSPFLASH $\times$ $(1 / f_{CPU}) \geq t_a$.

3) Storage and inactive time included.

4) Values given are valid for an average weighted junction temperature of T_J = 110°C.

Table 35 Power Sequencing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Positive Load Step Current	ΔI_{PLS} SR	-	–	50	mA	Load increase on V_{DDP} $\Delta t \leq 10$ ns
Negative Load Step Current	ΔI_{NLS} SR	-	–	150	mA	Load decrease on V_{DDP} $\Delta t \leq 10$ ns
V_{DDC} Voltage Over- / Undershoot from Load Step	ΔV_{LS} CC	-	–	±100	mV	For maximum positive or negative load step
Positive Load Step Settling Time	t_{PLSS} SR	50	–	-	µs	
Negative Load Step Settling Time	t_{NLSS} SR	100	–	-	µs	
External Buffer Capacitor on V_{DDC}	C_{EXT} SR	-	10	-	µF	In addition C = 100 nF capacitor on each V_{DDC} pin

Positive Load Step Examples

System assumptions:
$f_{CPU} = f_{SYS}$, target frequency f_{CPU} = 120 MHz, main PLL f_{VCO} = 480 MHz, stepping done by K2 divider, t_{PLSS} between individual steps:

24 MHz - 48 MHz - 68 MHz - 96 MHz - 120 MHz (K2 steps 20 - 10 - 7 - 5 - 4)
24 MHz - 68 MHz - 96 MHz - 120 MHz (K2 steps 20 - 7 - 5 - 4)
24 MHz - 68 MHz - 120 MHz (K2 steps 20 - 7 - 4)

3.3.6 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply.

Table 39 JTAG Interface Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
TCK clock period	t_1	SR	25	–	–	ns	
TCK high time	t_2	SR	10	–	–	ns	
TCK low time	t_3	SR	10	–	–	ns	
TCK clock rise time	t_4	SR	–	–	4	ns	
TCK clock fall time	t_5	SR	–	–	4	ns	
TDI/TMS setup to TCK rising edge	t_6	SR	6	–	–	ns	
TDI/TMS hold after TCK rising edge	t_7	SR	6	–	–	ns	
TDO valid after TCK falling edge[1] (propagation delay)	t_8	CC	–	–	13	ns	C_L = 50 pF
			3	–	–	ns	C_L = 20 pF
TDO hold after TCK falling edge[1]	t_{18}	CC	2	–	–	ns	
TDO high imped. to valid from TCK falling edge[1)2]	t_9	CC	–	–	14	ns	C_L = 50 pF
TDO valid to high imped. from TCK falling edge[1]	t_{10}	CC	–	–	13.5	ns	C_L = 50 pF

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

3.3.7 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply.

Table 40 SWD Interface Timing Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
SWDCLK clock period	t_{SC}	SR	25	–	–	ns	C_L = 30 pF
			40	–	–	ns	C_L = 50 pF
SWDCLK high time	t_1	SR	10	–	500000	ns	
SWDCLK low time	t_2	SR	10	–	500000	ns	
SWDIO input setup to SWDCLK rising edge	t_3	SR	6	–	–	ns	
SWDIO input hold after SWDCLK rising edge	t_4	SR	6	–	–	ns	
SWDIO output valid time after SWDCLK rising edge	t_5	CC	–	–	17	ns	C_L = 50 pF
			–	–	13	ns	C_L = 30 pF
SWDIO output hold time from SWDCLK rising edge	t_6	CC	3	–	–	ns	

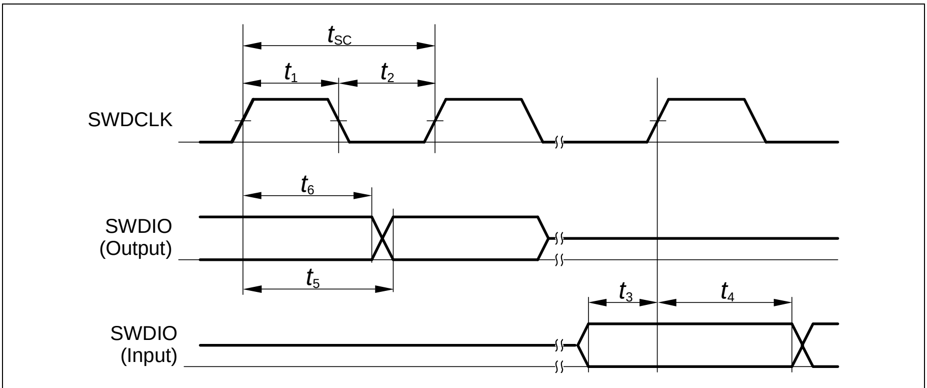

Figure 29 SWD Timing

3.3.8 Embedded Trace Macro Cell (ETM) Timing

The data timing refers to the active clock edge. The XMC4500 ETM uses the half-rate clocking mode. In this mode both, the rising and falling clock edges are active clock edges.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply, with $C_L \leq 15$ pF.

Table 41 ETM Interface Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
TRACECLK period	t_1	CC	16.7	–	–	ns	–
TRACECLK high time	t_2	CC	2	–	–	ns	–
TRACECLK low time	t_3	CC	2	–	–	ns	–
TRACECLK and TRACEDATA rise time	t_4	CC	–	–	3	ns	–
TRACECLK and TRACEDATA fall time	t_5	CC	–	–	3	ns	–
TRACEDATA output valid time	t_6	CC	-2	–	3	ns	–

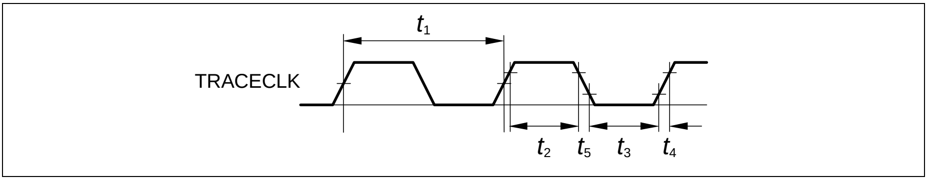

Figure 30 ETM Clock Timing

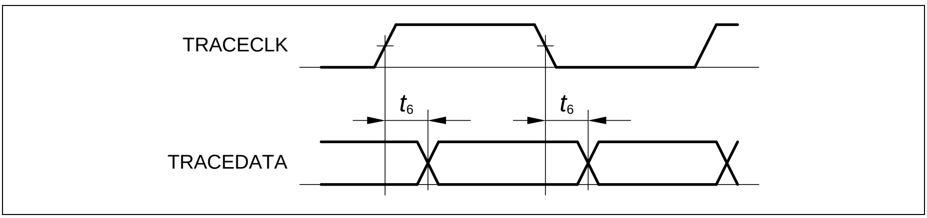

Figure 31 ETM Data Timing

3.3.10.3 EBU Arbitration Signal Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 57 EBU Arbitration Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Output delay from BFCLKO rising edge	t_1	CC	–	–	16	ns	C_L = 50 pF
Data setup to BFCLKO falling edge	t_2	SR	11	–	–	ns	–
Data hold from BFCLKO falling edge	t_3	SR	2	–	–	ns	–

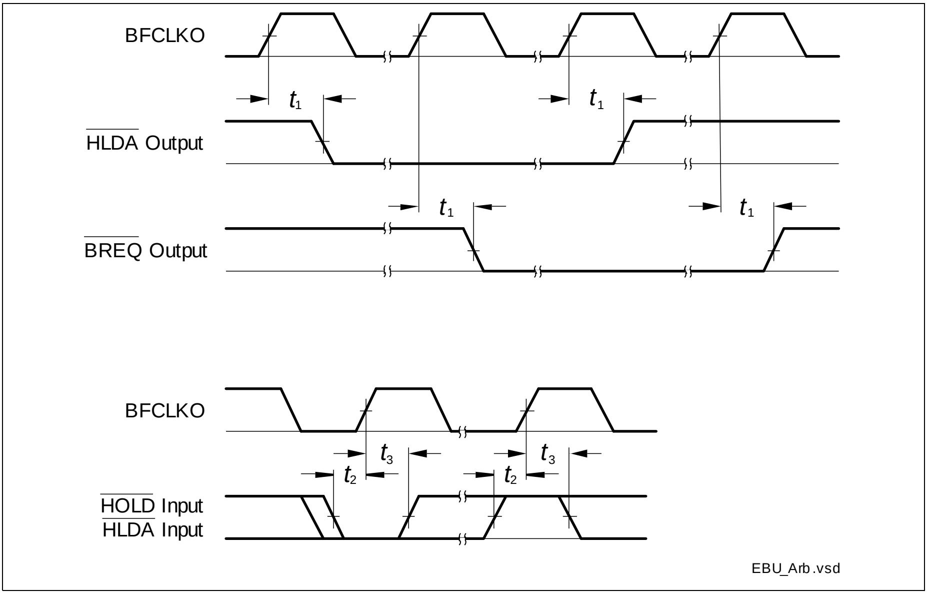

Figure 46 EBU Arbitration Signal Timing

3.3.10.4 EBU SDRAM Access Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply, with Class A2 pins and C_L = 16 pF.

Table 58 EBU SDRAM Access SDCLKO Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Con dition
			Min.	Typ.	Max.		
SDCLKO period	t_1	CC	12.5	–	–	ns	–
SDCLKO high time	t_2	SR	5.5	–	–	ns	–
SDCLKO low time	t_3	SR	3.75	–	–	ns	–
SDCLKO rise time	t_4	SR	–	–	3.0	ns	–
SDCLKO fall time	t_5	SR	–	–	3.0	ns	–

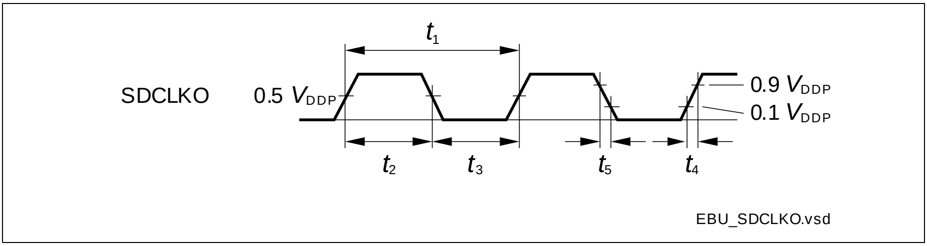

Figure 47 EBU SDRAM Access CLKOUT Timing

3.3.12 Ethernet Interface (ETH) Characteristics

For proper operation of the Ethernet Interface it is required that $f_{SYS} \geq 100$ MHz.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.3.12.1 ETH Measurement Reference Points

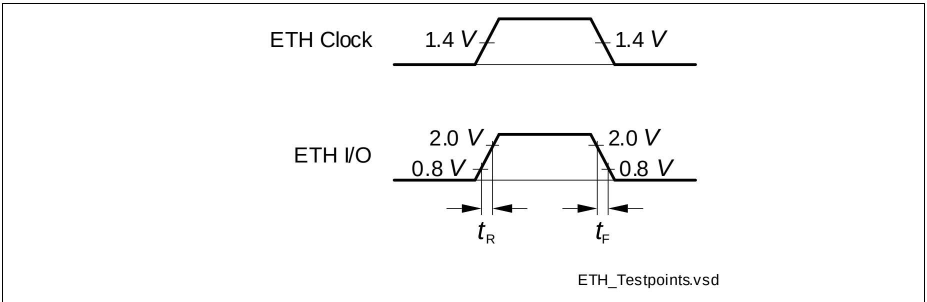

Figure 51 ETH Measurement Reference Points

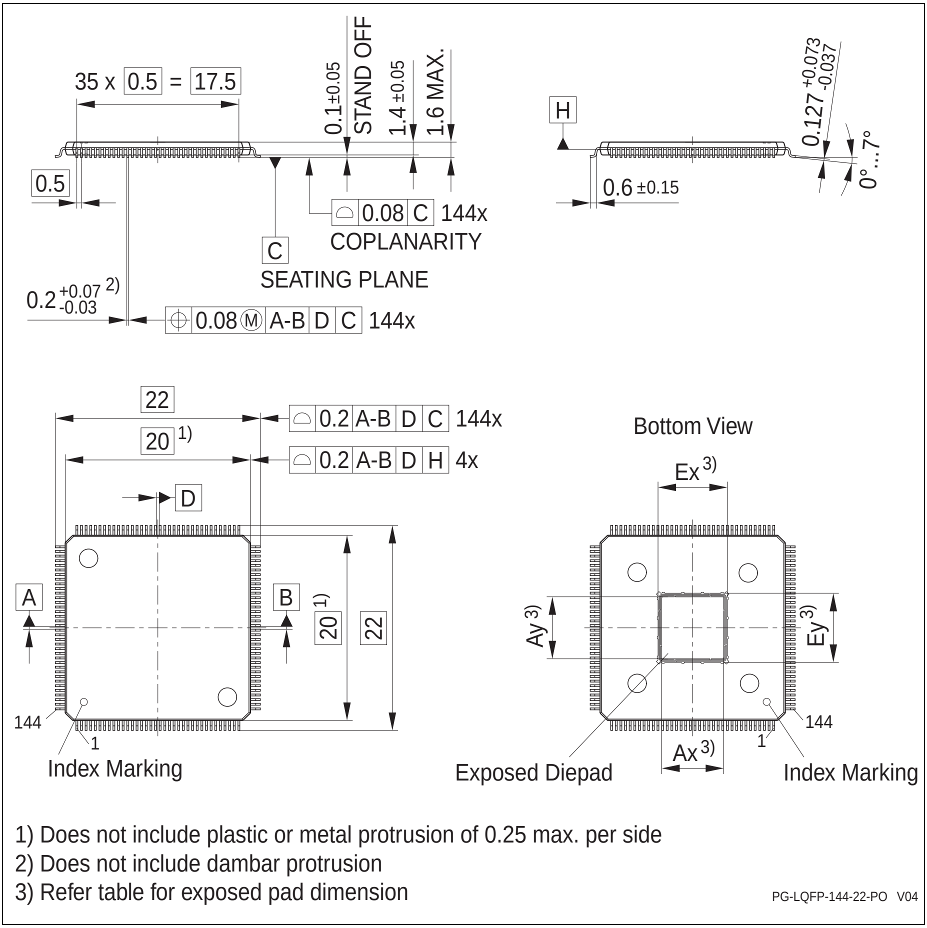

Figure 56 **PG-LQFP-144-24** (Plastic Green Low Profile Quad Flat Package)