What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Discontinued at Digi-Key
Core Processor	8051
Core Size	8-Bit
Speed	48 MIPS
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	40
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.25V
Data Converters	A/D 32x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f388-gqr

C8051F388/9/A/B

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Figure 1.2. C8051F389/B Block Diagram

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Table 5.7. Internal High-Frequency Oscillator Electrical Characteristics

V_{DD} = 2.7 to 3.6 V; T_A = –40 to +85 °C unless otherwise specified; Using factory-calibrated settings.

Parameter	Test Condition	Min	Typ	Max	Unit
Oscillator Frequency	IFCN = 11b	47.3	48	48.7	MHz
Oscillator Supply Current (from V_{DD})	25 °C, V_{DD} = 3.0 V, OSCICN.7 = 1, OCSICN.5 = 0	—	900	—	µA
Power Supply Sensitivity	Constant Temperature	—	110	—	ppm/V
Temperature Sensitivity	Constant Supply	—	25	—	ppm/°C

Table 5.8. Internal Low-Frequency Oscillator Electrical Characteristics

V_{DD} = 2.7 to 3.6 V; T_A = –40 to +85 °C unless otherwise specified; Using factory-calibrated settings.

Parameter	Test Condition	Min	Typ	Max	Unit
Oscillator Frequency	OSCLD = 11b	75	80	85	kHz
Oscillator Supply Current (from V_{DD})	25 °C, V_{DD} = 3.0 V, OSCLCN.7 = 1	—	4	—	µA
Power Supply Sensitivity	Constant Temperature	—	0.05	—	%/V
Temperature Sensitivity	Constant Supply	—	65	—	ppm/°C

Table 5.9. External Oscillator Electrical Characteristics

V_{DD} = 2.7 to 3.6 V; T_A = –40 to +85 °C unless otherwise specified.

Parameter	Test Condition	Min	Typ	Max	Unit
External Crystal Frequency		0.02	—	30	MHz
External CMOS Oscillator Frequency		0	—	48	MHz

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6.1. Output Code Formatting

The conversion code format differs between Single-ended and Differential modes. The registers ADC0H and ADC0L contain the high and low bytes of the output conversion code from the ADC at the completion of each conversion. Data can be right-justified or left-justified, depending on the setting of the AD0LJST bit (ADC0CN.0). When in Single-ended Mode, conversion codes are represented as 10-bit unsigned integers. Inputs are measured from 0 to VREF x 1023/1024. Example codes are shown below for both right-justified and left-justified data. Unused bits in the ADC0H and ADC0L registers are set to 0.

Input Voltage (Single-Ended)	Right-Justified ADC0H:ADC0L (AD0LJST = 0)	Left-Justified ADC0H:ADC0L (AD0LJST = 1)
VREF x 1023/1024	0x03FF	0xFFC0
VREF x 512/1024	0x0200	0x8000
VREF x 256/1024	0x0100	0x4000
0	0x0000	0x0000

When in Differential Mode, conversion codes are represented as 10-bit signed 2s complement numbers. Inputs are measured from –VREF to VREF x 511/512. Example codes are shown below for both right-justified and left-justified data. For right-justified data, the unused MSBs of ADC0H are a sign-extension of the data word. For left-justified data, the unused LSBs in the ADC0L register are set to 0.

Input Voltage (Differential)	Right-Justified ADC0H:ADC0L (AD0LJST = 0)	Left-Justified ADC0H:ADC0L (AD0LJST = 1)
VREF x 511/512	0x01FF	0x7FC0
VREF x 256/512	0x0100	0x4000
0	0x0000	0x0000
–VREF x 256/512	0xFF00	0xC000
–VREF	0xFE00	0x8000

SFR Definition 6.4. ADC0CN: ADC0 Control

Bit	7	6	5	4	3	2	1	0
Name	AD0EN	AD0TM	AD0INT	AD0BUSY	AD0WINT	AD0CM[2:0]		
Type	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE8; SFR Page = All Pages; Bit-Addressable

Bit	Name	Function
7	AD0EN	**ADC0 Enable Bit.** 0: ADC0 Disabled. ADC0 is in low-power shutdown. 1: ADC0 Enabled. ADC0 is active and ready for data conversions.
6	AD0TM	**ADC0 Track Mode Bit.** 0: Normal Track Mode: When ADC0 is enabled, tracking is continuous unless a conversion is in progress. Conversion begins immediately on start-of-conversion event, as defined by AD0CM[2:0]. 1: Delayed Track Mode: When ADC0 is enabled, input is tracked when a conversion is not in progress. A start-of-conversion signal initiates three SAR clocks of additional tracking, and then begins the conversion. Note that there is not a tracking delay when CNVSTR is used (AD0CM[2:0] = 100).
5	AD0INT	**ADC0 Conversion Complete Interrupt Flag.** 0: ADC0 has not completed a data conversion since AD0INT was last cleared. 1: ADC0 has completed a data conversion.
4	AD0BUSY	**ADC0 Busy Bit.** **Read:** 0: ADC0 conversion is not in progress. 1: ADC0 conversion is in progress. **Write:** 0: No Effect. 1: Initiates ADC0 Conversion if AD0CM[2:0] = 000b
3	AD0WINT	**ADC0 Window Compare Interrupt Flag.** 0: ADC0 Window Comparison Data match has not occurred since this flag was last cleared. 1: ADC0 Window Comparison Data match has occurred.
2:0	AD0CM[2:0]	**ADC0 Start of Conversion Mode Select.** 000: ADC0 start-of-conversion source is write of 1 to AD0BUSY. 001: ADC0 start-of-conversion source is overflow of Timer 0. 010: ADC0 start-of-conversion source is overflow of Timer 2. 011: ADC0 start-of-conversion source is overflow of Timer 1. 100: ADC0 start-of-conversion source is rising edge of external CNVSTR. 101: ADC0 start-of-conversion source is overflow of Timer 3. 110: ADC0 start-of-conversion source is overflow of Timer 4. 111: ADC0 start-of-conversion source is overflow of Timer 5.

6.5. ADC0 Analog Multiplexer

AMUX0 selects the positive and negative inputs to the ADC. The positive input (AIN+) can be connected to individual Port pins, the on-chip temperature sensor, or the positive power supply (V_{DD}). The negative input (AIN-) can be connected to individual Port pins, VREF, or GND. When GND is selected as the negative input, ADC0 operates in Single-ended Mode; at all other times, ADC0 operates in Differential Mode. The ADC0 input channels are selected in the AMX0P and AMX0N registers as described in SFR Definition 6.9 and SFR Definition 6.10.

Important Note About ADC0 Input Configuration: Port pins selected as ADC0 inputs should be configured as analog inputs, and should be skipped by the Digital Crossbar. To configure a Port pin for analog input, set to 0 the corresponding bit in register PnMDIN. To force the Crossbar to skip a Port pin, set to 1 the corresponding bit in register PnSKIP. See Section "20. Port Input/Output" on page 147 for more Port I/O configuration details.

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7. Voltage Reference Options

The Voltage reference multiplexer for the ADC is configurable to use an externally connected voltage reference, the on-chip reference voltage generator routed to the VREF pin, the unregulated power supply voltage (V_{DD}), or the regulated 1.8 V internal supply (see Figure 7.1). The REFSL bit in the Reference Control register (REF0CN, SFR Definition 7.1) selects the reference source for the ADC. For an external source or the on-chip reference, REFSL should be set to 0 to select the VREF pin. To use V_{DD} as the reference source, REFSL should be set to 1. To override this selection and use the internal regulator as the reference source, the REGOVR bit can be set to 1.

The BIASE bit enables the internal voltage bias generator, which is used by many of the analog peripherals on the device. This bias is automatically enabled when any peripheral which requires it is enabled, and it does not need to be enabled manually. The bias generator may be enabled manually by writing a 1 to the BIASE bit in register REF0CN. The electrical specifications for the voltage reference circuit are given in Table 5.12.

The C8051F388/9/A/B devices also include an on-chip voltage reference circuit which consists of a 1.2 V, temperature stable bandgap voltage reference generator and a selectable-gain output buffer amplifier. The buffer is configured for 1x or 2x gain using the REFBGS bit in register REF0CN. On the 1x gain setting the output voltage is nominally 1.2 V, and on the 2x gain setting the output voltage is nominally 2.4 V. The on-chip voltage reference can be driven on the VREF pin by setting the REFBE bit in register REF0CN to a 1. The maximum load seen by the VREF pin must be less than 200 µA to GND. Bypass capacitors of 0.1 µF and 4.7 µF are recommended from the VREF pin to GND, and a minimum of 0.1uF is required. If the on-chip reference is not used, the REFBE bit should be cleared to 0. Electrical specifications for the on-chip voltage reference are given in Table 5.12.

Important Note about the VREF Pin: When using either an external voltage reference or the on-chip reference circuitry, the VREF pin should be configured as an analog pin and skipped by the Digital Crossbar. Refer to Section "20. Port Input/Output" on page 147 for the location of the VREF pin, as well as details of how to configure the pin in analog mode and to be skipped by the crossbar.
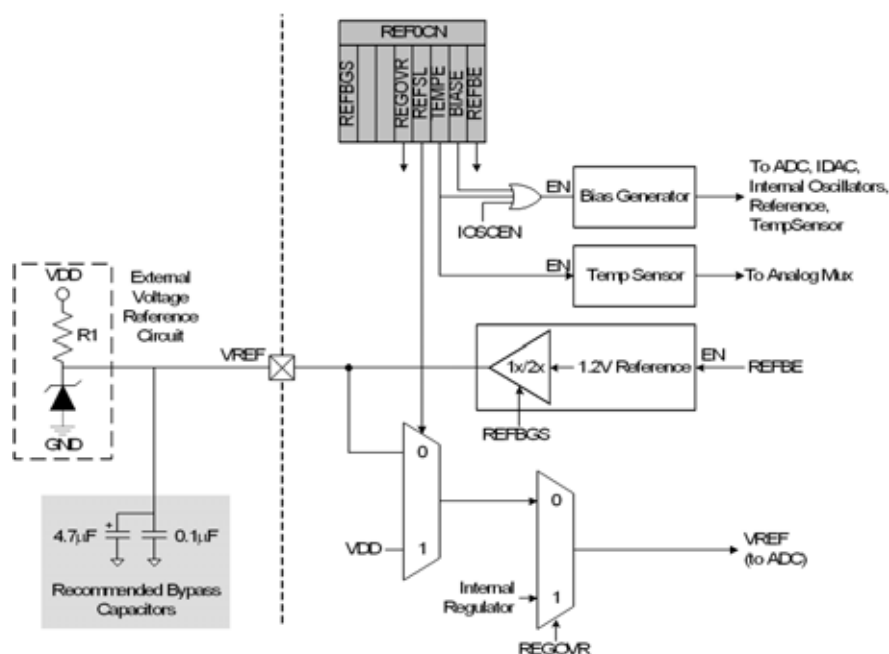
Figure 7.1. Voltage Reference Functional Block Diagram

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SFR Definition 8.2. CPT0MD: Comparator0 Mode Selection

Bit	7	6	5	4	3	2	1	0
Name			CP0RIE	CP0FIE			CP0MD[1:0]	
Type	R	R	R/W	R/W	R	R	R/W	
Reset	0	0	0	0	0	0	1	0

SFR Address = 0x9D; SFR Page = All Pages

Bit	Name	Function
7:6	Unused	Read = 00b, Write = don't care.
5	CP0RIE	**Comparator0 Rising-Edge Interrupt Enable.** 0: Comparator0 Rising-edge interrupt disabled. 1: Comparator0 Rising-edge interrupt enabled.
4	CP0FIE	**Comparator0 Falling-Edge Interrupt Enable.** 0: Comparator0 Falling-edge interrupt disabled. 1: Comparator0 Falling-edge interrupt enabled.
3:2	Unused	Read = 00b, Write = don't care.
1:0	CP0MD[1:0]	**Comparator0 Mode Select.** These bits affect the response time and power consumption for Comparator0. 00: Mode 0 (Fastest Response Time, Highest Power Consumption) 01: Mode 1 10: Mode 2 11: Mode 3 (Slowest Response Time, Lowest Power Consumption)

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17.6. PCA Watchdog Timer Reset

The programmable Watchdog Timer (WDT) function of the Programmable Counter Array (PCA) can be used to prevent software from running out of control during a system malfunction. The PCA WDT function can be enabled or disabled by software as described in Section "26.4. Watchdog Timer Mode" on page 269; the WDT is enabled and clocked by SYSCLK / 12 following any reset. If a system malfunction prevents user software from updating the WDT, a reset is generated and the WDTRSF bit (RSTSRC.5) is set to 1. The state of the $\overline{RST}$ pin is unaffected by this reset.

17.7. Flash Error Reset

If a Flash program read, write, or erase operation targets an illegal address, a system reset is generated. This may occur due to any of the following:

- Programming hardware attempts to write or erase a Flash location which is above the user code space address limit.
- A Flash read from firmware is attempted above user code space. This occurs when a MOVC operation is attempted above the user code space address limit.
- A Program read is attempted above user code space. This occurs when user code attempts to branch to an address above the user code space address limit.
- A Flash read, write, or erase attempt is restricted due to a Flash security setting.
- A Flash write or erase is attempted when the V_{DD} monitor is not enabled.

The FERROR bit (RSTSRC.6) is set following a Flash error reset. The state of the $\overline{RST}$ pin is unaffected by this reset.

17.8. Software Reset

Software may force a reset by writing a 1 to the SWRSF bit (RSTSRC.4). The SWRSF bit will read 1 following a software forced reset. The state of the $\overline{RST}$ pin is unaffected by this reset.

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20.2. Port I/O Initialization

Port I/O initialization consists of the following steps:

1. Select the input mode (analog or digital) for all Port pins, using the Port Input Mode register (PnMDIN).
2. Select the output mode (open-drain or push-pull) for all Port pins, using the Port Output Mode register (PnMDOUT).
3. Select any pins to be skipped by the I/O Crossbar using the Port Skip registers (PnSKIP).
4. Assign Port pins to desired peripherals (XBR0, XBR1).
5. Enable the Crossbar (XBARE = 1).

All Port pins must be configured as either analog or digital inputs. Any pins to be used as Comparator or ADC inputs should be configured as an analog inputs. When a pin is configured as an analog input, its weak pull-up, digital driver, and digital receiver are disabled. This process saves power and reduces noise on the analog input. Pins configured as digital inputs may still be used by analog peripherals; however this practice is not recommended. To configure a Port pin for digital input, write 0 to the corresponding bit in register PnMDOUT, and write 1 to the corresponding Port latch (register Pn).

Additionally, all analog input pins should be configured to be skipped by the Crossbar (accomplished by setting the associated bits in PnSKIP). Port input mode is set in the PnMDIN register, where a 1 indicates a digital input, and a 0 indicates an analog input. All pins default to digital inputs on reset.

The output driver characteristics of the I/O pins are defined using the Port Output Mode registers (PnMDOUT). Each Port Output driver can be configured as either open drain or push-pull. This selection is required even for the digital resources selected in the XBRn registers, and is not automatic. The only exception to this are the SMBus (SDA, SCL, SDA1 and SCL1) pins, which are configured as open-drain regardless of the PnMDOUT settings. When the WEAKPUD bit in XBR1 is 0, a weak pull-up is enabled for all Port I/O configured as open-drain. WEAKPUD does not affect the push-pull Port I/O. Furthermore, the weak pull-up is turned off on an output that is driving a 0 to avoid unnecessary power dissipation.

Registers XBR0 and XBR1 must be loaded with the appropriate values to select the digital I/O functions required by the design. Setting the XBARE bit in XBR1 to 1 enables the Crossbar. Until the Crossbar is enabled, the external pins remain as standard Port I/O (in input mode), regardless of the XBRn Register settings. For given XBRn Register settings, one can determine the I/O pin-out using the Priority Decode Table; as an alternative, the Configuration Wizard utility of the Silicon Labs IDE software will determine the Port I/O pin-assignments based on the XBRn Register settings.

Important Note: The Crossbar must be enabled to use Ports P0, P1, P2, and P3 as standard Port I/O in output mode. These Port output drivers are disabled while the Crossbar is disabled. Port 4 always functions as standard GPIO.

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SFR Definition 20.10. P1MDOUT: Port 1 Output Mode

Bit	7	6	5	4	3	2	1	0
Name	P1MDOUT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xA5; SFR Page = All Pages

Bit	Name	Function
7:0	P1MDOUT[7:0]	**Output Configuration Bits for P1.7–P1.0 (respectively).** These bits are ignored if the corresponding bit in register P1MDIN is logic 0. 0: Corresponding P1.n Output is open-drain. 1: Corresponding P1.n Output is push-pull.

SFR Definition 20.11. P1SKIP: Port 1 Skip

Bit	7	6	5	4	3	2	1	0
Name	P1SKIP[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xD5; SFR Page = All Pages

Bit	Name	Function
7:0	P1SKIP[7:0]	**Port 1 Crossbar Skip Enable Bits.** These bits select Port 1 pins to be skipped by the Crossbar Decoder. Port pins used for analog, special functions or GPIO should be skipped by the Crossbar. 0: Corresponding P1.n pin is not skipped by the Crossbar. 1: Corresponding P1.n pin is skipped by the Crossbar.

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SFR Definition 21.4. SMB0CN: SMBus Control

Bit	7	6	5	4	3	2	1	0
Name	MASTER0	TXMODE0	STA0	STO0	ACKRQ0	ARBLOST0	ACK0	SI0
Type	R	R	R/W	R/W	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC0; SFR Page = 0; Bit-Addressable

Bit	Name	Description	Read	Write
7	MASTER0	**SMBus0 Master/Slave Indicator.** This read-only bit indicates when the SMBus0 is operating as a master.	0: SMBus0 operating in slave mode. 1: SMBus0 operating in master mode.	N/A
6	TXMODE0	**SMBus0 Transmit Mode Indicator.** This read-only bit indicates when the SMBus0 is operating as a transmitter.	0: SMBus0 in Receiver Mode. 1: SMBus0 in Transmitter Mode.	N/A
5	STA0	**SMBus0 Start Flag.**	0: No Start or repeated Start detected. 1: Start or repeated Start detected.	0: No Start generated. 1: When Configured as a Master, initiates a START or repeated START.
4	STO0	**SMBus0 Stop Flag.**	0: No Stop condition detected. 1: Stop condition detected (if in Slave Mode) or pending (if in Master Mode).	0: No STOP condition is transmitted. 1: When configured as a Master, causes a STOP condition to be transmitted after the next ACK cycle. Cleared by Hardware.
3	ACKRQ0	**SMBus0 Acknowledge Request.**	0: No ACK requested 1: ACK requested	N/A
2	ARBLOST0	**SMBus0 Arbitration Lost Indicator.**	0: No arbitration error. 1: Arbitration Lost	N/A
1	ACK0	**SMBus0 Acknowledge.**	0: NACK received. 1: ACK received.	0: Send NACK 1: Send ACK
0	SI0	**SMBus0 Interrupt Flag.** This bit is set by hardware under the conditions listed in Table 15.3. SI0 must be cleared by software. While SI0 is set, SCL0 is held low and the SMBus0 is stalled.	0: No interrupt pending 1: Interrupt Pending	0: Clear interrupt, and initiate next state machine event. 1: Force interrupt.

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Table 21.5. SMBus Status Decoding: Hardware ACK Disabled (EHACK = 0) (Continued)

Mode	Values Read				Current SMbus State	Typical Response Options	Values to Write			Next Status Vector Expected
	Status Vector	ACKRQ	ARBLOST	ACK			STA	STO	ACK	
Bus Error Condition	0010	0	1	X	Lost arbitration while attempting a repeated START.	Abort failed transfer.	0	0	X	—
						Reschedule failed transfer.	1	0	X	1110
	0001	0	1	X	Lost arbitration due to a detected STOP.	Abort failed transfer.	0	0	X	—
						Reschedule failed transfer.	1	0	X	1110
	0000	1	1	X	Lost arbitration while transmitting a data byte as master.	Abort failed transfer.	0	0	0	—
						Reschedule failed transfer.	1	0	0	1110

Table 21.6. SMBus Status Decoding: Hardware ACK Enabled (EHACK = 1)

Mode	Values Read				Current SMbus State	Typical Response Options	Values to Write			Next Status Vector Expected
	Status Vector	ACKRQ	ARBLOST	ACK			STA	STO	ACK	
Master Transmitter	1110	0	0	X	A master START was generated.	Load slave address + R/W into SMB0DAT.	0	0	X	1100
	1100	0	0	0	A master data or address byte was transmitted; NACK received.	Set STA to restart transfer.	1	0	X	1110
						Abort transfer.	0	1	X	—
		0	0	1	A master data or address byte was transmitted; ACK received.	Load next data byte into SMB0-DAT.	0	0	X	1100
						End transfer with STOP.	0	1	X	—
						End transfer with STOP and start another transfer.	1	1	X	—
						Send repeated START.	1	0	X	1110
						Switch to Master Receiver Mode (clear SI without writing new data to SMB0DAT). Set ACK for initial data byte.	0	0	1	1000

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23. UART1

UART1 is an asynchronous, full duplex serial port offering a variety of data formatting options. A dedicated baud rate generator with a 16-bit timer and selectable prescaler is included, which can generate a wide range of baud rates (details in Section "23.1. Baud Rate Generator" on page 202). A received data FIFO allows UART1 to receive up to three data bytes before data is lost and an overflow occurs.

UART1 has six associated SFRs. Three are used for the Baud Rate Generator (SBCON1, SBRLH1, and SBRLL1), two are used for data formatting, control, and status functions (SCON1, SMOD1), and one is used to send and receive data (SBUF1). The single SBUF1 location provides access to both the transmit holding register and the receive FIFO. **Writes to SBUF1 always access the Transmit Holding Register. Reads of SBUF1 always access the first byte of the Receive FIFO; it is not possible to read data from the Transmit Holding Register.**

With UART1 interrupts enabled, an interrupt is generated each time a transmit is completed (TI1 is set in SCON1), or a data byte has been received (RI1 is set in SCON1). The UART1 interrupt flags are not cleared by hardware when the CPU vectors to the interrupt service routine. They must be cleared manually by software, allowing software to determine the cause of the UART1 interrupt (transmit complete or receive complete). Note that if additional bytes are available in the Receive FIFO, the RI1 bit cannot be cleared by software.
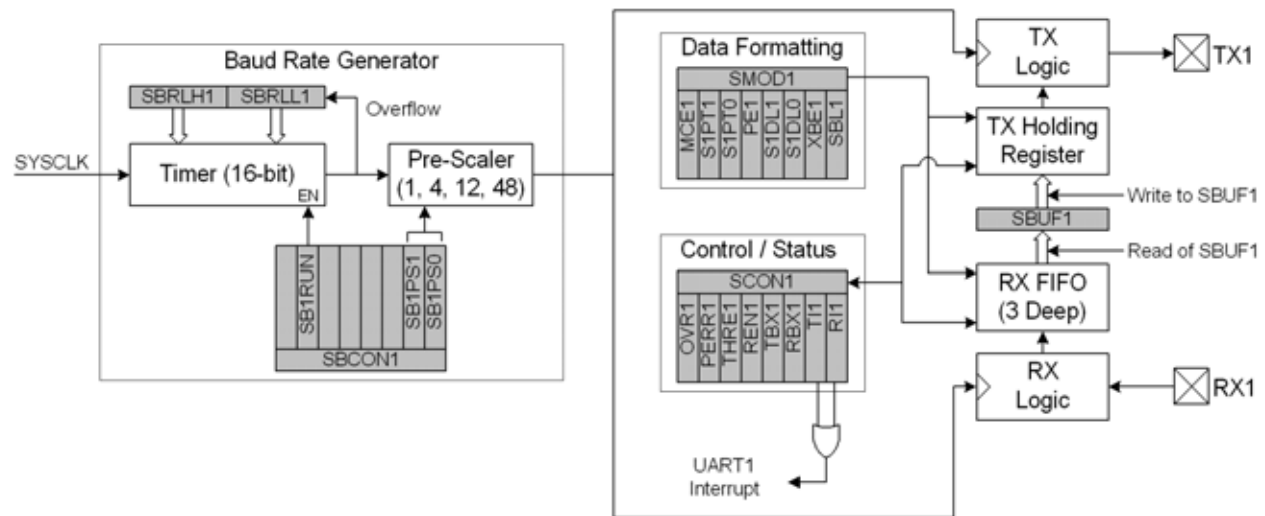

Figure 23.1. UART1 Block Diagram

SFR Definition 23.2. SMOD1: UART1 Mode

Bit	7	6	5	4	3	2	1	0
Name	MCE1	S1PT[1:0]		PE1	S1DL[1:0]		XBE1	SBL1
Type	R/W	R/W		R/W	R/W		R/W	R/W
Reset	0	0	0	0	1	1	0	0

SFR Address = 0xE5; SFR Page = All Pages

Bit	Name	Function
7	MCE1	**Multiprocessor Communication Enable.** 0: RI will be activated if stop bit(s) are 1. 1: RI will be activated if stop bit(s) and extra bit are 1 (extra bit must be enabled using XBE1). Note: This function is not available when hardware parity is enabled.
6:5	S1PT[1:0]	**Parity Type Bits.** 00: Odd 01: Even 10: Mark 11: Space
4	PE1	**Parity Enable.** This bit activates hardware parity generation and checking. The parity type is selected by bits S1PT1-0 when parity is enabled. 0: Hardware parity is disabled. 1: Hardware parity is enabled.
3:2	S1DL[1:0]	**Data Length.** 00: 5-bit data 01: 6-bit data 10: 7-bit data 11: 8-bit data
1	XBE1	**Extra Bit Enable.** When enabled, the value of TBX1 will be appended to the data field. 0: Extra Bit Disabled. 1: Extra Bit Enabled.
0	SBL1	**Stop Bit Length.** 0: Short—Stop bit is active for one bit time. 1: Long—Stop bit is active for two bit times (data length = 6, 7, or 8 bits), or 1.5 bit times (data length = 5 bits).

SFR Definition 23.6. SBRLL1: UART1 Baud Rate Generator Low Byte

Bit	7	6	5	4	3	2	1	0
Name	SBRLL1[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xB4; SFR Page = All Pages

Bit	Name	Function
7:0	SBRLL1[7:0]	**UART1 Baud Rate Reload Low Bits.** Low Byte of reload value for UART1 Baud Rate Generator.

25.5.2. 8-bit Timers with Auto-Reload

When T5SPLIT is 1 and T5CE = 0, Timer 5 operates as two 8-bit timers (TMR5H and TMR5L). Both 8-bit timers operate in auto-reload mode as shown in Figure 25.15. TMR5RLL holds the reload value for TMR5L; TMR5RLH holds the reload value for TMR5H. The TR5 bit in TMR5CN handles the run control for TMR5H. TMR5L is always running when configured for 8-bit Mode.

Each 8-bit timer may be configured to use SYSCLK, SYSCLK divided by 12, or the external oscillator clock source divided by 8. The Timer 5 Clock Select bits (T5MH and T5ML in CKCON1) select either SYSCLK or the clock defined by the Timer 5 External Clock Select bit (T5XCLK in TMR5CN), as follows:

T5MH	T5XCLK	TMR5H Clock Source
0	0	SYSCLK/12
0	1	External Clock/8
1	X	SYSCLK

T5ML	T5XCLK	TMR5L Clock Source
0	0	SYSCLK/12
0	1	External Clock/8
1	X	SYSCLK

The TF5H bit is set when TMR5H overflows from 0xFF to 0x00; the TF5L bit is set when TMR5L overflows from 0xFF to 0x00. When Timer 5 interrupts are enabled, an interrupt is generated each time TMR5H overflows. If Timer 5 interrupts are enabled and TF5LEN (TMR5CN.5) is set, an interrupt is generated each time either TMR5L or TMR5H overflows. When TF5LEN is enabled, software must check the TF5H and TF5L flags to determine the source of the Timer 5 interrupt. The TF5H and TF5L interrupt flags are not cleared by hardware and must be manually cleared by software.
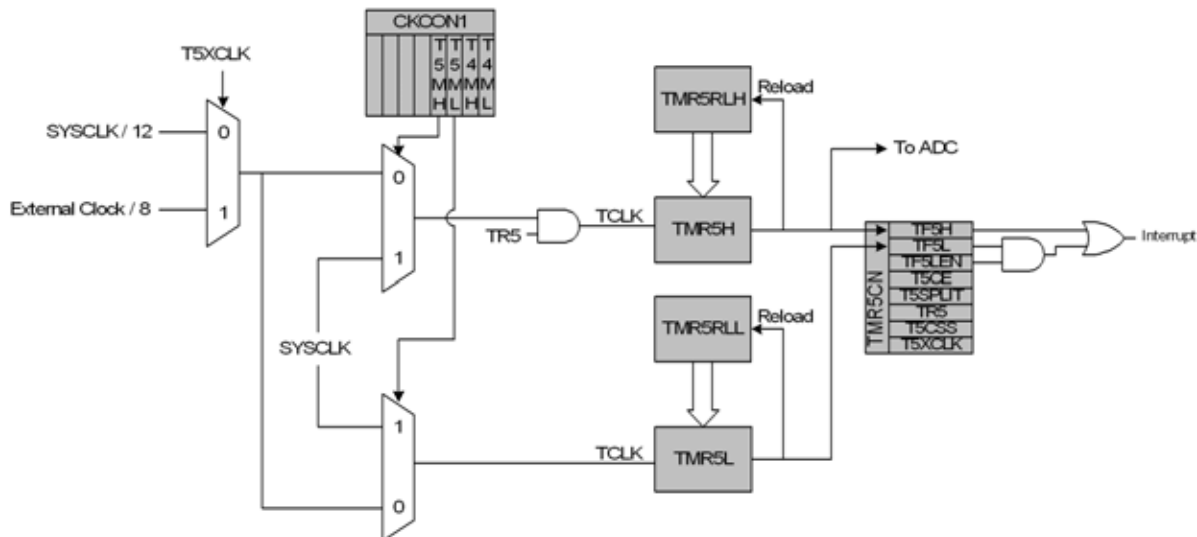

Figure 25.15. Timer 5 8-Bit Mode Block Diagram

26.3.2. Software Timer (Compare) Mode

In Software Timer mode, the PCA counter/timer value is compared to the module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn). When a match occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Setting the ECOMn and MATn bits in the PCA0CPMn register enables Software Timer mode.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.
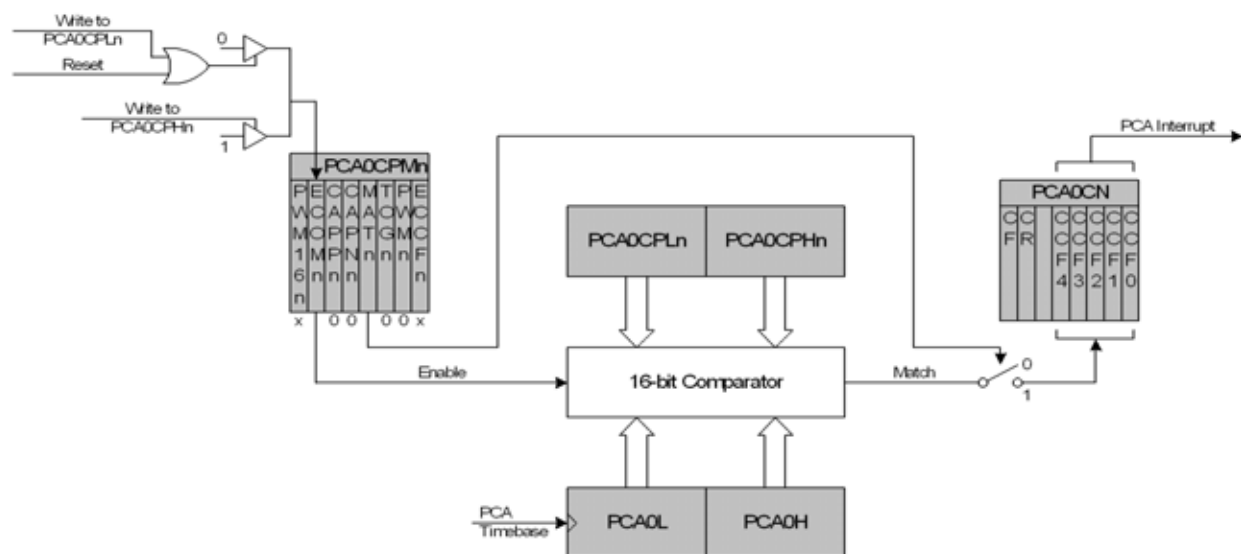

Figure 26.5. PCA Software Timer Mode Diagram